



UNIVERSITY OF PISA  
MASTER'S DEGREE IN CYBERSECURITY

TITLE

COURSE HARDWARE AND EMBEDDED SECURITY

Author(s)

**Bernardini Diego, Cisternini Giovanni**

Academic year 2024/2025

---

---

## Contents

---

<b>1</b>	<b>Project Specifications</b>	<b>1</b>
<b>2</b>	<b>High-level Model</b>	<b>2</b>
<b>3</b>	<b>RTL Design</b>	<b>3</b>
<b>4</b>	<b>Interface Specifications and Expected Behavior</b>	<b>5</b>
<b>5</b>	<b>Functional Verification</b>	<b>6</b>
<b>6</b>	<b>FPGA Implementation Results</b>	<b>7</b>

---

# CHAPTER *1*

---

## **Project Specifications**

---

An introduction to the project, including the specifications and their analysis

---

## CHAPTER 2

---

### High-level Model

---

Description of the high-level model (Python or C/C++ or other).

---

# CHAPTER 3

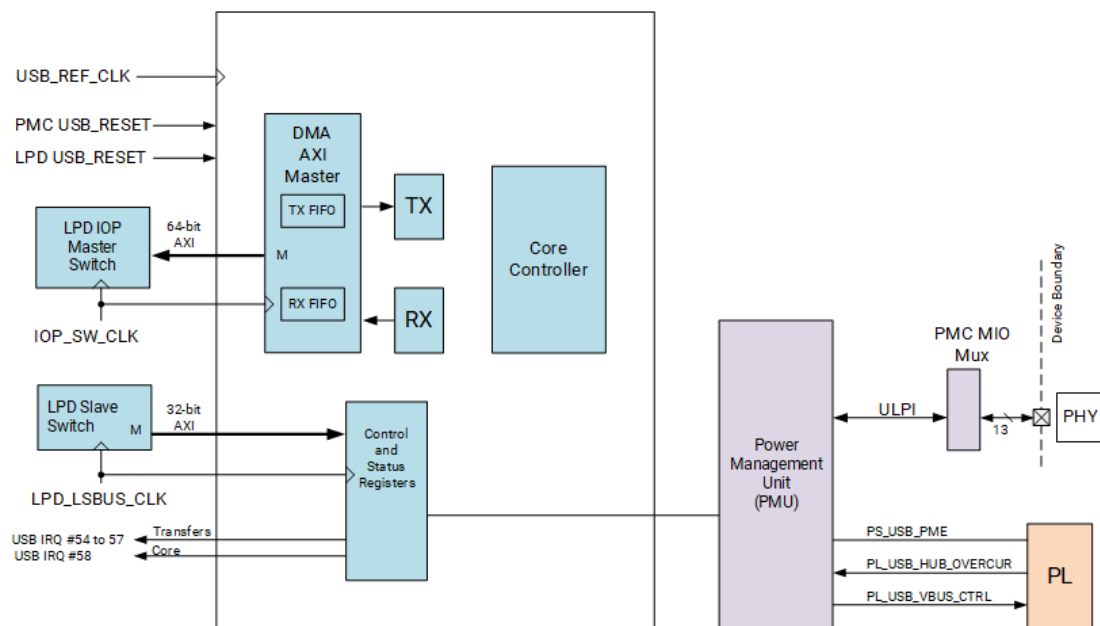
---

## RTL Design

---

Description of the RTL design architecture, with block diagrams, schematics (functional and/or architectural), FSM diagrams, etc ...

Figure 3.1 illustrates an example of high-level block diagram. Please, note the hierarchical organization and the usage of a blank triangle to indicate the edge-triggering logic of some blocks (i.e. blocks containing registers).



**Figure 3.1:** Example of high-level block diagram.

In Figure 3.1, DMA stands for Direct Access Memory, LPD indicates ... and so on. Remember to explain any symbols and/or terms and/or acronyms in figures and tables that have not been explicitly explained previously. Remember also to define each acronym before its usage!!!

---

## CHAPTER 4

---

### **Interface Specifications and Expected Behavior**

---

Describe how your module should be used in terms of how inputs should be provided (including timing) and what the corresponding output(s) would be. In practice, a kind of user manual, which may also include the waveforms at the input and/or output for several use cases (main case(s) and possible corner case(s)).

---

# CHAPTER 5

---

## Functional Verification

---

Describe how you tested your module, the testbench architecture, and what test(s) you performed to verify the functionality of your module according to the expected behavior described in Chapter 4



---

# CHAPTER 6

---

## FPGA Implementation Results

---

Describe the steps you performed on Quartus (including the FPGA device you used), the corresponding results such as resource utilization, maximum frequency, ..., and including comments on the results.

Remember that the maximum frequency is the result of the Static Timing Analysis (STA), which is optional.

Table 6.1 shows an example of table. The following link can be used to automatically generate the latex code for tables online: <https://www.tablesgenerator.com/>.

**Table 6.1:** *Example of table*

Heading 1	Heading 2	Heading 3
Value 1.1	Value 2.1	Value 3.1
Value 1.2	Value 2.2	Value 3.2