

# Demo 7: TimeQuest

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November 7, 2024

Question 8.

	Fmax	Setup Time
Slow 1100mV 85C	451.67 MHz	-19.472
Slow 110mV 0C	431.03 MHz	-20.359
Fast 1100mV 85C		-1.168
Fast 1100mV 0C		-0.924

Table 1: No clock constraint

Slow 1100mV 85C Model								
Command Info		Summary of Paths						
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-1.214	b_sync_2[4]	result_sync_1[14]	CLOCK_50	CLOCK_50	1.000	-0.069	1.975
2	-1.199	a_sync_2[3]	result_sync_1[14]	CLOCK_50	CLOCK_50	1.000	-0.082	1.947

Figure 1: Path Summary

Question 22. The clock was updated to match the results.

Question 23. The updated Fmax is now smaller than the Fmax without the constraint. This is because the smaller time constraint

	Fmax	Setup Time
Slow 1100mV 85C	398.72 MHz	0.000
Slow 110mV 0C	383.73 MHz	0.000
Fast 1100mV 85C		0.000
Fast 1100mV 0C		0.000

Table 2: With clock constraint

Slow 1100mV 85C Model								
Command Info		Summary of Paths						
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	17.492	a_sync_2[1]	result_sync_1[14]	clk	clk	20.000	-0.080	2.258
2	17.552	a_sync_2[1]	result_sync_1[12]	clk	clk	20.000	-0.078	2.200

Figure 2: Path Summary for 100 paths

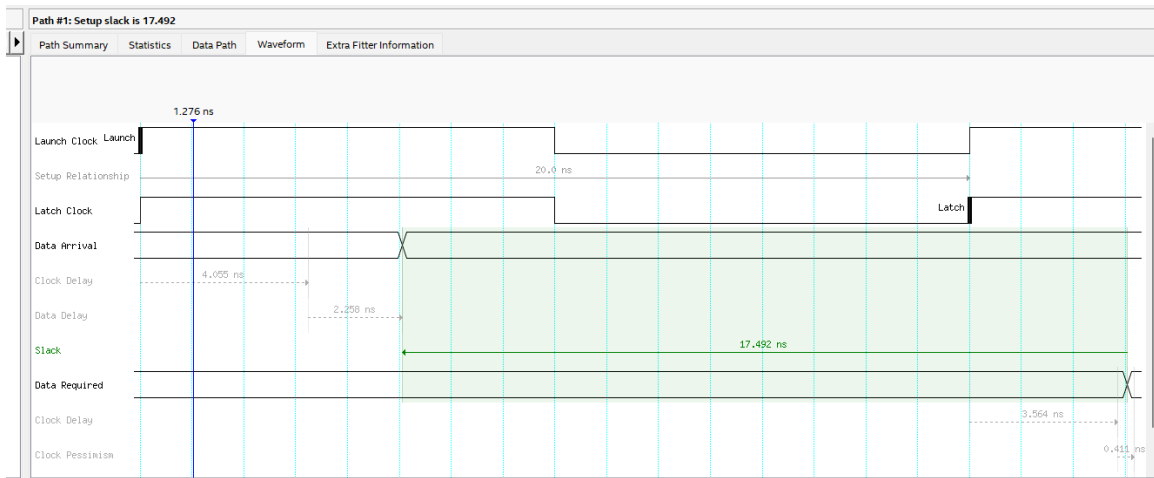


Figure 3: Path Summary for 100 paths

## Conclusion

TimeQuest is a timing analysis tool that helps test the timing of a design. The Fmax parameter is the max frequency and the Setup parameter is the minimum amount of time that the data must be stable before reaching a clock edge. Meeting the timing constraints ensures that the design operates reliably at the intended clock frequency, which is critical in embedded systems.