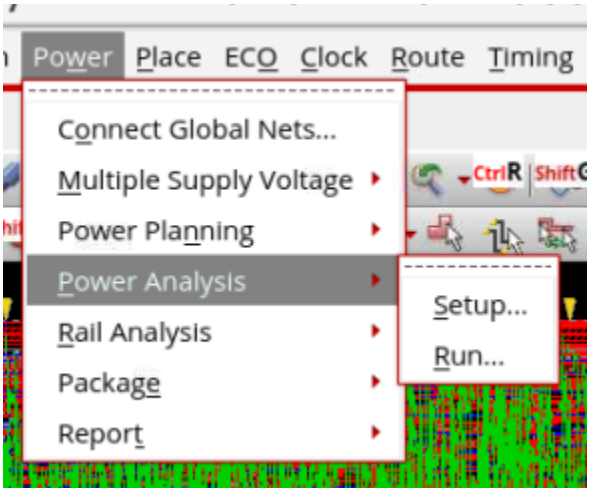
Refer to pages 1299-1302 of the Innovus User Guide document at "/usr/local/cadence/INNOVUS1710/doc/innovusUG/innovusUG.pdf".

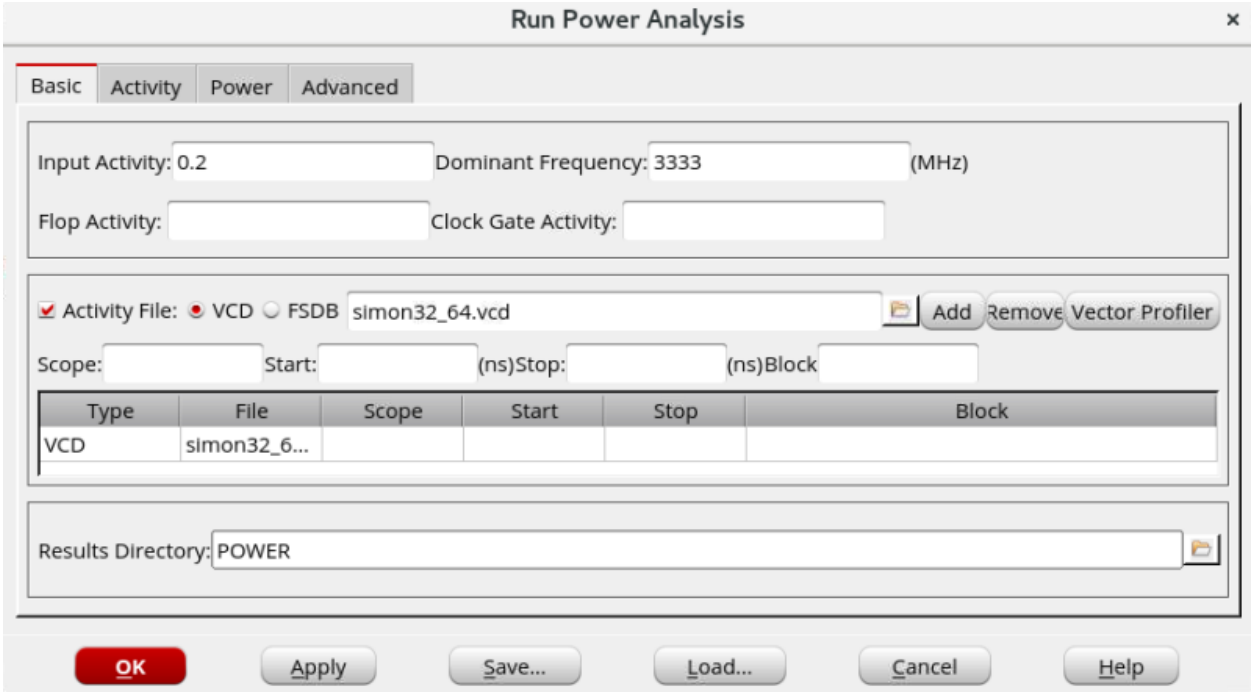
The following steps were followed for the VCD file based power analysis in Innovus:

1. The "**simon32_64.vcd**" file was generated from the modelsim simulation of "simon32_64.apr.v" file.

2. [**Power → Power Analysis → Run**] as shown in the picture below was selected.



3. The "**Run Power Analysis**" dialog box opens, as shown in the picture below.



Change the **dominant frequency** to your design's operating frequency of XXX GHz, which should be the highest frequency you can run APR without having any setup or hold time violations.

Check the **Activity File** check box and see that the **VCD** radio button is checked. Select the ***.vcd file** that you generated from the testbench Verilog simulation with the post-layout netlist, and then clock the **Add** button.

You will see that the **Results Directory** is changed to a local directory named "POWER".

4. Click the **OK** button at the bottom.

Then, "simon32_64.rpt" file will be generated in the selected "**Results Directory**". Include this "simon32_64.rpt" file in your final *.bz2 that you submit to Canvas for Lab 5 MS2.

In the Innovus command terminal, you will see the total power and breakdown as shown in the following picture. Take a screenshot of the picture like below, and add this power screenshot in your final report document for Lab 5 MS2.

```
Total Power
--------------------------------------------------------------------
Total Internal Power:       16.29372714            63.3803%
Total Switching Power:       9.41290611            36.6149%
Total Leakage Power:         0.00124994             0.0049%
Total Power:                25.70788327
--------------------------------------------------------------------
```