EDA Assignment 1

Thursday, September 4, 2025 8:54 PM

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Q 2.1. What do link library and source library refer to? (*2)*

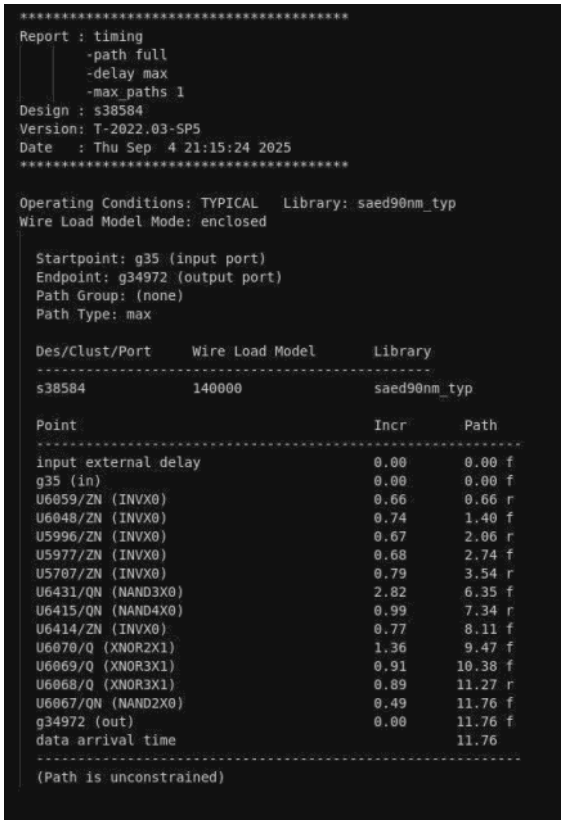
a. *The link library refers to a list of design files and libraries and resolves references to the specified files whereas source will read and evaluate TCL scripts. Both read files, but one links to the designs and the other sources the scripts.*

Q 2.2. What does '_typ', '_hvt', '_lvt' libraries mean? What does the last part mean in the name "saed32lvt_ff0p85v125c" for a library? What is the area for an MUX41X2 gate in saed90nm_typ library? (*2)*

a. *The ending of libraries show various performance corner suffixes such as '_typ' for typical silicon, '_hvt' for high voltage threshold, and '_lvt' for low voltage threshold. These directly impact the response times of the transistors.*
b. *The filename 'saed32lvt_ff0p85v125c' indicates an operation corner of low voltage threshold (_lvt), fast NMOS and PMOS devices (ff), 0.85V source voltage (0p85v), and hot operating temperature (125c)*
c. *The area of the MUX41x2 gate in saed90nm_typ is* 24.8832 um^2

Q 2.3. Parse the report files to obtain the start point and end point of a critical path. What is the max delay? (*2)*

a. *The delay seen from input to output of the critical path is 11.76fs, observed in the image below from the compiled s38584 _report.out report.*



```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : s38584
Version: T-2022.03-SP5
Date   : Thu Sep  4 21:15:24 2025
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: g35 (input port)
  Endpoint: g34972 (output port)
  Path Group: (none)
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  s38584             140000                saed90nm_typ

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 f
  g35 (in)                                 0.00       0.00 f
  U6059/ZN (INVX0)                         0.66       0.66 r
  U6048/ZN (INVX0)                         0.74       1.40 f
  U5996/ZN (INVX0)                         0.67       2.06 r
  U5977/ZN (INVX0)                         0.68       2.74 f
  U5707/ZN (INVX0)                         0.79       3.54 r
  U6431/QN (NAND3X0)                       2.82       6.35 f
  U6415/QN (NAND4X0)                       0.99       7.34 r
  U6414/ZN (INVX0)                         0.77       8.11 f
  U6070/Q (XNOR2X1)                        1.36       9.47 f
  U6069/Q (XNOR3X1)                        0.91      10.38 f
  U6068/Q (XNOR3X1)                        0.89      11.27 r
  U6067/QN (NAND2X0)                       0.49      11.76 f
  g34972 (out)                             0.00      11.76 f
  data arrival time                                  11.76
  -----------------------------------------------------------
  (Path is unconstrained)
```

Q 2.4. What is the total power consumption? (*2)*

a. *The delay seen from input to output of the critical path is 11.76fs, observed in the image below from the compiled s38584 _report.out report.*

```
Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =   4.4028 mW   (80%)
  Net Switching Power  =   1.1335 mW   (20%)
                         ---------
Total Dynamic Power    =   5.5363 mW  (100%)

Cell Leakage Power     = 445.6431 uW

Information: report_power power group summary does not include estimated clock tree power. (PWR-789)


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000             0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000             0.0000  (   0.00%)  i
register           0.0000           0.0000            0.0000             0.0000  (   0.00%)
sequential     2.3935e+03         102.2980        1.8521e+08         2.6810e+03  (  44.82%)
combinational  2.0093e+03        1.0312e+03        2.6043e+08         3.3010e+03  (  55.18%)
--------------------------------------------------------------------------------------------------
Total          4.4028e+03 uW     1.1335e+03 uW     4.4564e+08 pW      5.9820e+03 uW
1
```

Q 2.5. What is the net load, static probability, toggle rate and switching power for net n6833? *(2)*

a. *The net load, static probability, toggle rate and switching power for neet n6833 are as follows, collected from the s38584 _switching_power.txt:*

net load	5.933
static probability	0.001
toggle rate	0.92e-4
switching power	0.0004