Task-1(Mod-5 Counter)

- Designed mod-5 synchronous counter using Master Slave JK Flip-flop.
- Frequency of Operation-250MHz.
- For Schematic:
  Nmos:W=200nm,L=60nm
  Pmos:W=400nm,L=60nm
  Simulated the circuit and achieved the desired output.
  (The simulated output waveform is in the repository)
- For layout:
  Length=1.4um
  Width=63.735um
  Area =89.229um^2
- Cleared the DRC errors and also verified the LVS(The reports are attached in the repository).
- Performed the PEX analysis(pex report attached).
- Counter has 5 states:000,001,010,011,100,000…….
- The timing parameters of counter is in the spec file in the repository.
- The Rise time, Fall time, Delay time($T_{phl,}T_{plh}$)calculated for the inverter.
- Minimum frequency can be nearly to zero and to find maximum freq, I operated at 2Mhz and achieved correct output(Simulated waveform attached),After that operated at 3.125Mhz and was not able to achieve the output(waveform attached).So the Maximum freq is less than 3.125MHz.

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