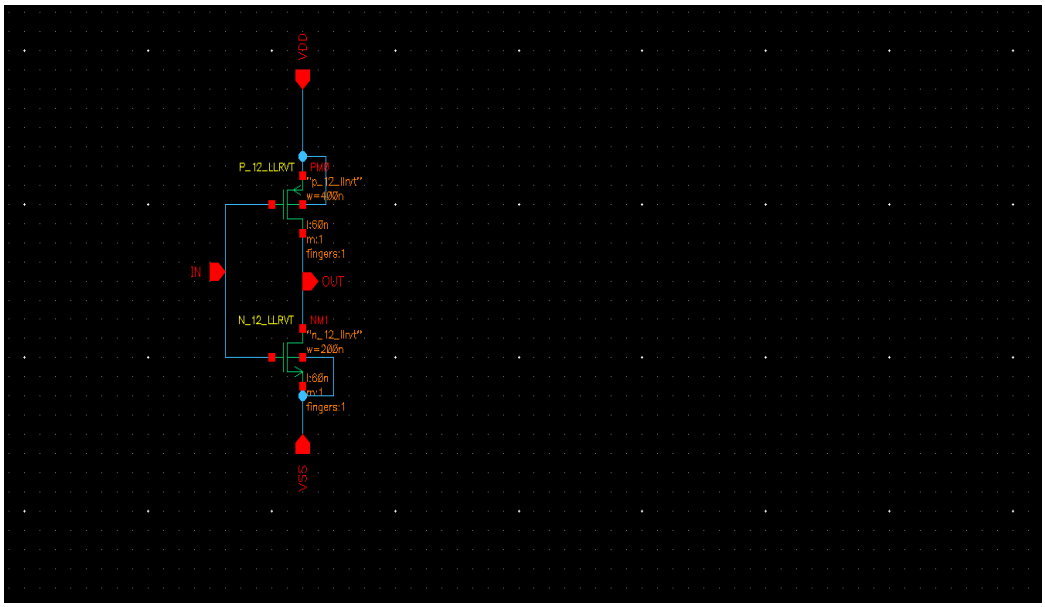
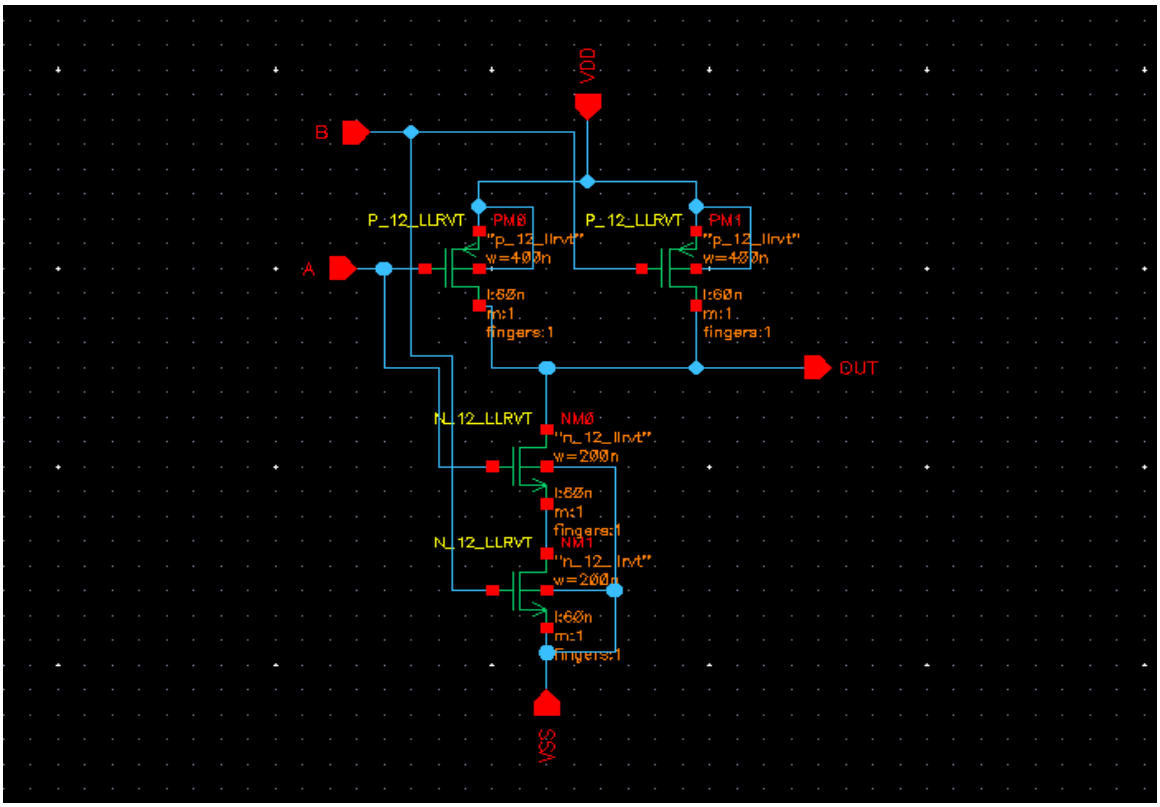
IEC Lab
Task-1(Mod-5 Counter)

- Designed mod-5 synchronous counter using Master Slave JK Flip-flop.
- Frequency of Operation-250MHz.
- For Schematic:
  Nmos:W=200nm,L=60nm
  Pmos:W=400nm,L=60nm
  Simulated the circuit and achieved the desired output.
  (The simulated output waveform and schematic are given below)
- For layout:
  Length=1.4um
  Width=63.735um
  Area =89.229um^2
- Cleared the DRC errors and also verified the LVS(The reports are attached in the repository).
- Performed the PEX analysis(pex report attached).
- Performed the Post Layout Simulation for which waveform is being given.
- Counter has 5 states:000,001,010,011,100,000…….
- The timing parameters of counter is in the spec file in the repository as well as given below.
- Setup and Hold time is same for the counter as well as for the ff.
- The Rise time, Fall time, Delay time(T_{phl},T_{plh}) is calculated for the Counter
- Setup time is calculated
- After that max frequency is being calculated below.

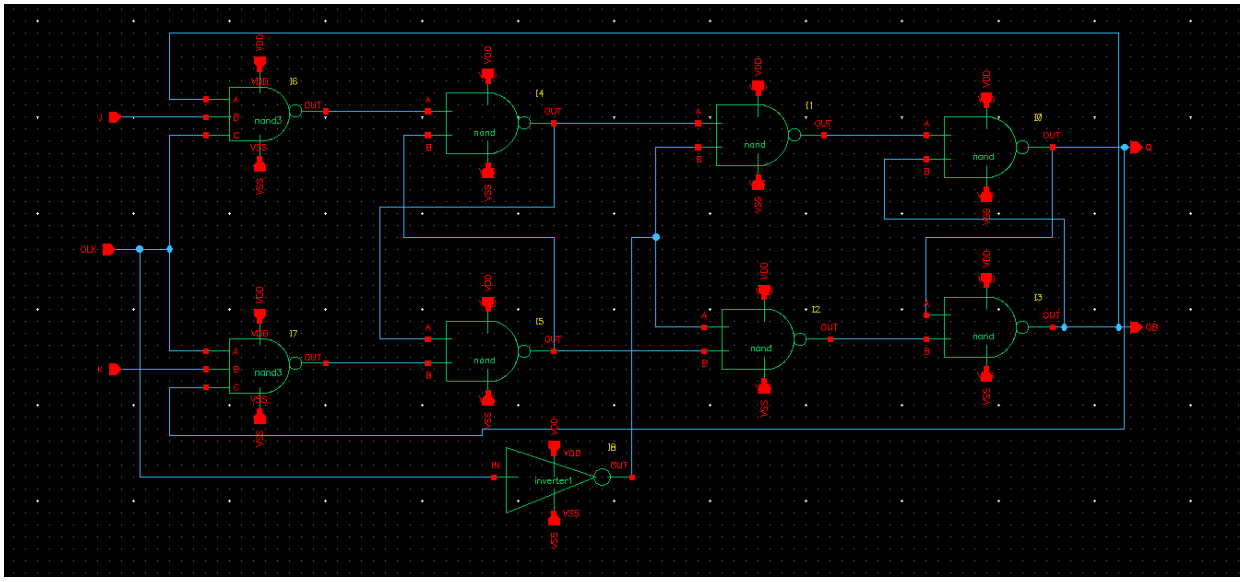
Inverter Schematic:



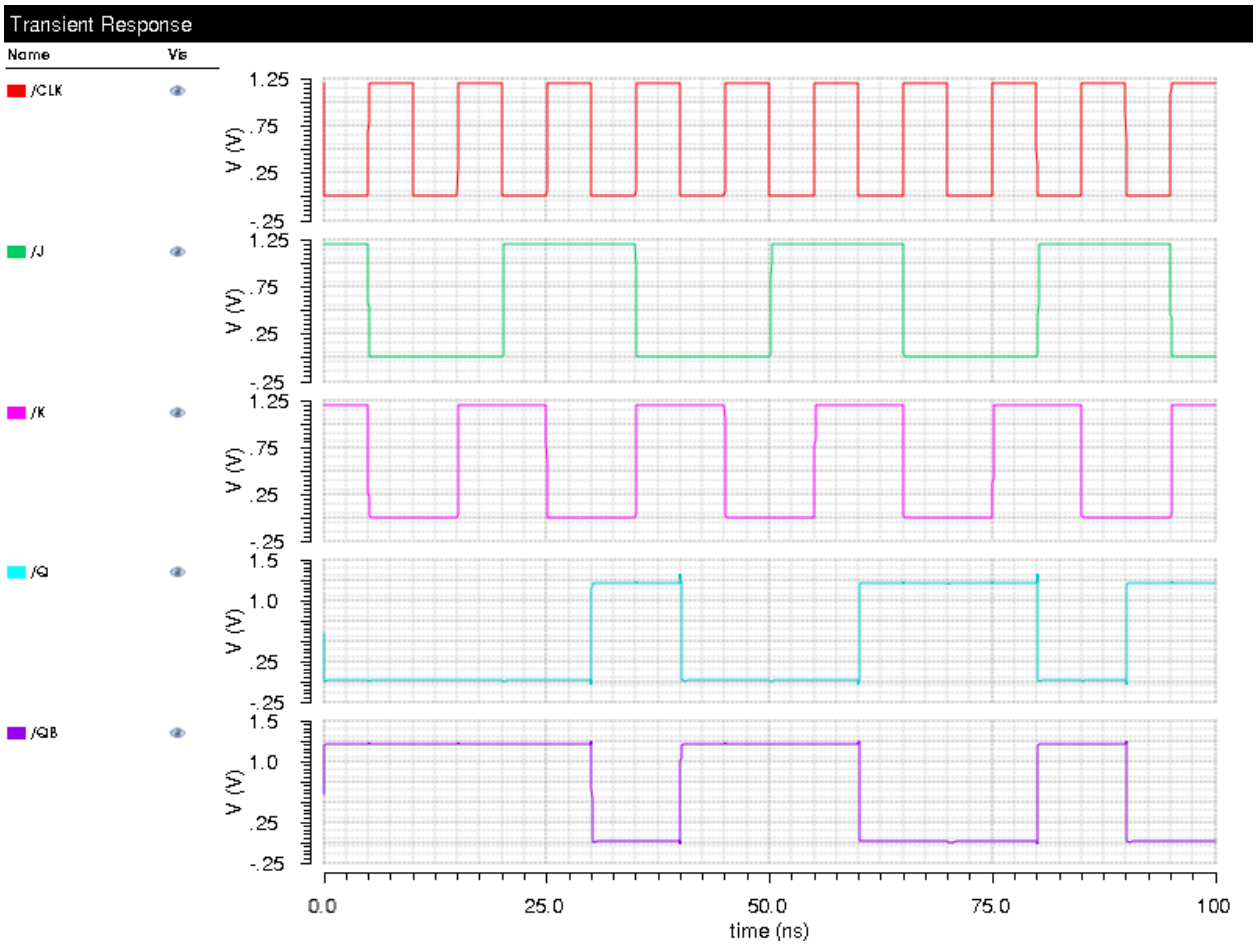
Nand Schematic:



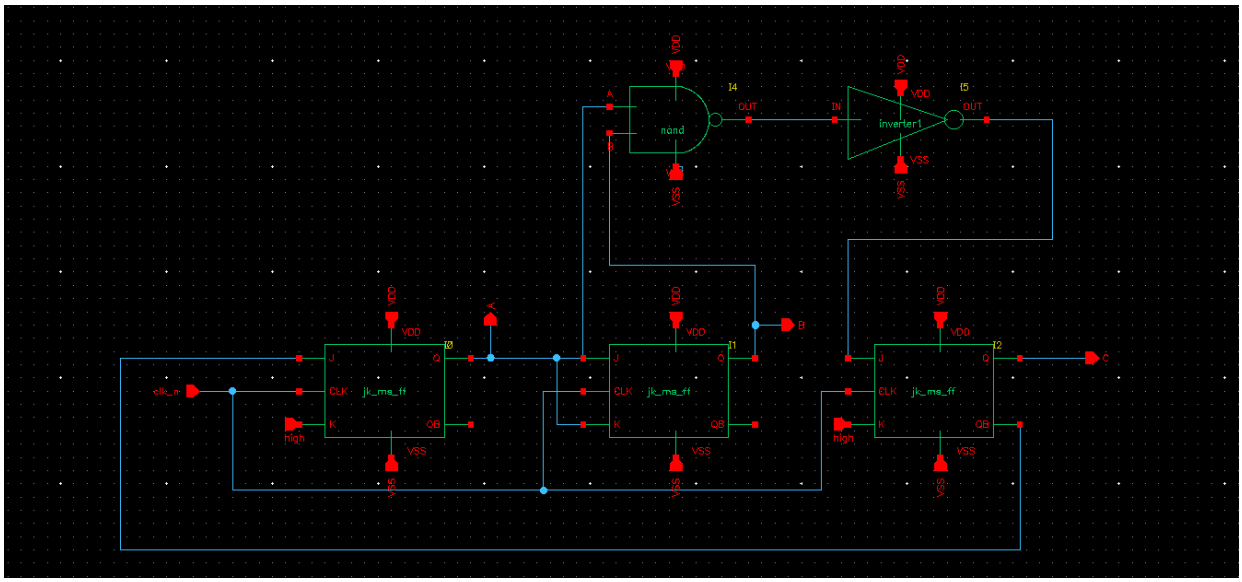
JK flip-flop Schematic:



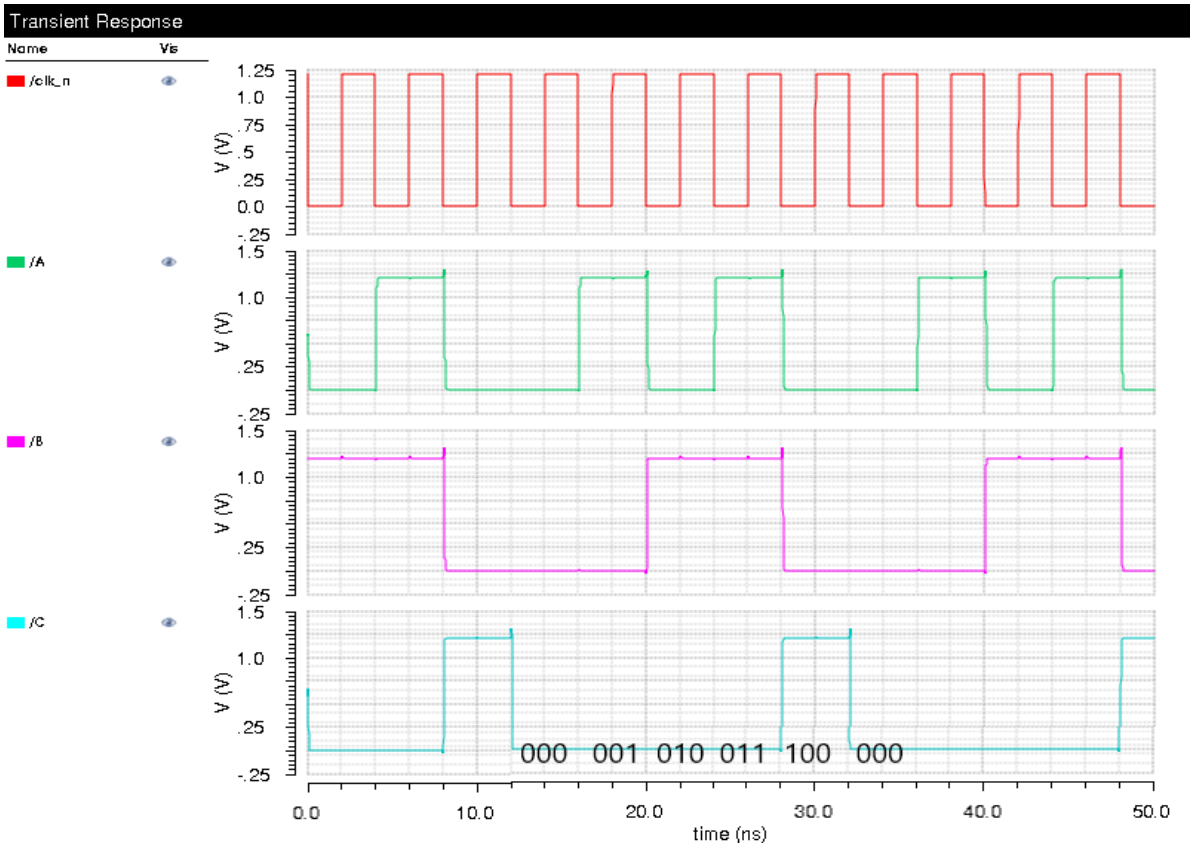
JK flip-flop Pre layout simulation:



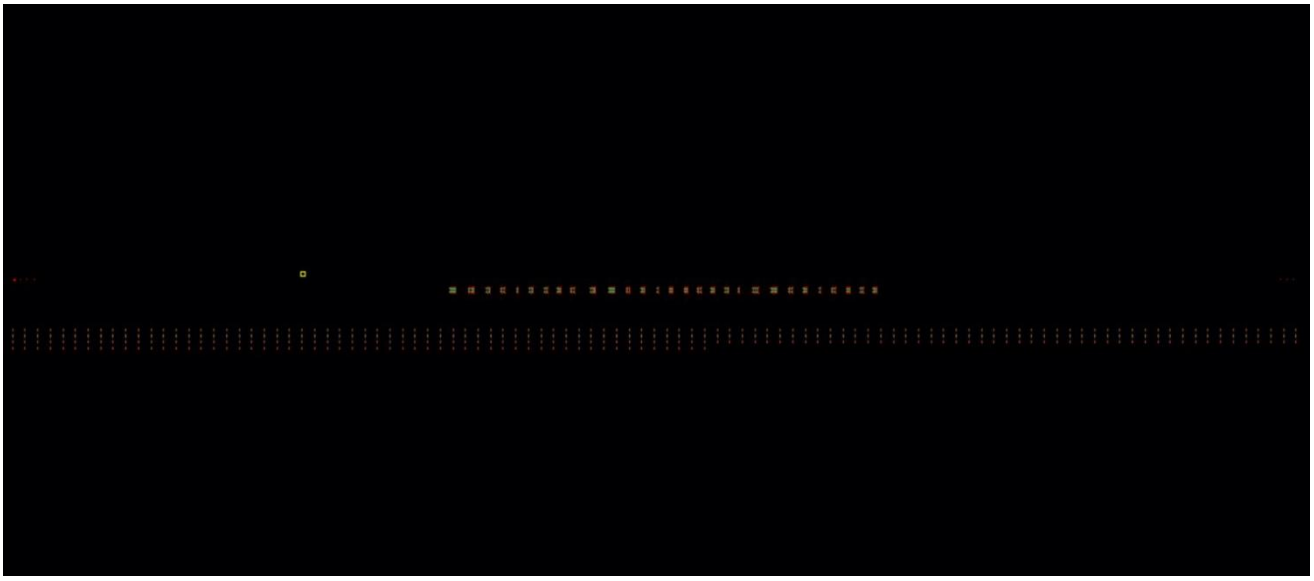
MOD-5 COUNTER Schematic:



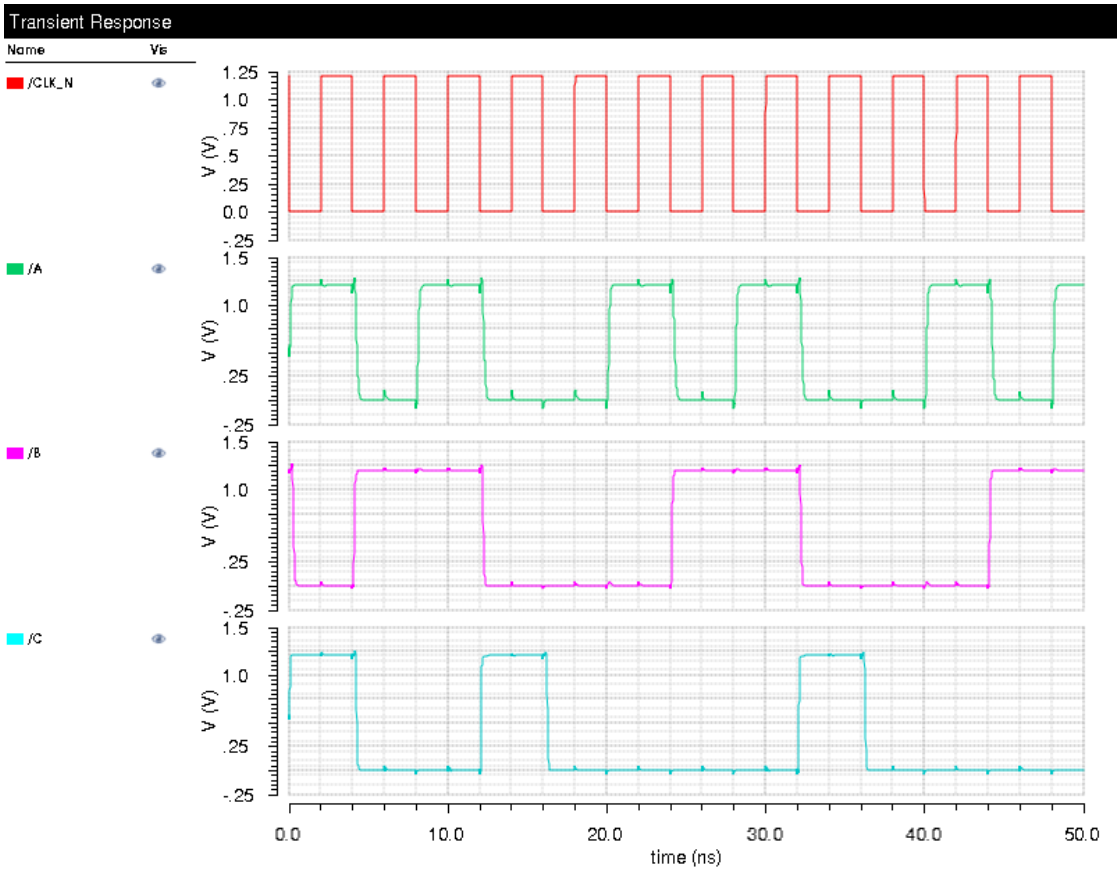
MOD-5 COUNTER Pre layout Simulation:



Mod 5 Counter Extracted Image



Mod 5 Counter Post layout simulation(at 250MHz)



Specification of a JK flip flop:

Delay (Clk to Q(high to low))=279ps

Setup time=97ps

Specification of Counter(at 250 Mhz)

For A

Rise time:153.28 ps;Fall time:216.20ps

For B

Rise time:95.83ps;Fall time:148.44 ps

For C

Rise time:68.25ps;Fall time:116.67ps

Delay time (From clk to output A):low to high=161.406ps; high to low=279.14ps

Delay time (From clk to output B): low to high=133.487ps; high to low=258.44ps

Delay time (From clk to output C): low to high=121.076 ps; high to low=245.32ps

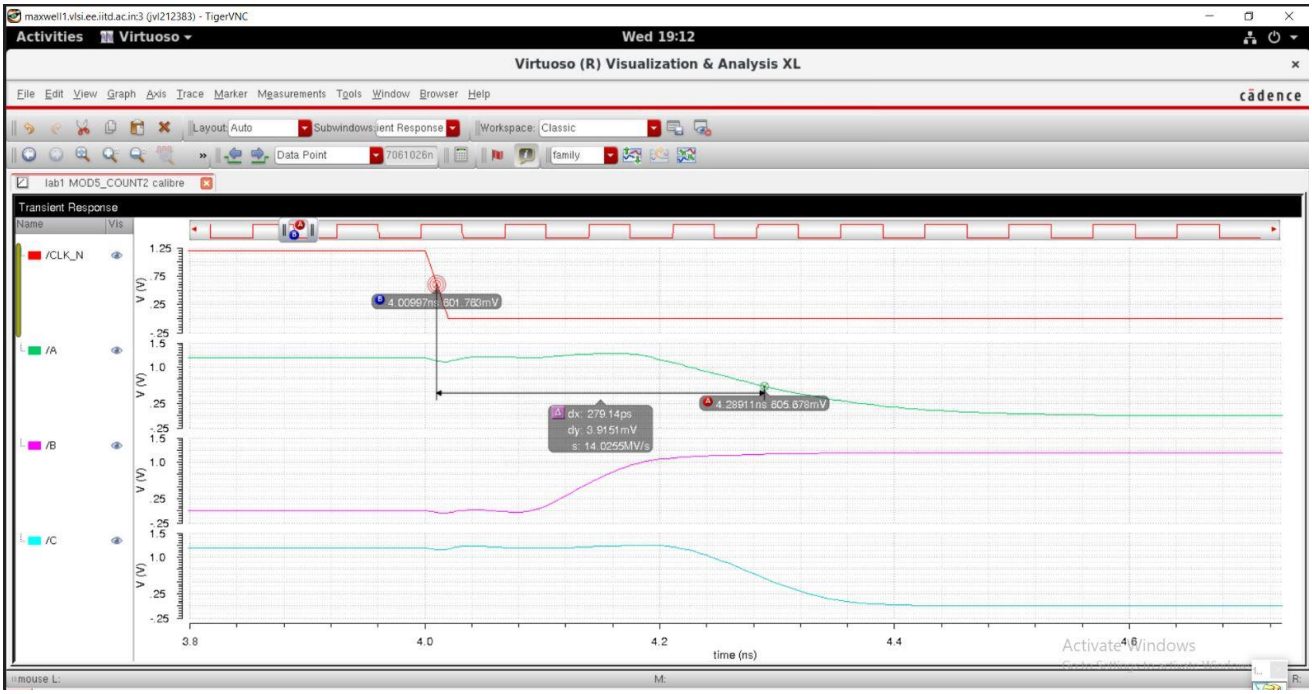
Maximum Frequency for mod 5 counter :

For maximum frequency we have to calculate the delays for the flip flops and then add the Clock to Q delay with the setup time of JK flip flop. This will give the min time period of the clock pulse. Then we get the maximum frequency.

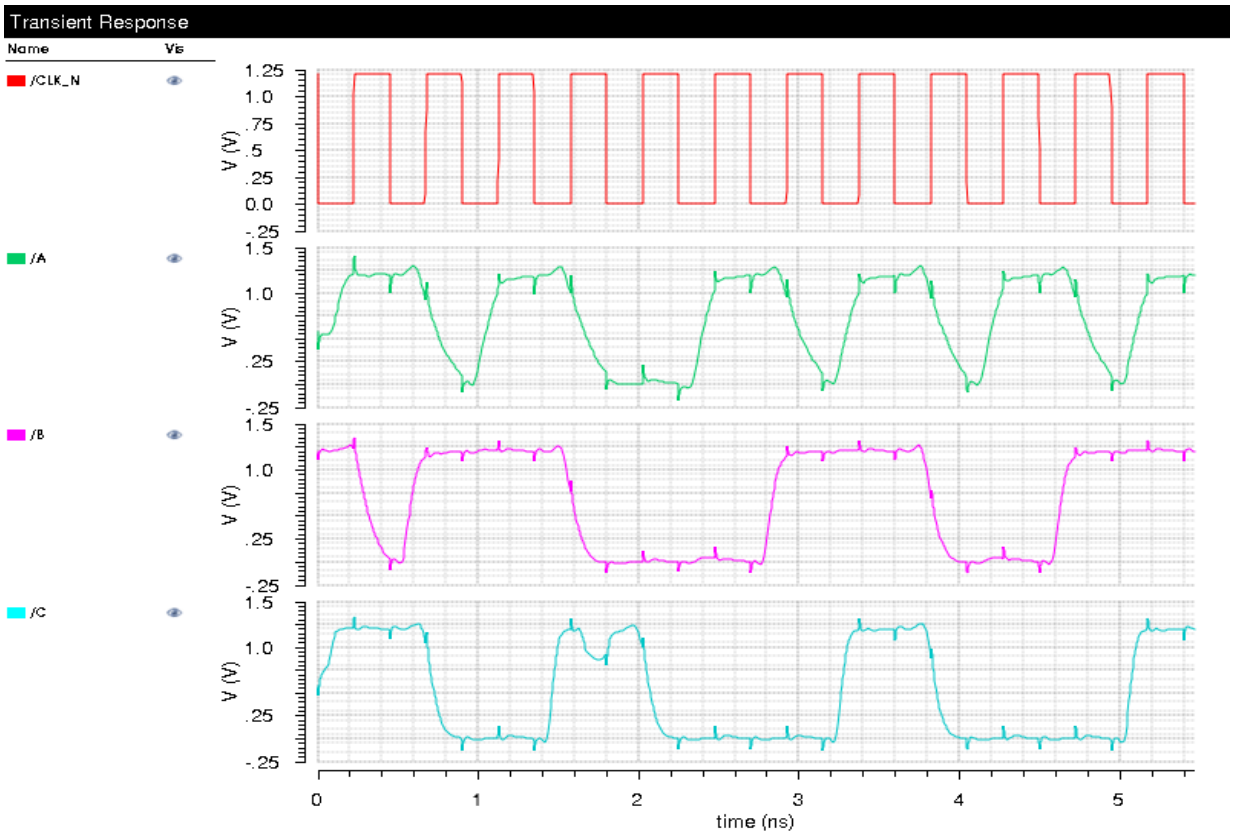
Min time period=Clock to Q delay + Setup time

Min time period=(279.14ps +97ps)=376.14ps

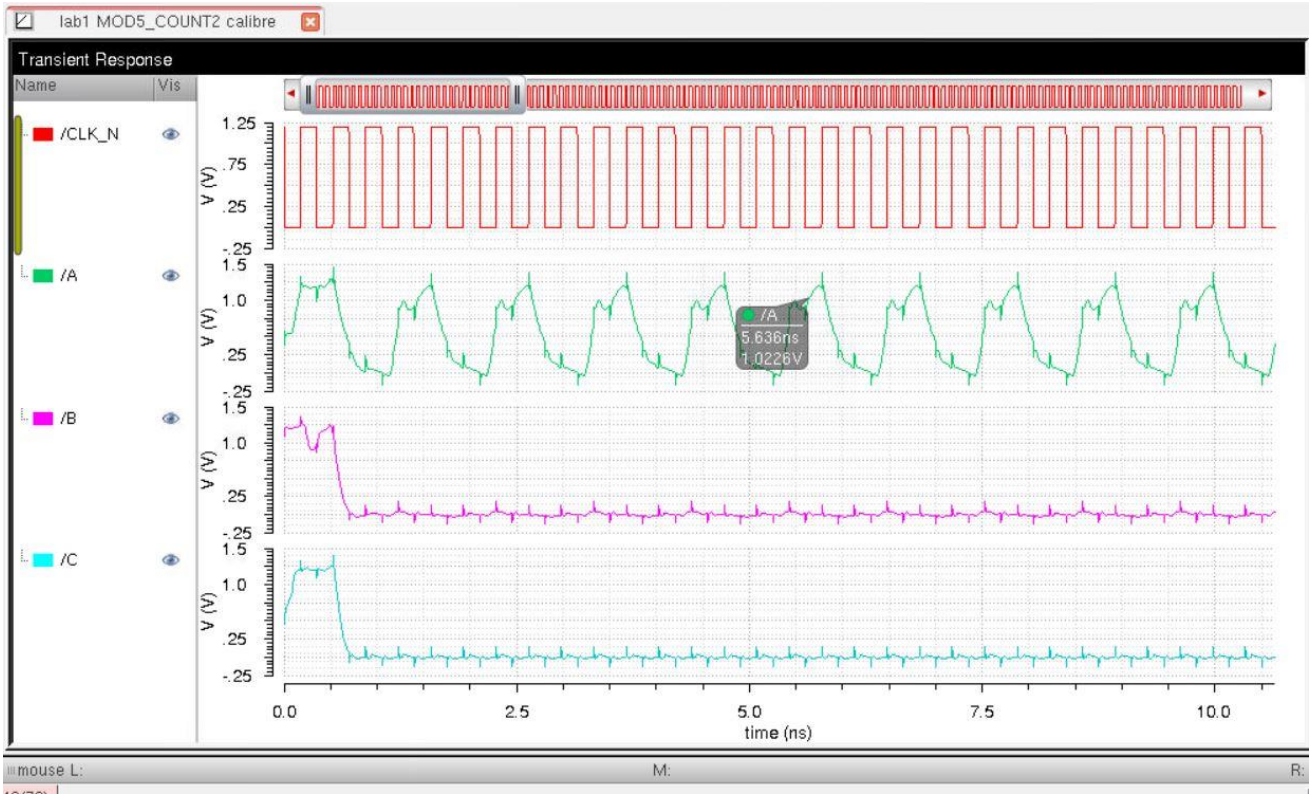
Max Frequency=2.65GHz



Simulation Output for T=0.450ns:



Simulation Output for T=0.350ns:



Here we can observe that the output is much distorted at t=350nsHz,So max frequency is below 3.125Hz.