TEXAS INSTRUMENTS

**SN54LVC138A, SN74LVC138A**

SCAS291W – MARCH 1993 – REVISED OCTOBER 2016

# SN74LVC138A 3-Line to 8-Line Decoders Demultiplexers

## 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 5.8 ns at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Latch-Up Performance Exceeds 250 mA Per JESD 17

## 2 Applications

- LED Displays
- Servers
- White Goods
- Power Infrastructure
- Building Automation
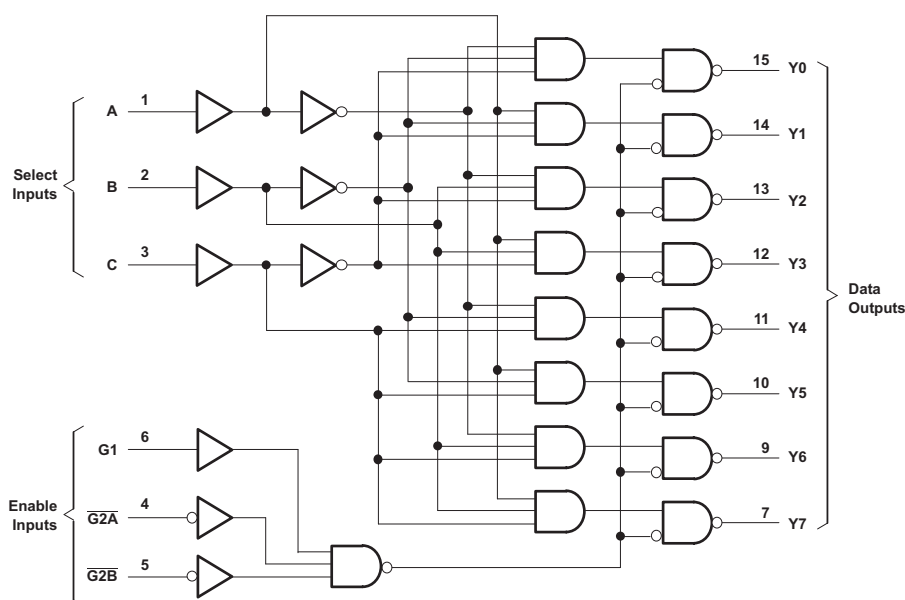- Factory Automation

## 3 Description

The SN74LVC138A devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders minimize the effects of system decoding. When employed with high-speed memories using a fast enable circuit, delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

**Device Information[1]**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SNx4LVC138A | LCCC (20) | 8.89 mm × 8.89 mm |
| | CDIP (16) | 19.56 mm × 6.92 mm |
| | CFP (16) | 10.30 mm × 6.73 mm |
| | SOIC (16) | 9.90 mm × 3.91 mm |
| | SSOP (16) | 6.20 mm × 5.30 mm |
| | TVSOP (16) | 3.60 mm × 4.40 mm |
| | BGA MICROSTAR JUNIOR (20) | 4.00 mm × 3.00 mm |
| | TSSOP (16) | 5.00 mm × 4.40 mm |
| | UQFN (16) | 2.60 mm × 1.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.
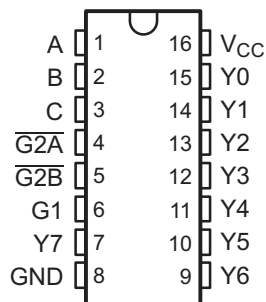
# Table of Contents

# 4   Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision V (November 2013) to Revision W**                                              **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .................................................................................................. 1
- Deleted *Ordering Information* table; see *Packaging Ordering Addendum* at the end of the data sheet................................ 1
- Changed $R_{\theta JA}$ values from: 73 to 86.8 (D), 82 to 100.1 (DB), 120 to 122.1 (DGV), 78 to 84 (ZQN), 108 to 108.9 (PW) ............................................................................................................................................................................ 6
- Deleted $R_{\theta JA}$ values for NS and RGY packages............................................................................................................. 6

**Changes from Revision U (OCTOBER 2012) to Revision V**                                              **Page**

- Updated document to new TI data sheet format - no specification changes. ........................................................................... 1
- Removed Ordering Information table ...................................................................................................................................... 1
- Added ESD warning .............................................................................................................................................................. 1

# 5 Pin Configuration and Functions

**SN54LVC138A . . . J OR W PACKAGE**
**SN74LVC138A . . . D, DB, DGV, NS,**
**OR PW PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| A | 1 | 16 $V_{CC}$ |
| B | 2 | 15 Y0 |
| C | 3 | 14 Y1 |
| $\overline{G2A}$ | 4 | 13 Y2 |
| $\overline{G2B}$ | 5 | 12 Y3 |
| G1 | 6 | 11 Y4 |
| Y7 | 7 | 10 Y5 |
| GND | 8 | 9 Y6 |

**SN74LVC138A . . . RGY  PACKAGE**
**(TOP VIEW)**

A   $V_{CC}$

| | | |
|---|---|---|
| | 1 | 16 |
| B | 2 | 15 Y0 |
| C | 3 | 14 Y1 |
| $\overline{G2A}$ | 4 | 13 Y2 |
| $\overline{G2B}$ | 5 | 12 Y3 |
| G1 | 6 | 11 Y4 |
| Y7 | 7 | 10 Y5 |
| | 8 | 9 |

GND   Y6
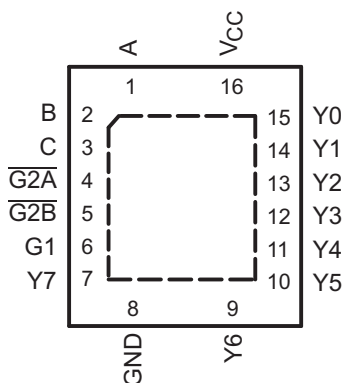
**SN54LVC138A . . . FK PACKAGE**
**(TOP VIEW)**

B   A   NC   $V_{CC}$   Y0
3   2   1   20   19

| | | |
|---|---|---|
| C | 4 | 18 Y1 |
| $\overline{G2A}$ | 5 | 17 Y2 |
| NC | 6 | 16 NC |
| $\overline{G2B}$ | 7 | 15 Y3 |
| G1 | 8 | 14 Y4 |

9   10   11   12   13
Y7   GND   NC   Y6   Y5
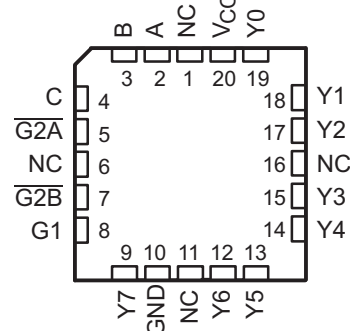
NC - No internal connection

**SN54LVC138A...RSV PACKAGE**
**(TOP VIEW)**

Y3   Y4   Y5   Y6
12   11   10   9

| | | | |
|---|---|---|---|
| Y2 | 13 | | 8 GND |
| Y1 | 14 | | 7 Y7 |
| Y0 | 15 | | 6 G1 |
| $V_{CC}$ | 16 | | 5 $\overline{G2B}$ |
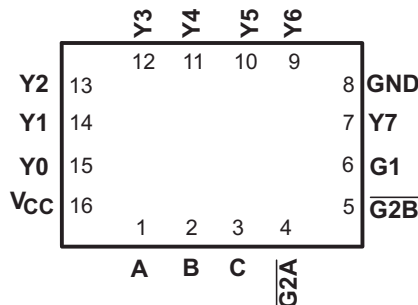
1   2   3   4
A   B   C   $\overline{G2A}$

**GQN OR ZQN PACKAGE**
**(TOP VIEW)**

1   2   3   4

A
B
C
D
E
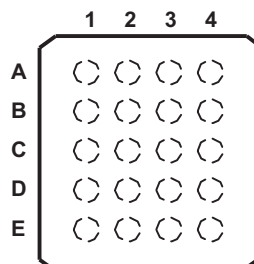
## Table 1. Pin Assignments for ZQN (BGA)

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| **A** | B | A | $V_{CC}$ | Y0 |
| **B** | C | NC[1] | NC[1] | Y1 |
| **C** | $\overline{G2B}$ | $\overline{G2A}$ | Y3 | Y2 |
| **D** | G1 | NC[1] | NC[1] | Y4 |
| **E** | GND | Y7 | Y6 | Y5 |

(1)   NC - No internal connection

Product Folder Links: *SN54LVC138A   SN74LVC138A*

## Pin Functions

| PIN | | | | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, TVSOP, SO, TSSOP, VQFN, UQFN | LCCC | BGA MICROSTAR JUNIOR | I/O | |
| A | 1 | 2 | A2 | I | Select input A (least significant bit) |
| B | 2 | 3 | A1 | I | Select input B |
| C | 3 | 4 | B1 | I | Select input C (most significant bit) |
| $\overline{G2A}$ | 4 | 5 | C2 | I | Active low enable A |
| $\overline{G2B}$ | 5 | 7 | C1 | I | Active low enable B |
| G1 | 6 | 8 | D1 | I | Active high enable |
| GND | 8 | 10 | E1 | — | Ground |
| NC | — | 1, 11, 16 | B2, B3, D2, D3 | — | No internal connection |
| $V_{CC}$ | 16 | 20 | A3 | — | Supply voltage |
| Y0 | 15 | 19 | A4 | O | Output 0 (least significant bit) |
| Y1 | 14 | 18 | B4 | O | Output 1 |
| Y2 | 13 | 17 | C4 | O | Output 2 |
| Y3 | 12 | 15 | C3 | O | Output 3 |
| Y4 | 11 | 14 | D4 | O | Output 4 |
| Y5 | 10 | 13 | E4 | O | Output 5 |
| Y6 | 9 | 12 | E3 | O | Output 6 |
| Y7 | 7 | 9 | E2 | O | Output 7 (most significant bit) |

Note: The I/O column header spans the PIN grouping; the first three NAME, SOIC/SSOP..., LCCC, BGA MICROSTAR JUNIOR columns are under "PIN".

Product Folder Links: *SN54LVC138A  SN74LVC138A*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.5 | 6.5 | V |
| $V_I$ | Input voltage[2] | | −0.5 | 6.5 | V |
| $V_O$ | Output voltage[2][3] | | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | −50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | −50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the recommended operating conditions table.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | 1000 | |
| | | Machine model (MM) | 200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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Product Folder Links: *SN54LVC138A  SN74LVC138A*

## 6.3 Recommended Operating Conditions

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | SN54LVC138A[1] | 2 | 3.6 | V |
| | | | SN74LVC138A[1] | 1.65 | 3.6 | |
| | | Data retention only | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | SN74LVC138A[1] | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | SN74LVC138A[1] | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | SN74LVC138A[1] | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | SN74LVC138A[1] | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | | 0.8 | |
| $V_I$ | Input voltage | | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | SN74LVC138A[1] | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | SN74LVC138A[1] | | −8 | |
| | | $V_{CC}$ = 2.7 V | | | −12 | |
| | | $V_{CC}$ = 3 V | | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | SN74LVC138A[1] | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | SN74LVC138A[1] | | 8 | |
| | | $V_{CC}$ = 2.7 V | | | 12 | |
| | | $V_{CC}$ = 3 V | | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | SN54LVC138A[1] | | −55 | 125 | °C |
| | | SN74LVC138A[1] | | −40 | 85 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

## 6.4 Thermal Information

| | THERMAL METRIC[1] | SNx4LVC138A | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | FK (LCCC) | J (CDIP) | W (CFP) | D (SOIC) | DB (SSOP) | DGV (TVSOP) | ZQN (BGA MICROSTAR JUNIOR) | PW (TSSOP) | RSV (UQFN) | |
| | | 20 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 20 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 79.2 | 85.8 | 138.0 | 86.8 | 100.1 | 122.1 | 84 | 108.9 | 168.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.5 | 49.3 | 74.6 | 47.9 | 50.6 | 47.4 | 56.9 | 42.5 | 78.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 55.2 | 64.9 | 127.7 | 43.8 | 50.7 | 53.8 | 46.1 | 54.5 | 96.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 49.8 | 37.4 | 50 | 15.7 | 14.3 | 4.6 | 3 | 4.4 | 4.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 55.0 | 69.5 | 115.7 | 43.5 | 50.1 | 53.2 | 48.9 | 53.8 | 96.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Product Folder Links: *SN54LVC138A   SN74LVC138A*

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = −100 μA | SN74LVC138A | 1.65 V to 3.6 V | $V_{CC}$ − 0.2 | | | V |
| | | | SN54LVC138A | 2.7 V to 3.6 V | $V_{CC}$ − 0.2 | | | |
| | | $I_{OH}$ = −4 mA | SN74LVC138A | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = −8 mA | SN74LVC138A | 2.3 V | 1.7 | | | |
| | | $I_{OH}$ = −12 mA | | 2.7 V | 2.2 | | | |
| | | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = −24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 100 μA | SN74LVC138A | 1.65 V to 3.6 V | | | 0.2 | V |
| | | | SN54LVC138A | 2.7 V to 3.6 V | | | 0.2 | |
| | | $I_{OL}$ = 4 mA | SN74LVC138A | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | SN74LVC138A | 2.3 V | | | 0.7 | |
| | | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | Input current | $V_I$ = 5.5 V or GND | | 3.6 V | | | ±5 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | | 3.6 V | | | 10 | μA |
| $\Delta I_{CC}$ | Change in supply current | One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | μA |
| $C_i$ | Input capacitance | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics—SN54LVC138A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation (delay) time | A or B or C | Y | $V_{CC}$ = 2.7 V | | 7.9 | ns |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.7 | |
| | | $\overline{G2A}$ or $\overline{G2B}$ | | $V_{CC}$ = 2.7 V | | 7.4 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.5 | |
| | | G1 | | $V_{CC}$ = 2.7 V | | 6.4 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.8 | |

## 6.7 Switching Characteristics—SN74LVC138A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation (delay) time | A or B or C | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 1 | 22 | ns |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 9.9 | |
| | | | | $V_{CC}$ = 2.7 V | 1 | 7.9 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.7 | |
| | | $\overline{G2A}$ or $\overline{G2B}$ | | $V_{CC}$ = 1.8 V ± 0.15 V | 1 | 21 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 9.4 | |
| | | | | $V_{CC}$ = 2.7 V | 1 | 7.4 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 6.5 | |
| | | G1 | | $V_{CC}$ = 1.8 V ± 0.15 V | 1 | 20.3 | |
| | | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 8.4 | |
| | | | | $V_{CC}$ = 2.7 V | 1 | 6.4 | |
| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1 | 5.8 | |
| $t_{sk(o)}$ | Skew (time), output | — | — | $V_{CC}$ = 3.3 V ± 0.3 V | | 1 | ns |

## 6.8 Operating Characteristics

$T_A = 25°C$

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | $V_{CC}$ = 1.8 V | 25 | pF |
| | | | $V_{CC}$ = 2.5 V | 26 | |
| | | | $V_{CC}$ = 3.3 V | 27 | |

## 6.9 Typical Characteristics
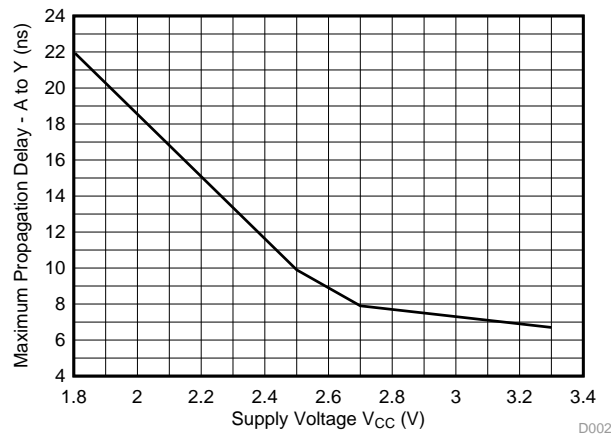


Figure 1. Maximum Propagation Delay vs Supply Voltage

Product Folder Links: *SN54LVC138A   SN74LVC138A*

# 7 Parameter Measurement Information
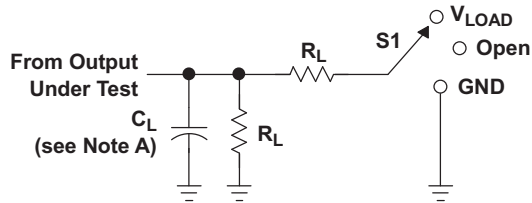


**LOAD CIRCUIT**

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

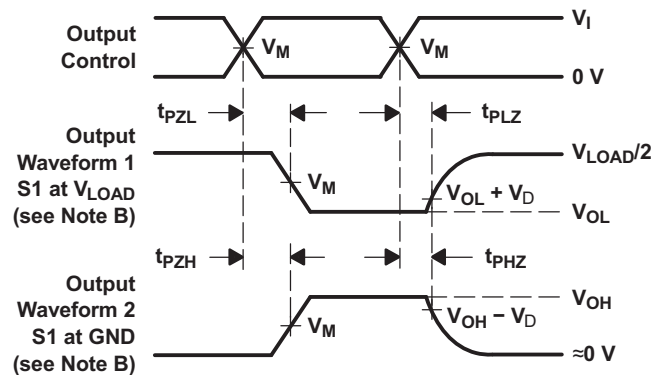| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_D$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
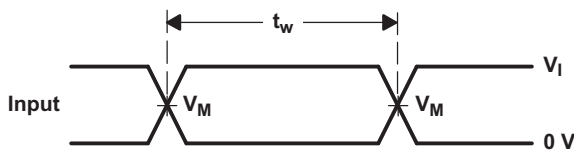


**VOLTAGE WAVEFORMS**
**PULSE DURATION**
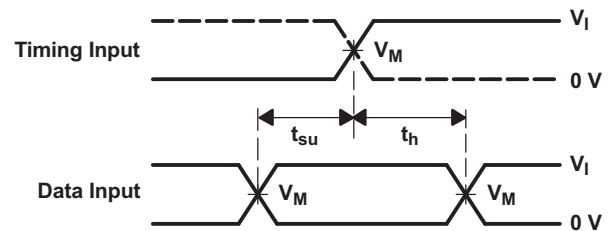


**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
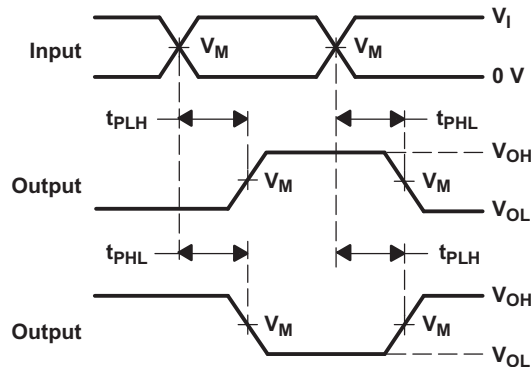


**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

Product Folder Links: *SN54LVC138A  SN74LVC138A*

# 8 Detailed Description

## 8.1 Overview

The SNx4LVC138A devices are 3-to-8 decoders and demultiplexers. The three input pins, A, B, and C, select which output is active. The selected output is pulled LOW, while the remaining outputs are all HIGH. The conditions at the binary-select inputs at the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the requirement for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

## 8.2 Functional Block Diagram
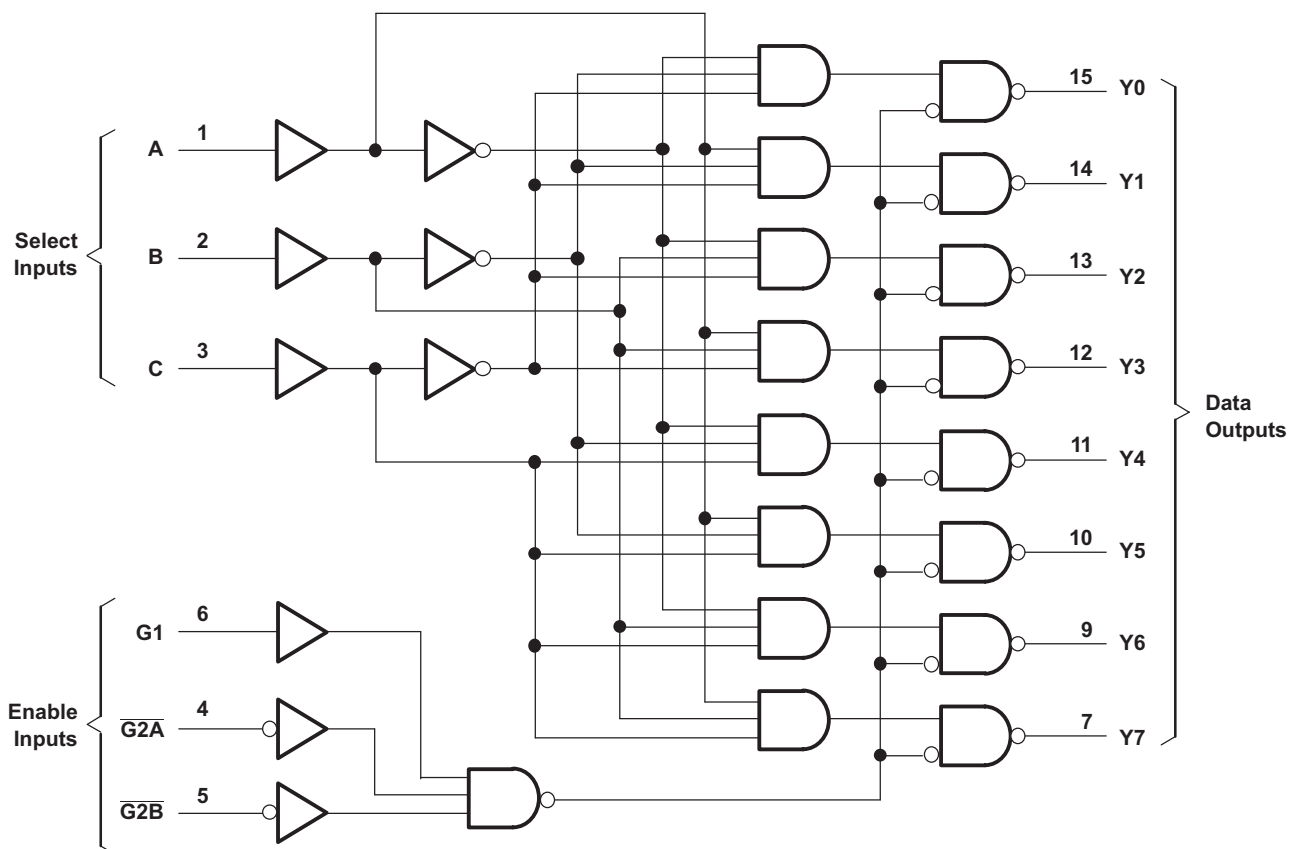


Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

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## 8.3 Feature Description

### 8.3.1 3-Line to 8-Line Decoder

This device features three binary inputs to select a single active-low output. Three enable pins are also available to enable or disable the outputs. One active high enable and two active low enable pins are available, and any enable pin can be deactivated to force all outputs high. All three enable pins must be active for the output to be enabled.

## Feature Description (continued)

### 8.3.2   1.65-V to 3.6-V Operation With Inputs up to 5.5 V

The SN54LVC138A 3-line to 8-line decoder demultiplexer is designed for 2.7-V to 3.6-V $V_{CC}$ operation, and the SN74LVC138A 3-line to 8-line decoder demultiplexer is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V and 5-V system environment.

### 8.4   Device Functional Modes

Table 2 lists the outputs of the SNx4LVC138A devices based on the possible input configurations.

**Table 2.  Function Table**

| ENABLE INPUTS | | | SELECT INPUTS | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | $\overline{G2A}$ | $\overline{G2B}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

# 9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC138A is useful as a scanning column selector for an LED Matrix display as it can be used for the low-side drive of the LED string. The decoder functionality ensures that no more than one output is pulled to a low-level logic voltage so that only a single column is enabled at any point in time.
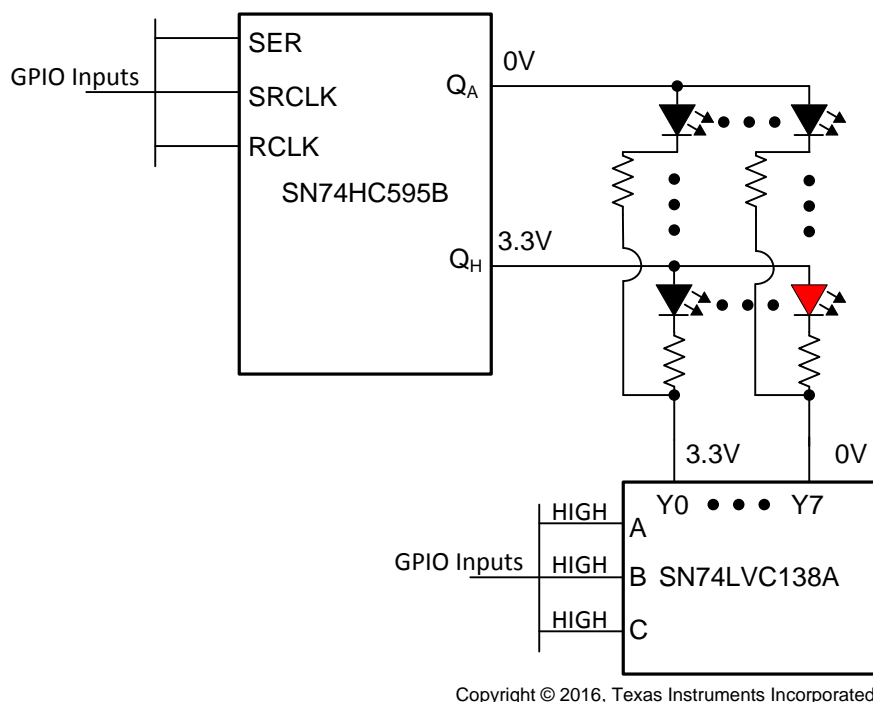
## 9.2 Typical Application



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**Figure 3. LED Matrix Driver Application**

### 9.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – For switch time specifications, see propagation delay times in *Switching Characteristics—SN74LVC138A*.
   – For input voltage level specifications for control inputs, see $V_{IH}$ and $V_{IL}$ in *Recommended Operating Conditions*.
2. Recommended Output Conditions
   – Outputs must not be pulled above $V_{CC}$ or below GND.

## Typical Application (continued)
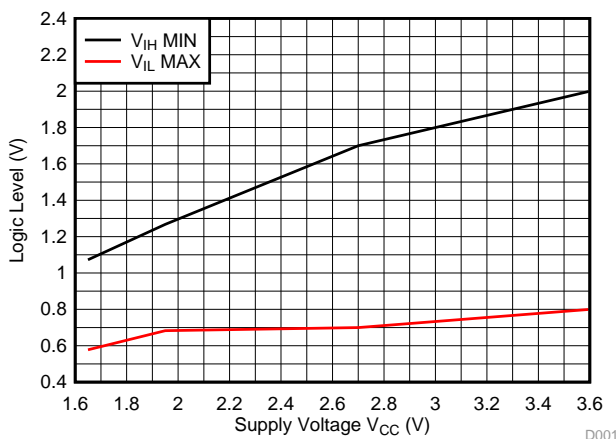
### 9.2.3 Application Curve



**Figure 4. Input High and Input Low Thresholds vs Supply Voltage**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each $V_{CC}$ terminal must have a good bypass capacitor to prevent power disturbance. A 0.1-µF bypass capacitor is recommended to be placed close to the $V_{CC}$ terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise; 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace (resulting in the reflection). It is a given that not all PCB traces can be straight, and so they have to turn corners. Figure 5 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.
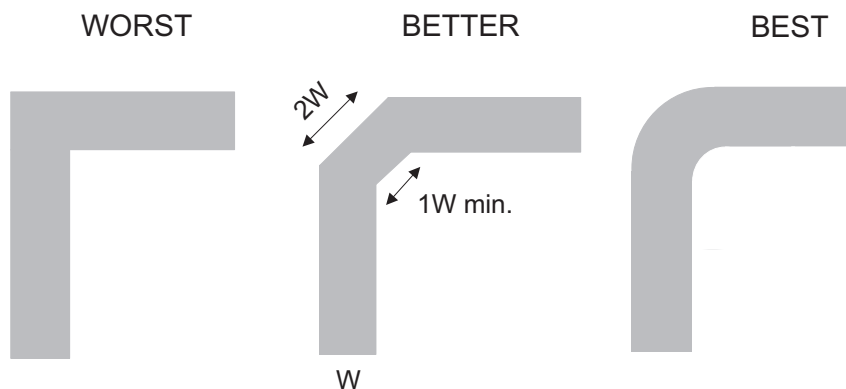
### 11.2 Layout Example



**Figure 5.  Trace Example**

Product Folder Links: *SN54LVC138A  SN74LVC138A*

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LVC138A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC138A | Click here | Click here | Click here | Click here | Click here |

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9752601Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9752601Q2A SNJ54LVC 138AFK | Samples |
| 5962-9752601QEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9752601QE A SNJ54LVC138AJ | Samples |
| 5962-9752601QFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9752601QF A SNJ54LVC138AW | Samples |
| 5962-9752601VFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9752601VF A SNV54LVC138AW | Samples |
| SN74LVC138AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ADBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ADT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC138A | Samples |
| SN74LVC138APW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC138APWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138APWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138APWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138APWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SN74LVC138ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LC138A | Samples |
| SN74LVC138ARGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LC138A | Samples |
| SN74LVC138ARSVR | ACTIVE | UQFN | RSV | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZTP | Samples |
| SN74LVC138AZQNR | ACTIVE | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LC138A | Samples |
| SNJ54LVC138AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9752601Q2A SNJ54LVC 138AFK | Samples |
| SNJ54LVC138AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9752601QE A SNJ54LVC138AJ | Samples |
| SNJ54LVC138AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9752601QF A SNJ54LVC138AW | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC138A, SN54LVC138A-SP, SN74LVC138A :**

- Catalog: SN74LVC138A, SN54LVC138A

- Automotive: SN74LVC138A-Q1, SN74LVC138A-Q1

- Enhanced Product: SN74LVC138A-EP, SN74LVC138A-EP

- Military: SN54LVC138A

- Space: SN54LVC138A-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC138ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC138ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC138APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC138APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC138APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC138APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC138ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN74LVC138AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| SN74LVC138ADGVR | TVSOP | DGV | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC138ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LVC138APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC138APWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC138APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC138APWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| SN74LVC138ARGYR | VQFN | RGY | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| SN74LVC138AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 350.0 | 350.0 | 43.0 |

W (R−GDFP−F16)                                    CERAMIC DUAL FLATPACK

Base and Seating Plane

0.285 (7,24)
0.245 (6,22)

0.045 (1,14)
0.026 (0,66)

0.008 (0,20)
0.004 (0,10)

0.080 (2,03)
0.055 (1,40)

0.305 (7,75) MAX

1                    16

0.019 (0,48)
0.015 (0,38)

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8                    9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−3/F   04/14

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  This package can be hermetically sealed with a ceramic lid using glass frit.
        D.  Index point is provided on cap for terminal identification only.
        E.  Falls within MIL STD 1835 GDFP2−F16

TEXAS
INSTRUMENTS
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J (R—GDIP—T**)                    CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

0.065 (1,65)
0.045 (1,14)

C

1                    7

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  This package is hermetically sealed with a ceramic lid using glass frit.
          D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.  Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

FK (S−CQCC−N**)                    LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN



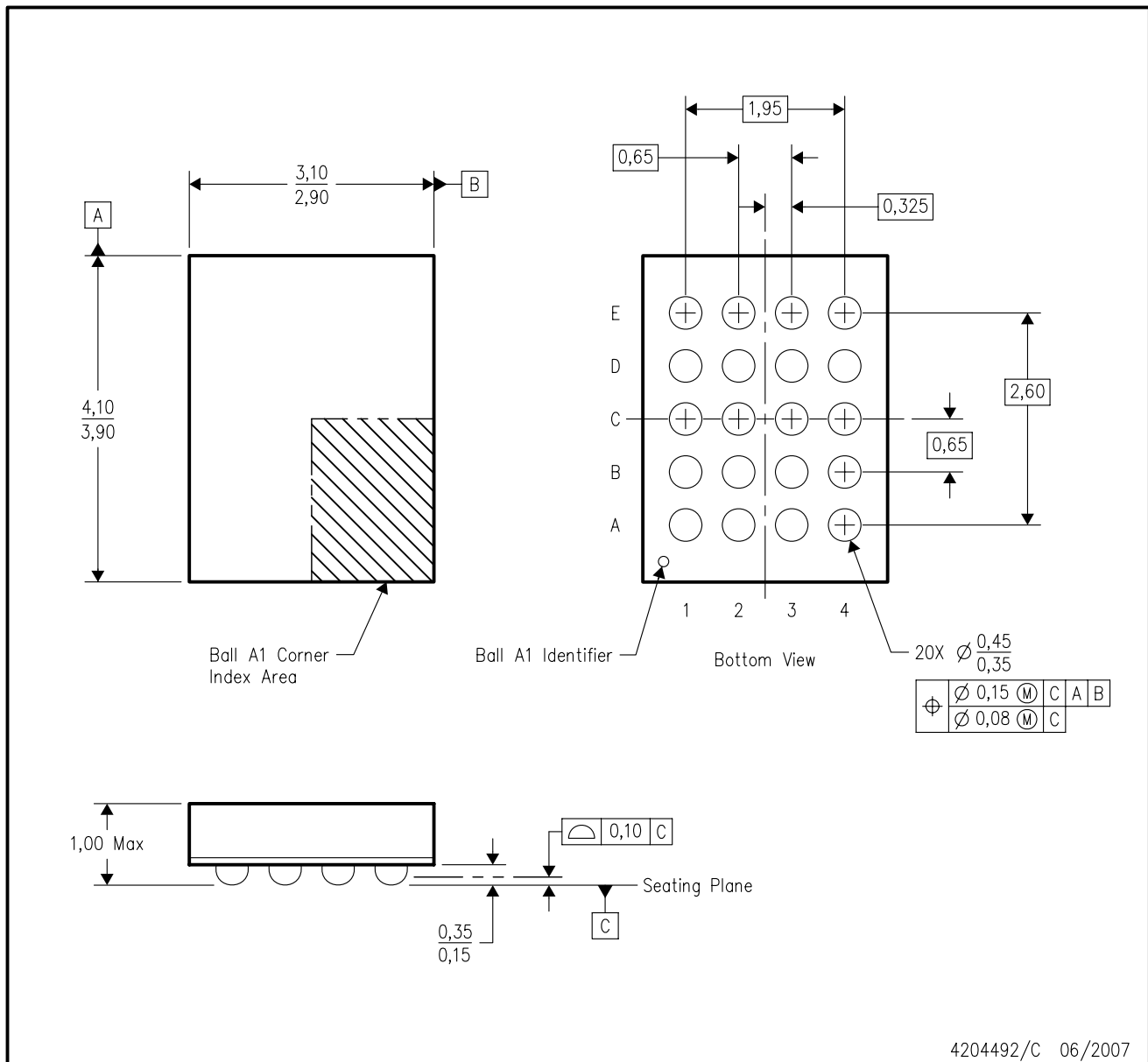| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

4040140/D 01/11

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS−004

TEXAS INSTRUMENTS
www.ti.com

## ZQN (R−PBGA−N20)　　　　　　　　　PLASTIC BALL GRID ARRAY

Ball A1 Corner
Index Area

Ball A1 Identifier

Bottom View

20X ∅ $\frac{0,45}{0,35}$

| ⊕ | ∅ 0,15 Ⓜ | C | A | B |
|---|---|---|---|---|
|   | ∅ 0,08 Ⓜ | C |   |   |

1,00 Max

Seating Plane

$\frac{0,35}{0,15}$

⌒ 0,10 C

C

4204492/C　06/2007

NOTES:　A.　All linear dimensions are in millimeters.　Dimensioning and tolerancing per ASME Y14.5M−1994.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Falls within JEDEC MO−285 variation BC−2.
　　　　　D.　This package is lead−free.　Refer to the 20 GQN package (drawing 4200704) for tin−lead (SnPb).

**DGV (R-PDSO-G\*\*)**                                          **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**



| PINS \*\*<br>DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A  MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A  MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

4073251/E 08/00

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
         D.   Falls within JEDEC:  24/48 Pins – MO-153
                                   14/16/20/56 Pins – MO-194

**TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

D (R−PDSO−G16)                                   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⟨C⟩

16                                              9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  ⟨D⟩

1                                               8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)       0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         ⟨D⟩ Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.  Reference JEDEC MS−012 variation AC.

**TEXAS INSTRUMENTS**
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D (R−PDSO−G16)                              PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
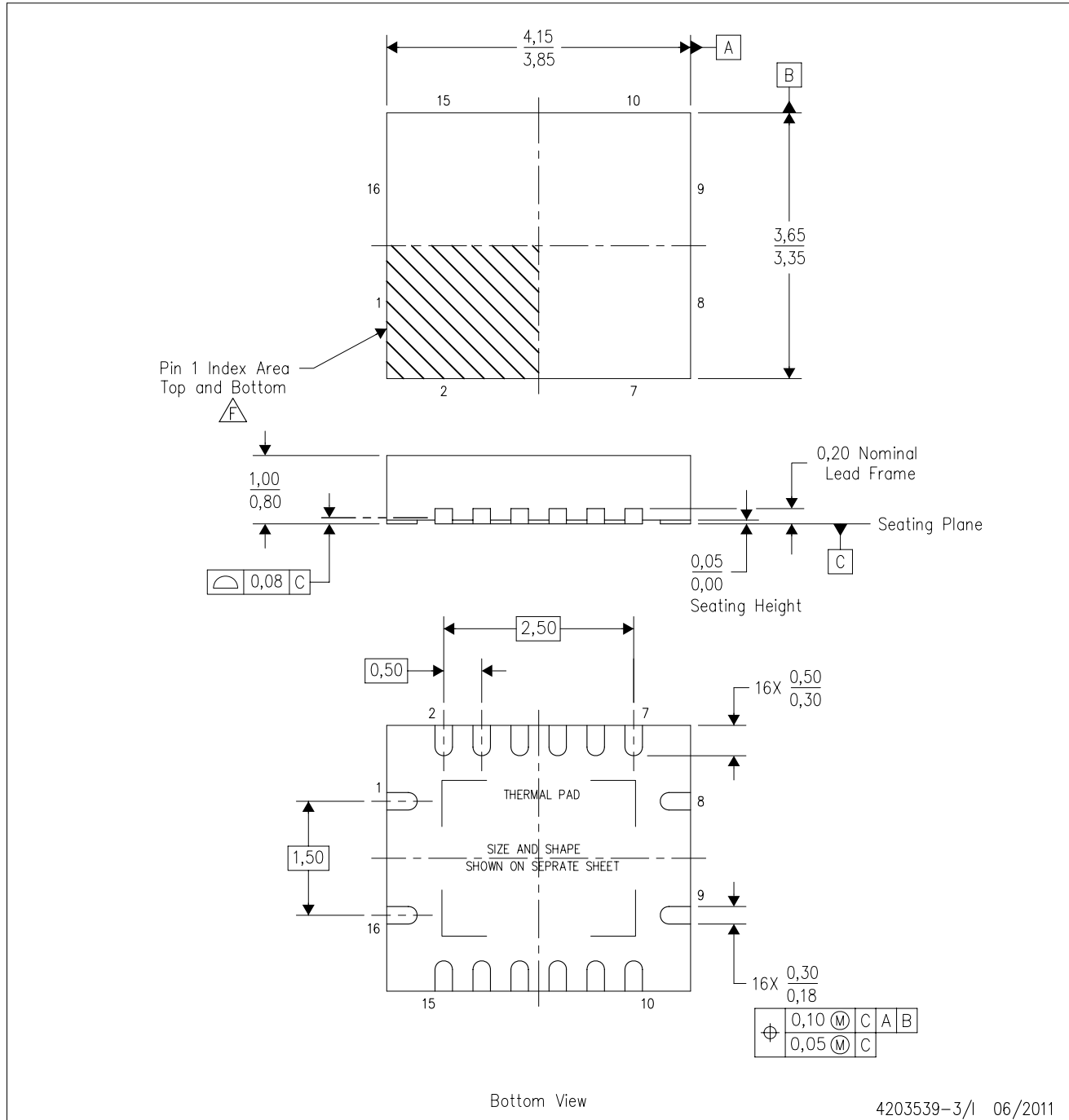Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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A

6.6
6.2 TYP

PIN 1 INDEX AREA

14X 0.65

16

1

2X
4.55

5.1
4.9
NOTE 3

8

9

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING PLANE

C

◁ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL
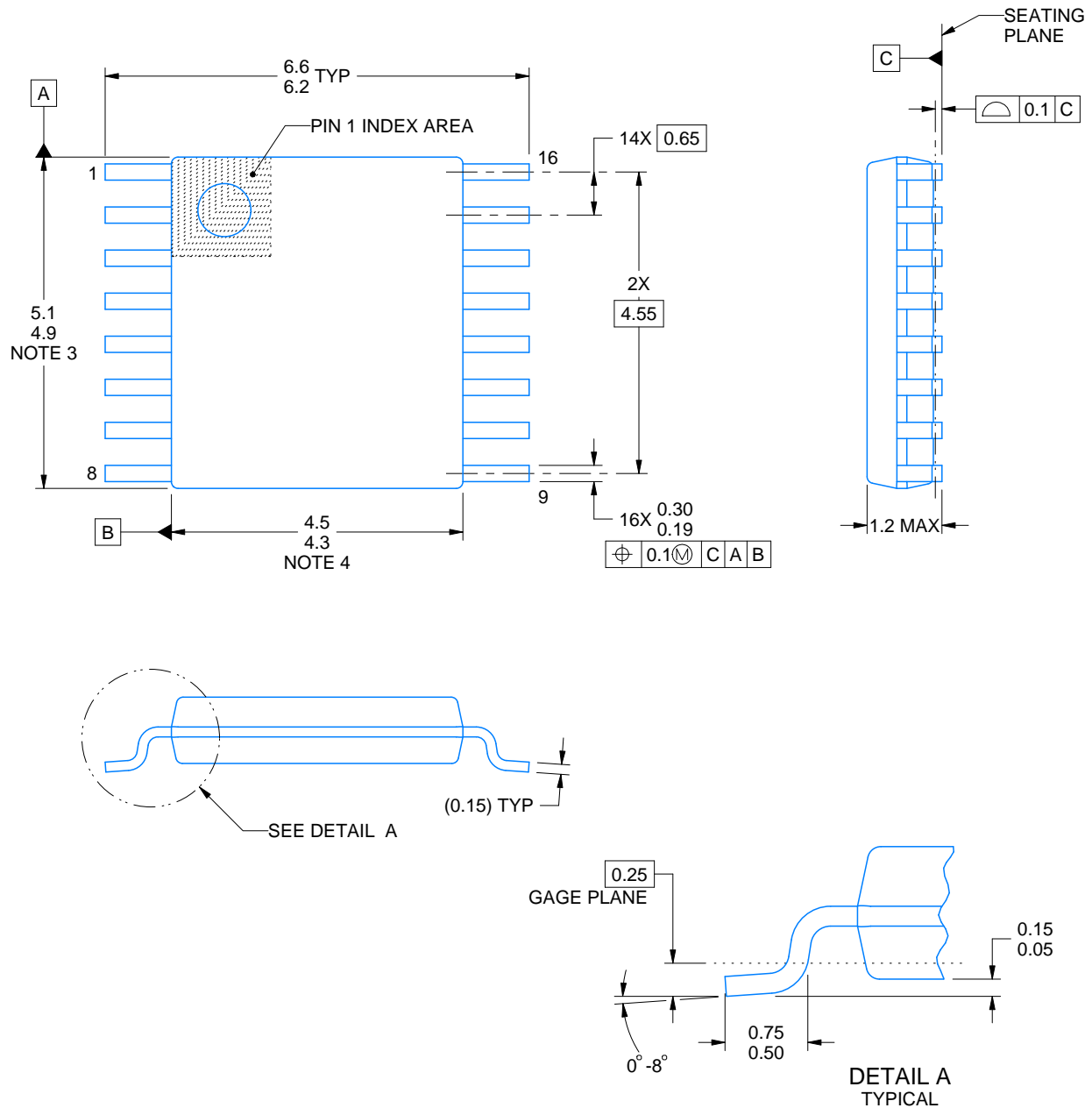
4220204/A  02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)
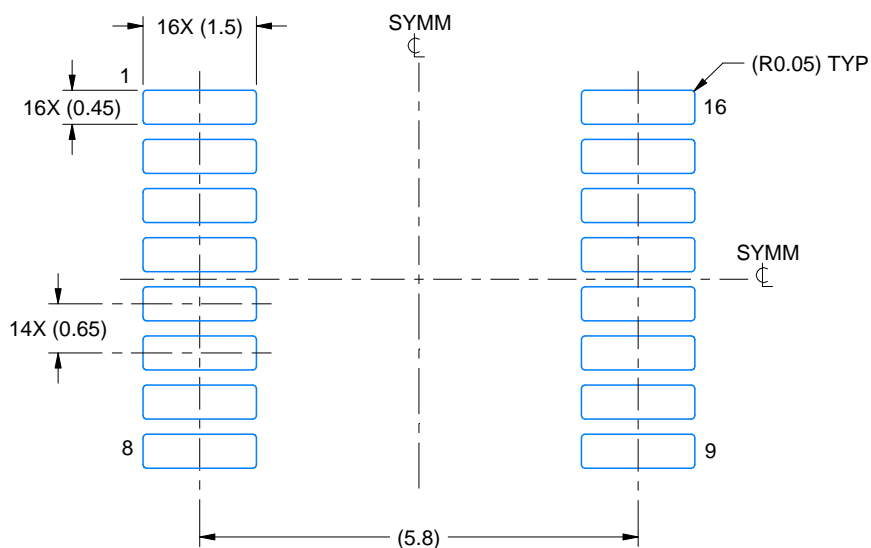
**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

**SOLDER MASK DETAILS**
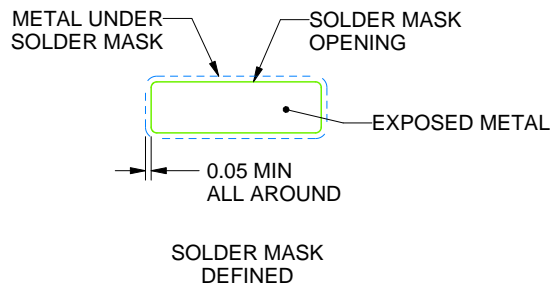
SOLDER MASK
DEFINED

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**DB (R-PDSO-G\*\*)**                                                            **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



| PINS \*\*<br>DIM | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A  MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A  MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES:   A.   All linear dimensions are in millimeters.
             B.   This drawing is subject to change without notice.
             C.   Body dimensions do not include mold flash or protrusion not to exceed 0,15.
             D.   Falls within JEDEC MO-150

RGY (R−PVQFN−N16)                    PLASTIC QUAD FLATPACK NO−LEAD

$\frac{4,15}{3,85}$  [A]

[B]

15          10

16                    9

8

$\frac{3,65}{3,35}$

Pin 1 Index Area
Top and Bottom

1

2          7

⬡F

$\frac{1,00}{0,80}$

0,20 Nominal
Lead Frame

Seating Plane

[⌒ | 0,08 | C]

$\frac{0,05}{0,00}$
Seating Height

[C]

2,50

0,50

2          7

16X $\frac{0,50}{0,30}$

1                    8

THERMAL PAD

1,50

SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

16                    9

15          10

16X $\frac{0,30}{0,18}$

| ⊕ | 0,10 Ⓜ | C | A | B |
| | 0,05 Ⓜ | C | | |

Bottom View

4203539−3/I   06/2011

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No−Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
    ⬡F   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
         The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO−241 variation BA.

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RGY (R−PVQFN−N16)                    PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad

2,05±0,10

2,55±0,10
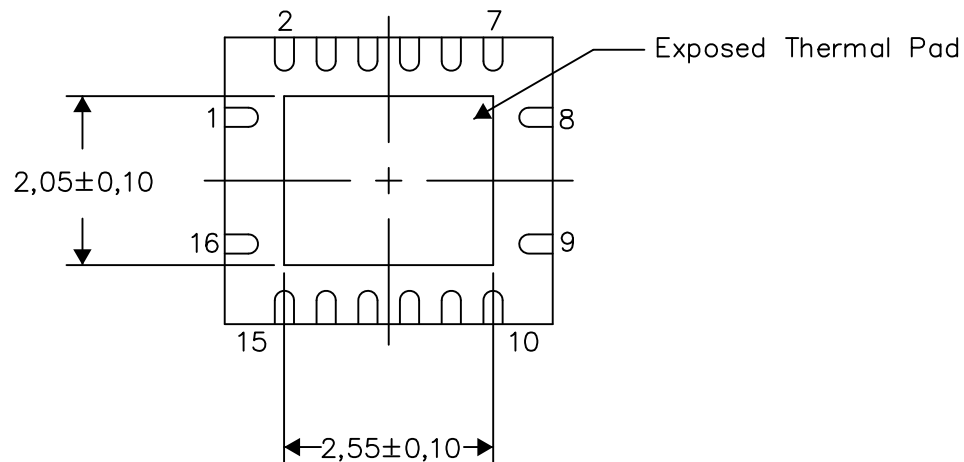
Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE:   All linear dimensions are in millimeters

RGY (R−PVQFN−N16)          PLASTIC QUAD FLATPACK NO−LEAD
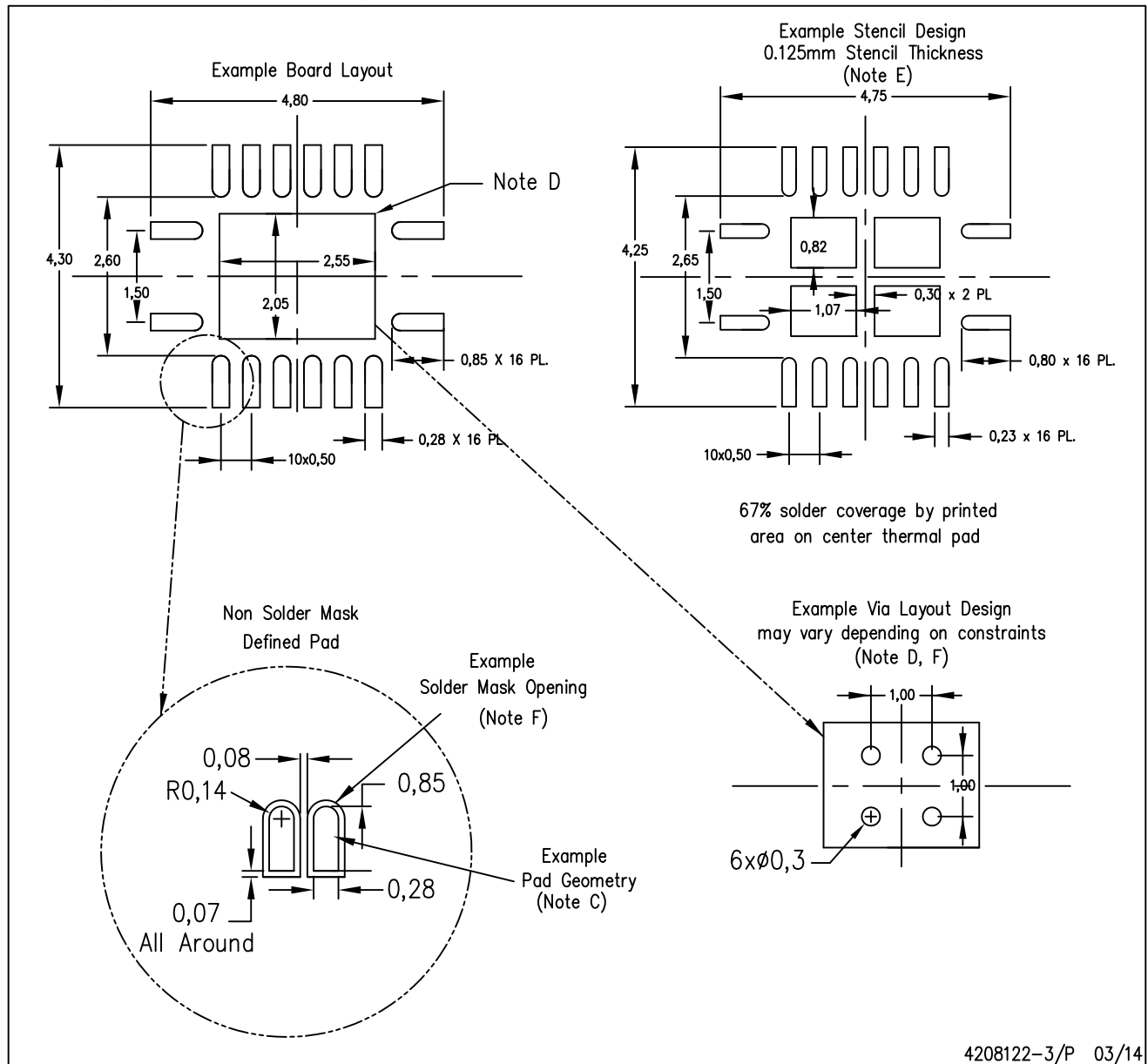
Example Board Layout

Note D

4,80

4,30  2,60

1,50

2,55

2,05

0,85 X 16 PL.

0,28 X 16 PL

10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75

4,25  2,65

1,50

0,82

1,07

0,30 x 2 PL

0,80 x 16 PL.

0,23 x 16 PL.

10x0,50

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6x∅0,3

4208122−3/P   03/14

NOTES:   A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Publication IPC−7351 is recommended for alternate designs.
D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.
These documents are available at www.ti.com <http://www.ti.com>.
E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
F.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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B | 1.85 / 1.75 | A

PIN 1 INDEX AREA

2.65 / 2.55

0.55 / 0.45

0.05 / 0.00

C

SEATING PLANE

0.05 C

2X 1.2

SYMM

5

8

15X 0.45 / 0.35

4

9

SYMM

2X 1.2

12X 0.4

1

12

16X 0.25 / 0.15

16

13

0.07 (M) C A B

0.05 (M)

0.55 / 0.45

PIN 1 ID
(45° X 0.1)

(0.13) TYP

4220314/A   03/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM

(0.7)

16    13

SEE SOLDER MASK DETAIL

16X (0.2)    1    12

12X (0.4)    SYMM

(2.4)

(R0.05) TYP    4    9

15X (0.6)

5    8

(1.6)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 25X

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED

**SOLDER MASK DETAILS**

4220314/A   03/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

**TEXAS INSTRUMENTS**
www.ti.com
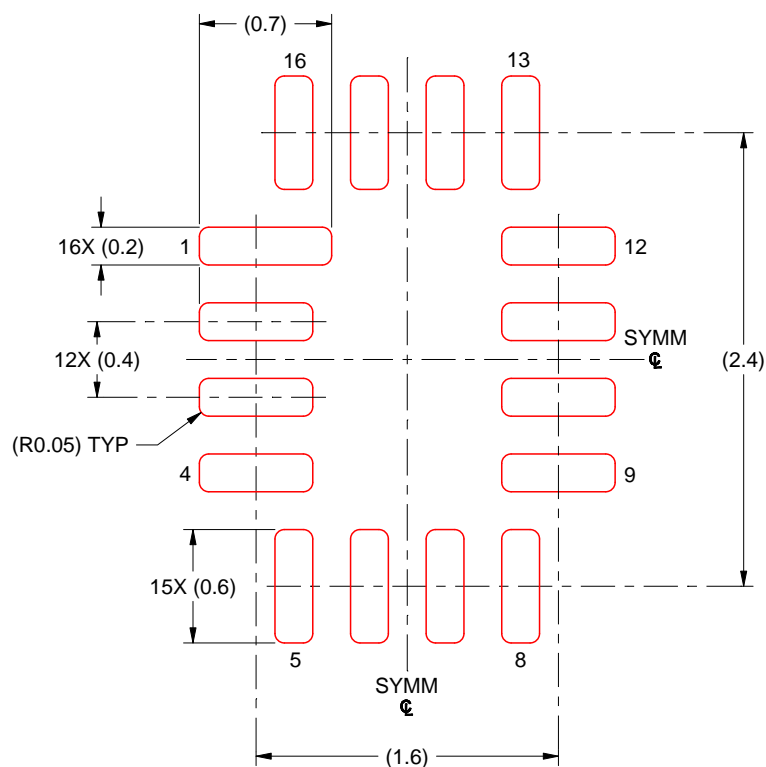
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/A   03/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

**NS (R-PDSO-G**)**                                                    PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

| | PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|---|
| DIM | | | | | |
| A MAX | | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:    A.    All linear dimensions are in millimeters.
          B.    This drawing is subject to change without notice.
          C.    Body dimensions do not include mold flash or protrusion, not to exceed 0,15.