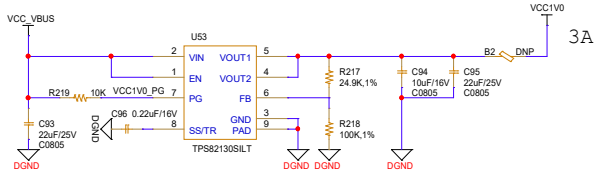
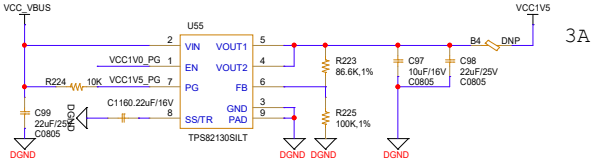
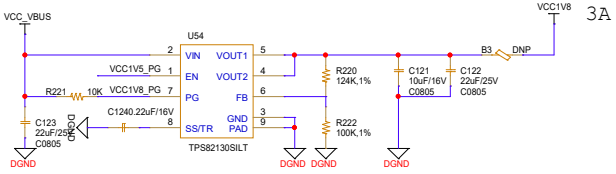
输出电压计算

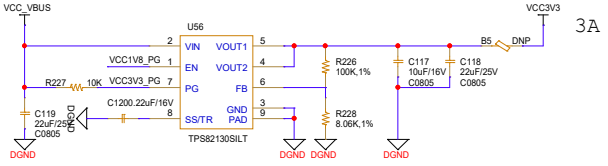
VOUT = Vfb * (1 + R1 / R2)

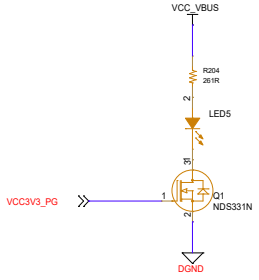
= 0.8V * (1 + R1 / R2)

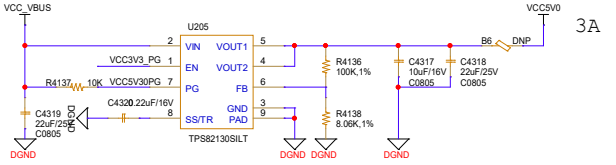




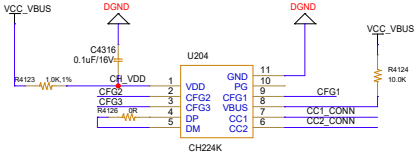






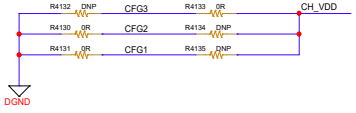


用于给扩展板供电
每个引脚支持2A电流
用丝印标注引脚定义

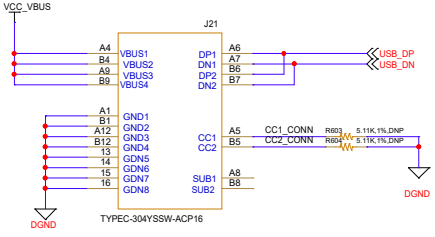


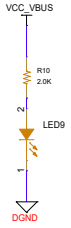
上下拉电阻值修改为0R。

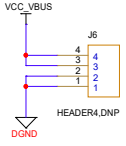
默认12V供电

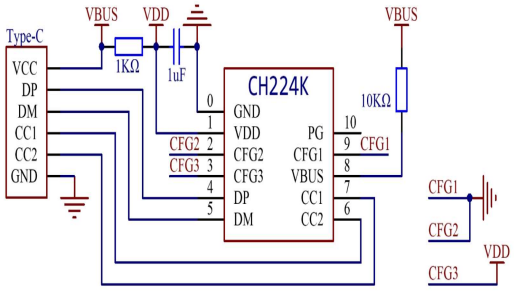


6.2. CH224K 使用 Type-C 母口，电平配置 5/9/12/15/20V（图中电平方式配置为 12v）



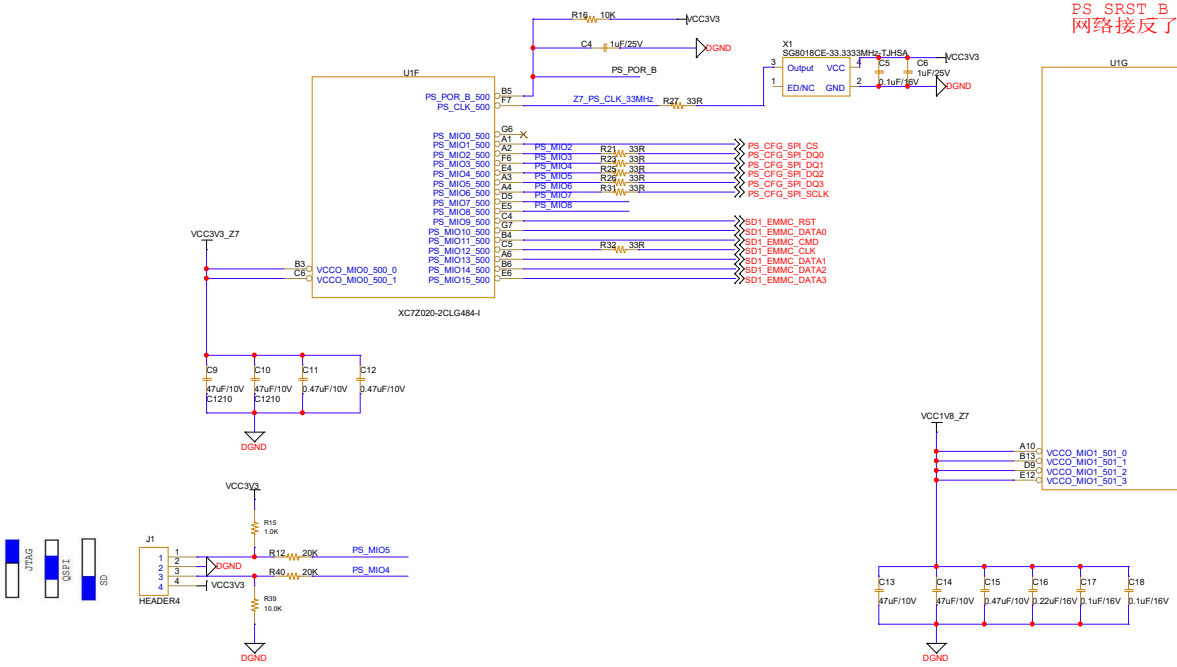






CFG1	CFG2	CFG3	请求电压
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

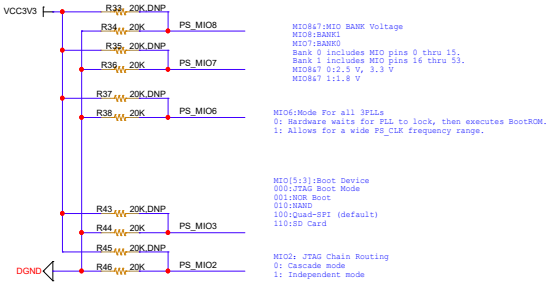
设计错误 ：
PS_SRST_B 和 PS_MIO_VREF
网络接反了



按照HREADER4左侧的图片的顺序来做一列丝印

MIO8的电阻应该修改为上拉 （1.8V）

BOOT STRAP CONFIGURATION



确认阻值为 20K

Table 5-3: **Voltage Mode Configuration**

I/O Bank	I/O Supply Name	Programming Pin	1.8V Mode	2.5V, 3.3V Modes
MIO Bank 0	V_{CCO_MIO0}	MIO[7]	20 KΩ resistor to V_{CCO_MIO0}	20 KΩ resistor to ground
MIO Bank 1	V_{CCO_MIO1}	MIO[8]	20 KΩ resistor to V_{CCO_MIO0}	20 KΩ resistor to ground

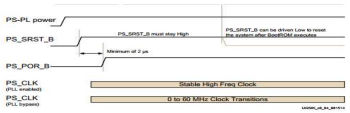
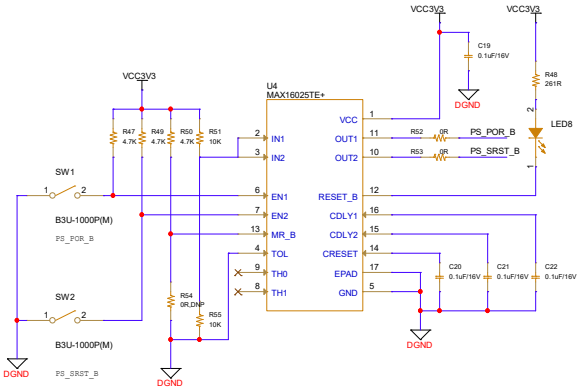


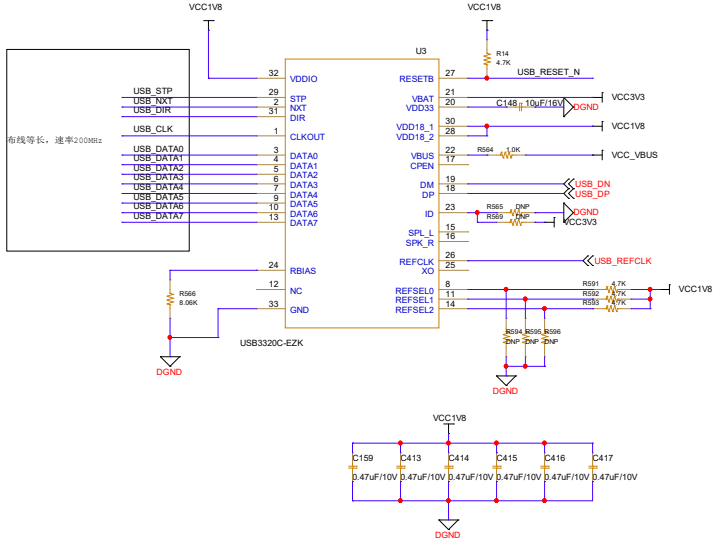
Figure 6-4: **Power and Reset Sequencing Waveform**

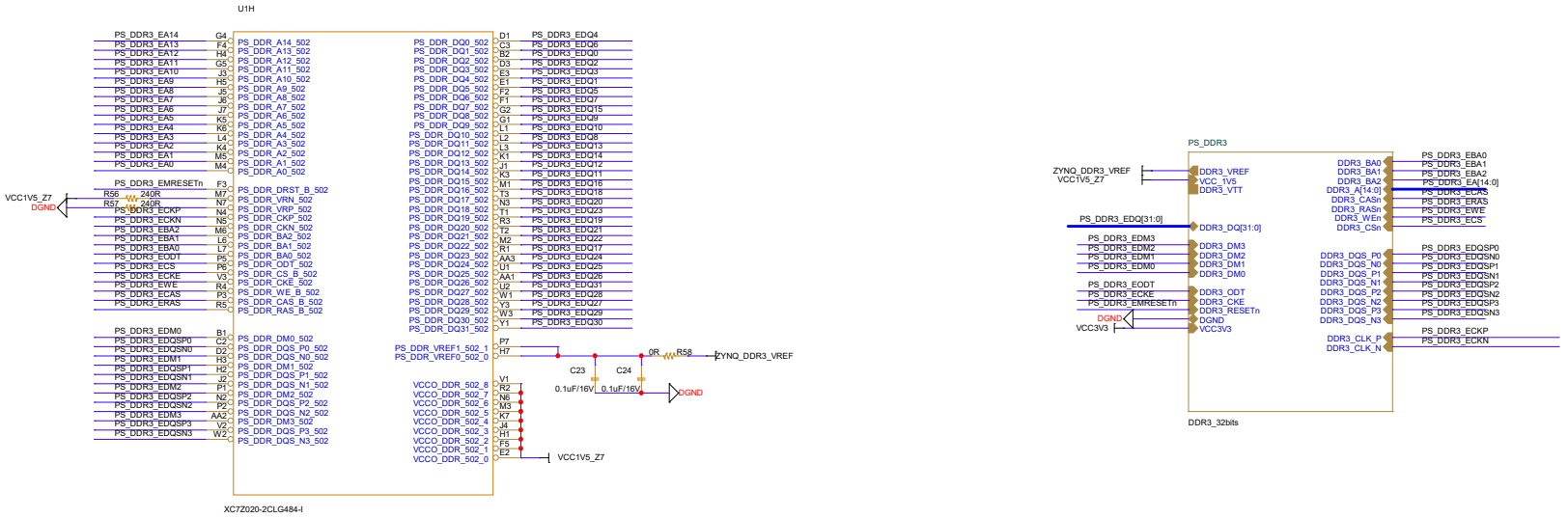
这一排上下拉电阻上拉电阻放成一排 ， 丝印标注为1
下拉放成一排，丝印标注为0 。
摆放位置方便手工焊接 。
标注对应的MIO编号 。
按照MIO8到MIO2的顺序排列 。



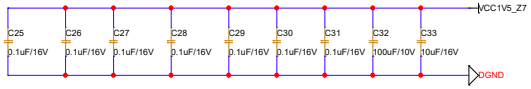
USB的电路需要确认 。

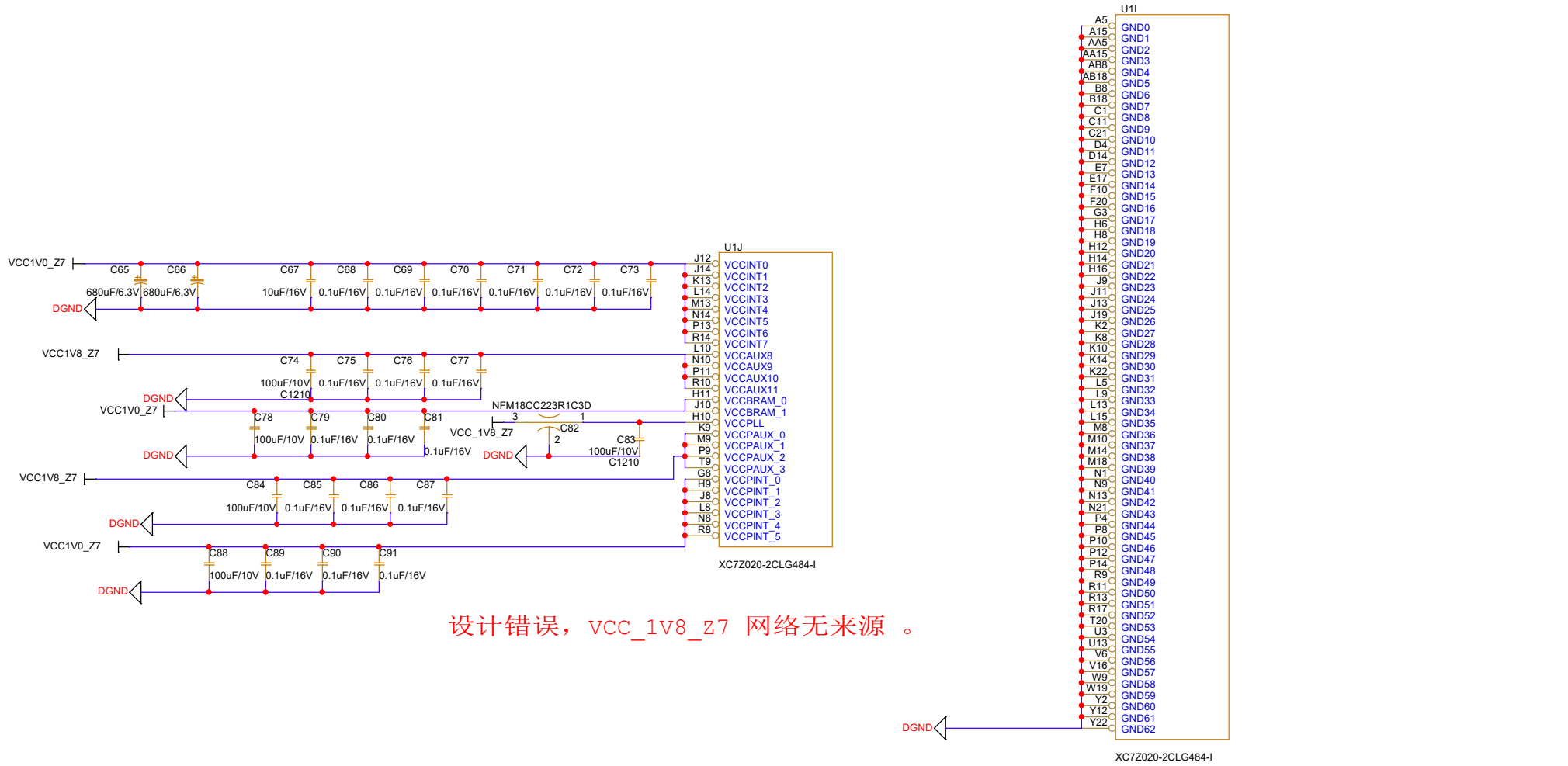
USB SLAVE 设备

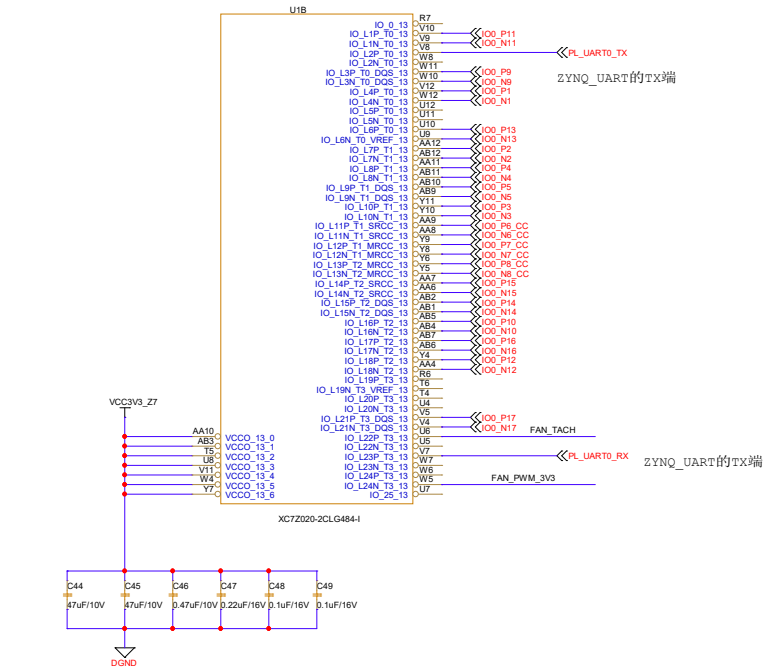


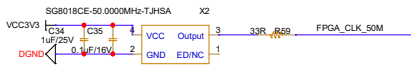


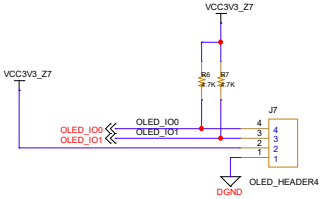
CK走线必须等于或长于DQS走线；（UG201）
1、写入DQS的时候，时钟信号也平有足够的调节容限；
2、读取DQS时，时钟信号有足够的容限去调节读数据眼图；
3、对于DDR的命令和地址信号相对于时钟的时序而言，是没有自动的训练功能，但是必要的时候，是可以设置一个固定的偏置值

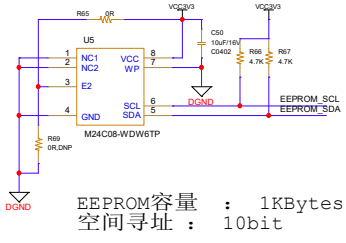



U1J
VCC1V0_Z7
C65
C66
C67
C68
C69
C70
C71
C72
C73
680uF/6.3V
680uF/6.3V
10uF/16V
0.1uF/16V
DGND
VCC1V8_Z7
C74
C75
C76
C77
100uF/10V
C1210
0.1uF/16V
C78
C79
C80
C81
NFM18CC223R1C3D
C82
C83
VCC_1V8_Z7
100uF/10V
C1210
C84
C85
C86
C87
C88
C89
C90
C91
J12
J14
K13
L14
M13
N14
P13
R14
L10
N10
P11
R10
H11
J10
H10
K9
M9
P9
T9
G8
H9
J8
L8
N8
R8
VCCINT0
VCCINT1
VCCINT2
VCCINT3
VCCINT4
VCCINT5
VCCINT6
VCCINT7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCBRAM_0
VCCBRAM_1
VCCPLL
VCCPAUX_0
VCCPAUX_1
VCCPAUX_2
VCCPAUX_3
VCCPINT_0
VCCPINT_1
VCCPINT_2
VCCPINT_3
VCCPINT_4
VCCPINT_5
XC7Z020-2CLG484-I
U1I
A5
A15
AA5
AA15
AB8
AB18
B8
B18
C1
C11
C21
D4
D14
E7
E17
F10
F20
G3
H6
H8
H12
H14
H16
J9
J11
J13
J19
K2
K8
K10
K14
K22
L5
L9
L13
L15
M8
M10
M14
M18
N1
N9
N13
N21
P4
P8
P10
P12
P14
R9
R11
R13
R17
T20
U3
U13
V6
V16
W9
W19
Y2
Y12
Y22
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND21
GND22
GND23
GND24
GND25
GND26
GND27
GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND36
GND37
GND38
GND39
GND40
GND41
GND42
GND43
GND44
GND45
GND46
GND47
GND48
GND49
GND50
GND51
GND52
GND53
GND54
GND55
GND56
GND57
GND58
GND59
GND60
GND61
GND62
XC7Z020-2CLG484-I
设计错误，VCC_1V8_Z7 网络无来源 。





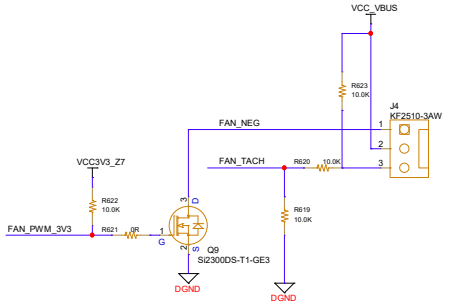




EEPROM容量 ： 1KBytes
空间寻址 ： 10bit

38mm * 13mm
128*32 , IIC 接口屏幕

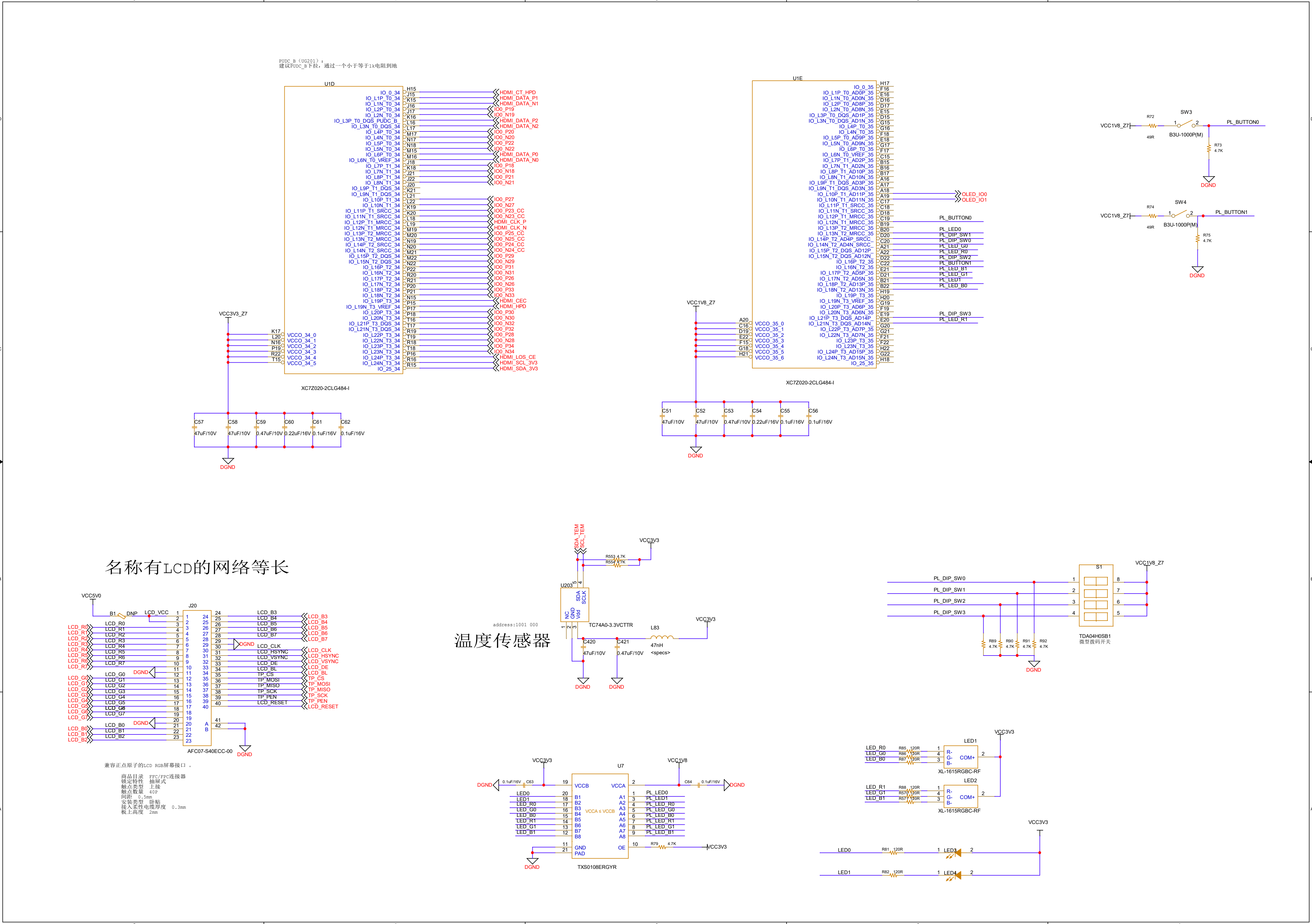
用于显示板卡的一些配置信息（如网络IP）

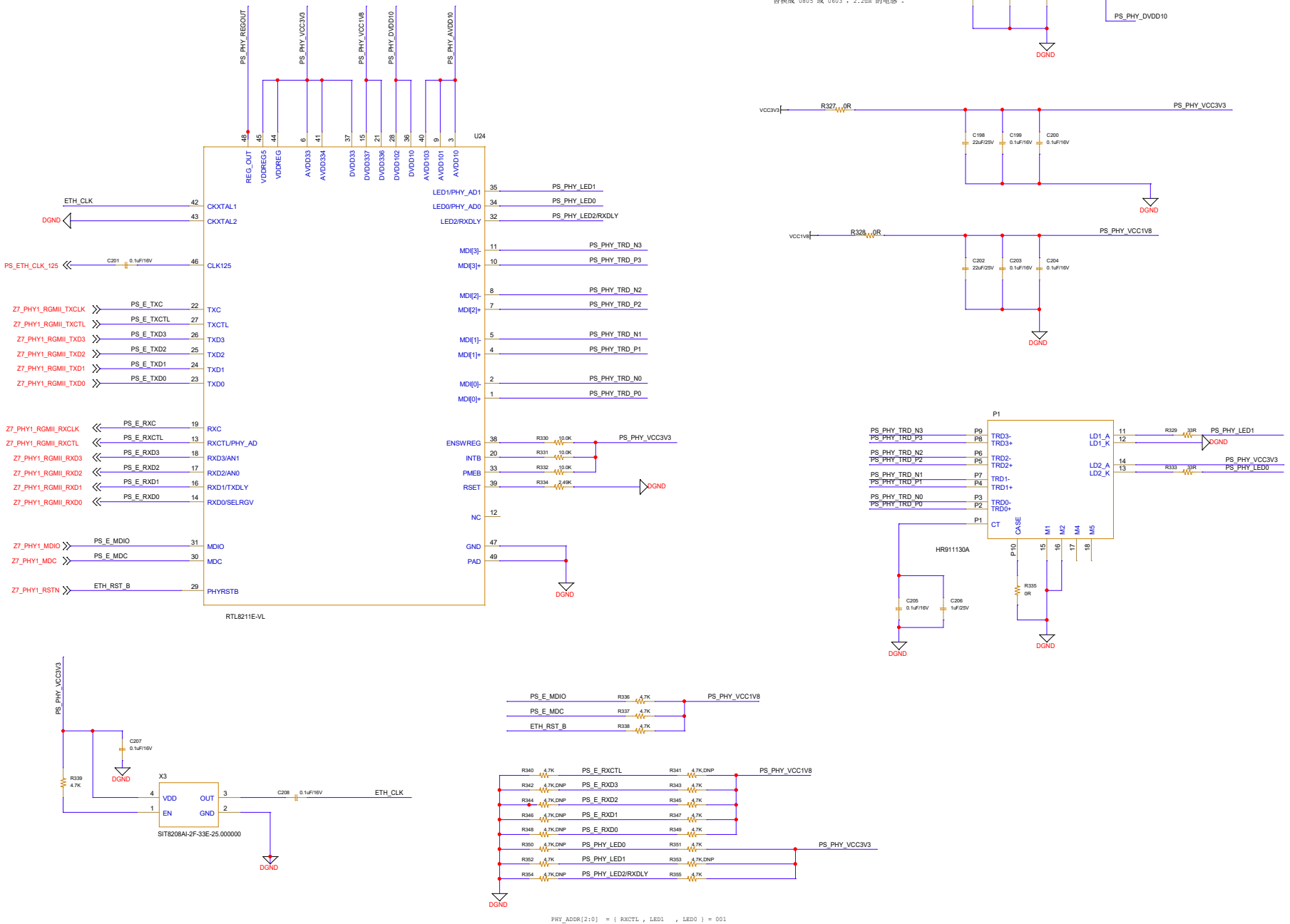


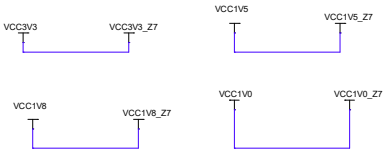
1 脚 和 2脚 至少支持3A的电流，用于直流风扇供电。

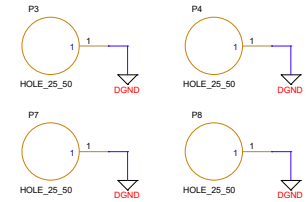
Table 3. Device select code

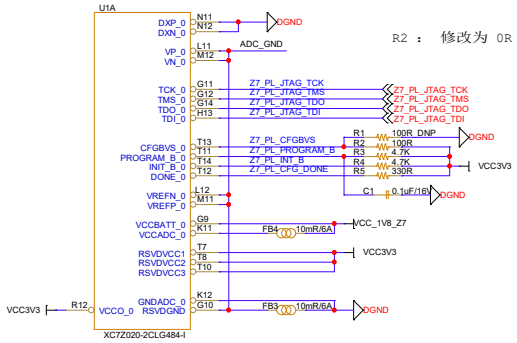
Package	Device type identifier(1)				Chip Enable address			R/W
	b7	b6	b5	b4	b3	b2	b1	b0
TSSOP8,SO8,PDIP8, UFDFPN8	1	0	1	0	E2	A9	A8	R/W


PUDC_B (UG201):
建议PUDC_B下拉，通过一个小于等于1k电阻到地
U1D
XC7Z020-2CLG484-I
HDMI_CT_HPD
HDMI_DATA_P1
HDMI_DATA_N1
IO0_P19
IO0_N19
HDMI_DATA_P2
HDMI_DATA_N2
IO0_P20
IO0_N20
IO0_P22
IO0_N22
HDMI_DATA_P0
HDMI_DATA_N0
IO0_P18
IO0_N18
IO0_P21
IO0_N21
IO0_P27
IO0_N27
IO0_P23_CC
IO0_N23_CC
HDMI_CLK_P
HDMI_CLK_N
IO0_P25_CC
IO0_N25_CC
IO0_P24_CC
IO0_N24_CC
IO0_P29
IO0_N29
IO0_P31
IO0_N31
IO0_P26
IO0_N26
IO0_P33
IO0_N33
HDMI_CEC
HDMI_HPD
IO0_P30
IO0_N30
IO0_P32
IO0_N32
IO0_P28
IO0_N28
IO0_P34
IO0_N34
HDMI_LOS_CE
HDMI_SCL_3V3
HDMI_SDA_3V3
VCC3V3_Z7
VCCO_34_0
VCCO_34_1
VCCO_34_2
VCCO_34_3
VCCO_34_4
VCCO_34_5
C57 47uF/10V
C58 47uF/10V
C59 0.47uF/10V
C60 0.22uF/16V
C61 0.1uF/16V
C62 0.1uF/16V
DGND
U1E
XC7Z020-2CLG484-I
OLED_IO0
OLED_IO1
PL_BUTTON0
PL_LED0
PL_DIP_SW1
PL_DIP_SW0
PL_LED_G0
PL_LED_R0
PL_DIP_SW2
PL_BUTTON1
PL_LED_B1
PL_LED_G1
PL_LED1
PL_LED_B0
PL_DIP_SW3
PL_LED_R1
VCC1V8_Z7
VCCO_35_0
VCCO_35_1
VCCO_35_2
VCCO_35_3
VCCO_35_4
VCCO_35_5
VCCO_35_6
C51 47uF/10V
C52 47uF/10V
C53 0.47uF/10V
C54 0.22uF/16V
C55 0.1uF/16V
C56 0.1uF/16V
SW3
R72 49R
B3U-1000P(M)
R73 4.7K
SW4
R74 49R
B3U-1000P(M)
R75 4.7K
名称有LCD的网络等长
VCC5V0
B1 DNP
LCD_VCC
J20
AFC07-S40ECC-00
LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_CLK
LCD_HSYNC
LCD_VSYNC
LCD_DE
LCD_BL
TP_CS
TP_MOSI
TP_MISO
TP_SCK
TP_PEN
LCD_RESET
兼容正点原子的LCD RGB屏幕接口 。
商品目录 FFC/FPC连接器
锁定特性 抽屉式
触点类型 上接
触点数量 40P
间距 0.5mm
安装类型 卧贴
接入柔性电缆厚度 0.3mm
板上高度 2mm
SDA_TEM
SCL_TEM
VCC3V3
R553 4.7K
R554 4.7K
U203
TC74A0-3.3VCTTR
address:1001 000
温度传感器
C420 47uF/10V
C421 0.47uF/10V
L83 47nH <specs>
S1
VCC1V8_Z7
PL_DIP_SW0
PL_DIP_SW1
PL_DIP_SW2
PL_DIP_SW3
R89 4.7K
R90 4.7K
R91 4.7K
R92 4.7K
TDA04H0SB1
微型拨码开关
U7
TXS0108ERGYR
VCC1V8
C63 0.1uF/16V
C64 0.1uF/16V
VCCB
VCCA
VCCA ≤ VCCB
LED0
LED1
LED_R0
LED_G0
LED_B0
LED_R1
LED_G1
LED_B1
PL_LED0
PL_LED1
PL_LED_R0
PL_LED_G0
PL_LED_B0
PL_LED_R1
PL_LED_G1
PL_LED_B1
GND
PAD
OE
R79 4.7K
LED1
R85 120R
R86 120R
R87 120R
XL-1615RGBC-RF
LED2
R88 120R
R570 120R
R571 120R
XL-1615RGBC-RF
R- G- B- COM+
R81 120R
LED3
R82 120R
LED4


PS_PHY_REGOUT
R326 2.2uH
PS_PHY_AVDD10
REG_OUT 输出端应该连接2.2uH ~ 4.7uH 的电感 。
替换成 0805 或 0603 , 2.2uH 的电感 。
C195 22uF/25V
C196 0.1uF/16V
C197 0.1uF/16V
PS_PHY_DVDD10
DGND
VCC3V3
R327 0R
PS_PHY_VCC3V3
C198 22uF/25V
C199 0.1uF/16V
C200 0.1uF/16V
VCC1V8
R328 0R
PS_PHY_VCC1V8
C202 22uF/25V
C203 0.1uF/16V
C204 0.1uF/16V
U24
REG_OUT
VDDREG5
VDDREG
AVDD33
AVDD334
DVDD33
DVDD337
DVDD336
DVDD102
DVDD10
AVDD103
AVDD101
AVDD10
ETH_CLK
CKXTAL1
CKXTAL2
PS_ETH_CLK_125
C201 0.1uF/16V
CLK125
Z7_PHY1_RGMII_TXCLK
PS_E_TXC
TXC
Z7_PHY1_RGMII_TXCTL
PS_E_TXCTL
TXCTL
Z7_PHY1_RGMII_TXD3
PS_E_TXD3
TXD3
Z7_PHY1_RGMII_TXD2
PS_E_TXD2
TXD2
Z7_PHY1_RGMII_TXD1
PS_E_TXD1
TXD1
Z7_PHY1_RGMII_TXD0
PS_E_TXD0
TXD0
Z7_PHY1_RGMII_RXCLK
PS_E_RXC
RXC
Z7_PHY1_RGMII_RXCTL
PS_E_RXCTL
RXCTL/PHY_AD
Z7_PHY1_RGMII_RXD3
PS_E_RXD3
RXD3/AN1
Z7_PHY1_RGMII_RXD2
PS_E_RXD2
RXD2/AN0
Z7_PHY1_RGMII_RXD1
PS_E_RXD1
RXD1/TXDLY
Z7_PHY1_RGMII_RXD0
PS_E_RXD0
RXD0/SELRGV
Z7_PHY1_MDIO
PS_E_MDIO
MDIO
Z7_PHY1_MDC
PS_E_MDC
MDC
Z7_PHY1_RSTN
ETH_RST_B
PHYRSTB
LED1/PHY_AD1
PS_PHY_LED1
LED0/PHY_AD0
PS_PHY_LED0
LED2/RXDLY
PS_PHY_LED2/RXDLY
MDI[3]-
PS_PHY_TRD_N3
MDI[3]+
PS_PHY_TRD_P3
MDI[2]-
PS_PHY_TRD_N2
MDI[2]+
PS_PHY_TRD_P2
MDI[1]-
PS_PHY_TRD_N1
MDI[1]+
PS_PHY_TRD_P1
MDI[0]-
PS_PHY_TRD_N0
MDI[0]+
PS_PHY_TRD_P0
ENSWREG
R330 10.0K
INTB
R331 10.0K
PMEB
R332 10.0K
RSET
R334 2.49K
NC
GND
PAD
RTL8211E-VL
P1
PS_PHY_TRD_N3
PS_PHY_TRD_P3
PS_PHY_TRD_N2
PS_PHY_TRD_P2
PS_PHY_TRD_N1
PS_PHY_TRD_P1
PS_PHY_TRD_N0
PS_PHY_TRD_P0
TRD3-
TRD3+
TRD2-
TRD2+
TRD1-
TRD1+
TRD0-
TRD0+
CT
CASE
HR911130A
LD1_A
LD1_K
LD2_A
LD2_K
R329 33R
R333 33R
PS_PHY_LED1
PS_PHY_LED0
R335 0R
C205 0.1uF/16V
C206 1uF/25V
PS_PHY_VCC3V3
DGND
X3
VDD
EN
OUT
GND
C207 0.1uF/16V
R339 4.7K
C208 0.1uF/16V
SIT8208AI-2F-33E-25.000000
R336 4.7K
R337 4.7K
R338 4.7K
R340 4.7K
R341 4.7K,DNP
R342 4.7K,DNP
R343 4.7K
R344 4.7K,DNP
R345 4.7K
R346 4.7K,DNP
R347 4.7K
R348 4.7K,DNP
R349 4.7K
R350 4.7K,DNP
R351 4.7K
R352 4.7K
R353 4.7K,DNP
R354 4.7K,DNP
R355 4.7K
PHY_ADDR[2:0] = { RXCTL , LED1 , LED0 } = 001
Auto - Negotiation [1:0] = { RXD3 , RXD2 } = 11 (Nway, Advertise all capabilities)
RX Delay = LED2 = 1 (add 2ns delay to RXC for RXD latching , via 4.7K to 3.3V)
TX Delay = RXD1 = 1 (add 2ns delay to TXC for TXD latching , via 4.7K to 3.3V)
SELRGV = RXD0 = 1 (Pull up for RGMII 1.8V)

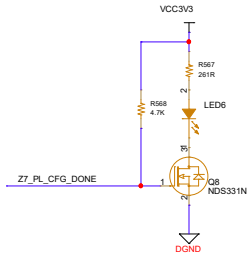


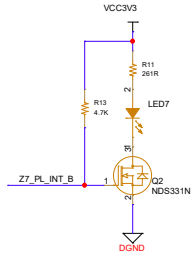




R2 ： 修改为 0R ？

FMQL的CFGBVS_0信号必须上拉至VCCO0电源
（上拉电阻10欧，如为低，PL部分JTAG存在下载失败风险！

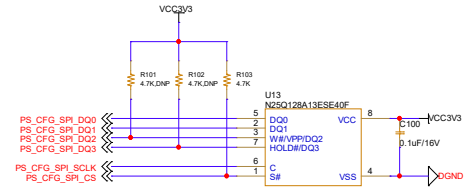




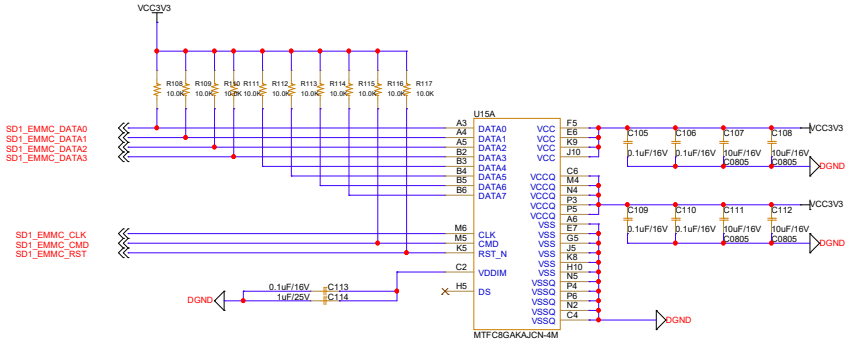
DONE INIT

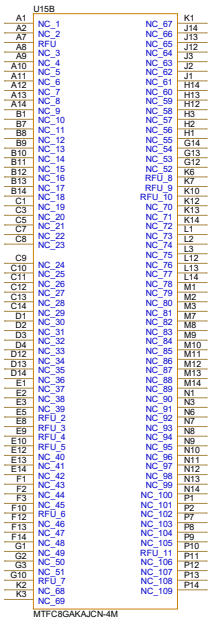
两个LED均等需打上丝印

设计更改：
LED限流电阻值过小，LED灯亮度太刺眼 。
限流电阻值需要改大。

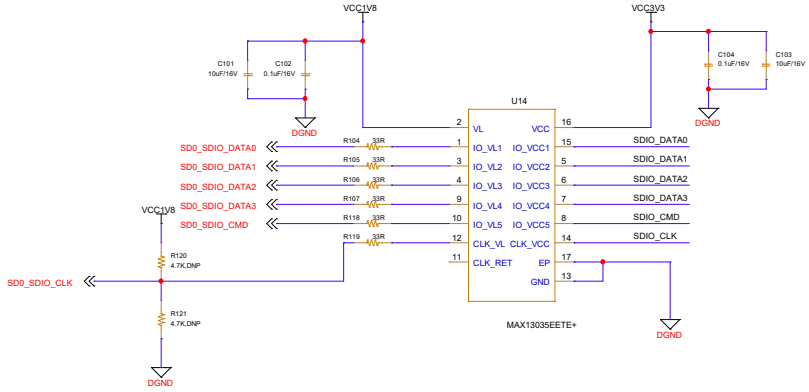


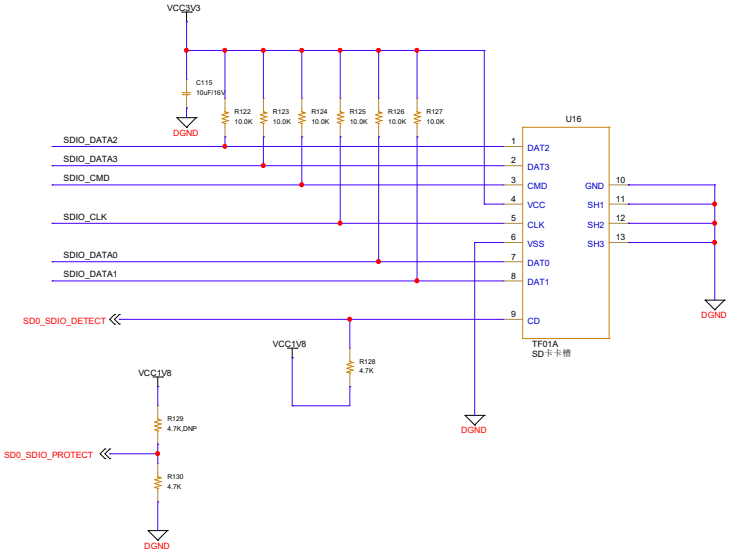
20210701:
FLASH的HOLD/WP信号增加上拉预留

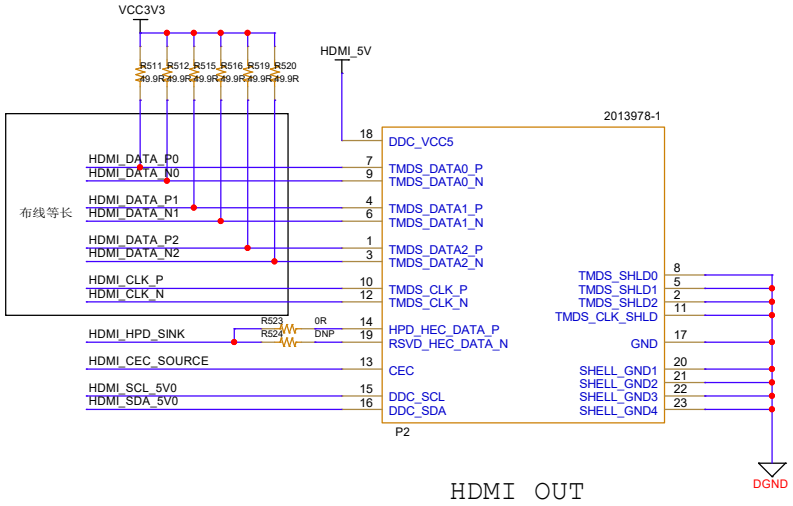




SD卡

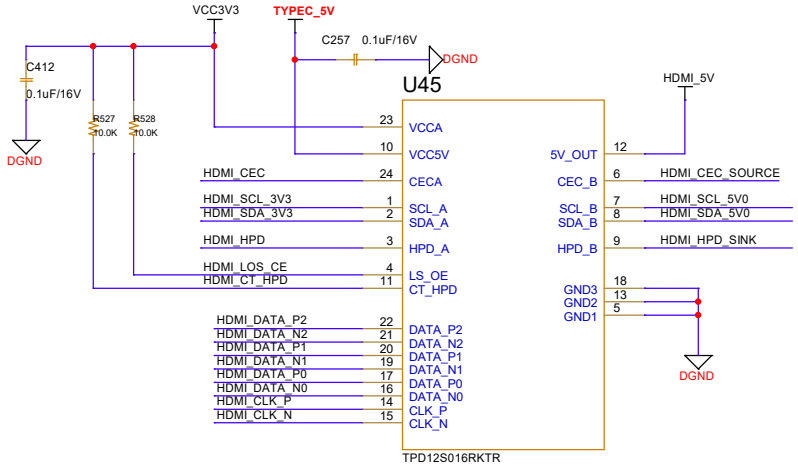




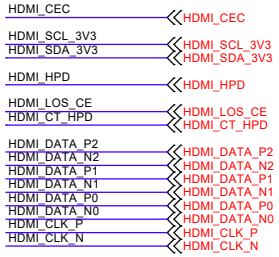


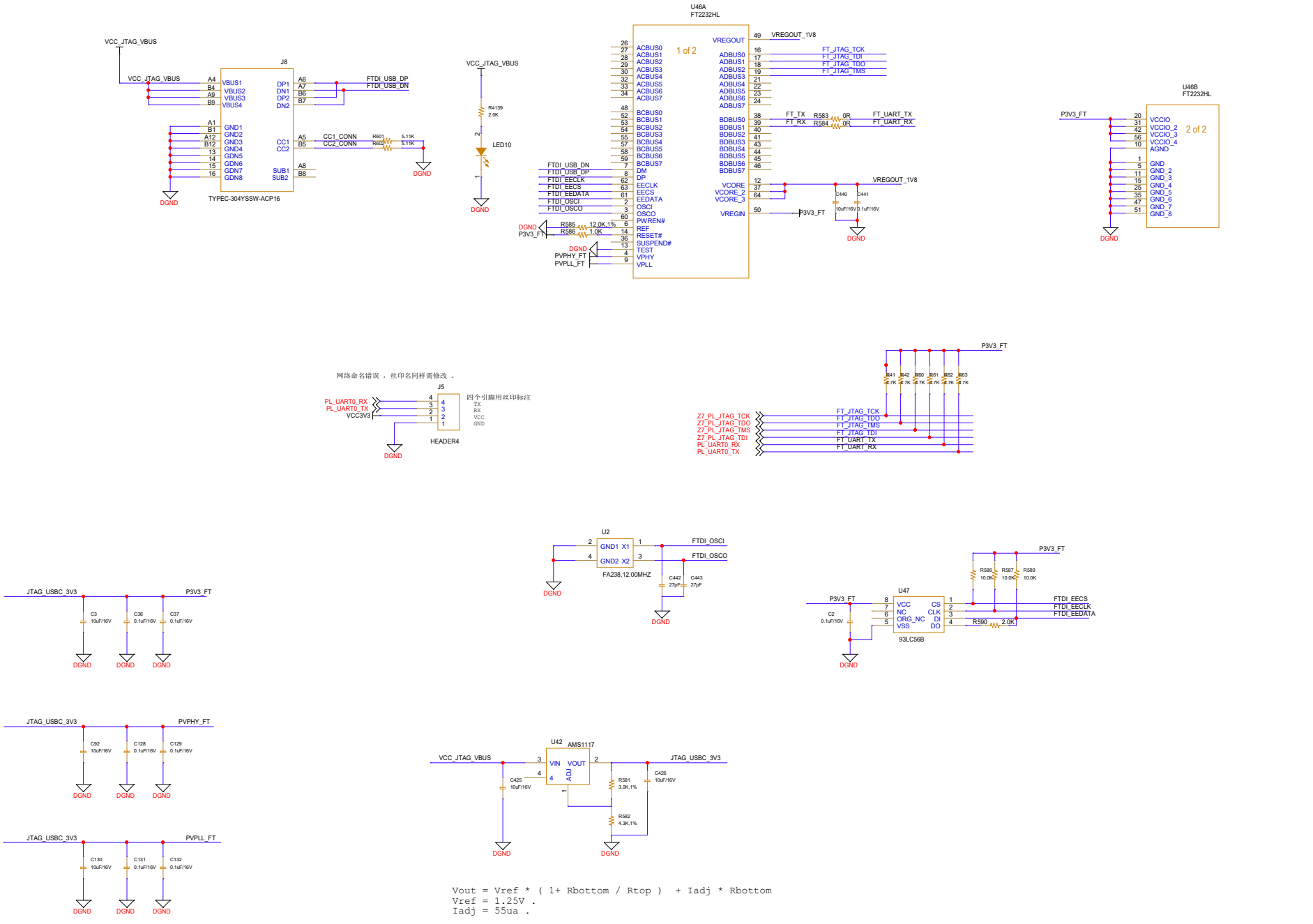
HDMI OUT

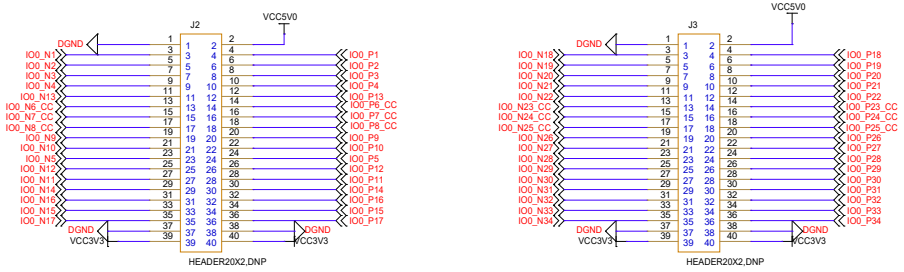
设计错误，此 TYPEC 5V 无来源 。
可用 B6 焊盘上飞线到 C257 的 1脚上使用。



HDMI ESD

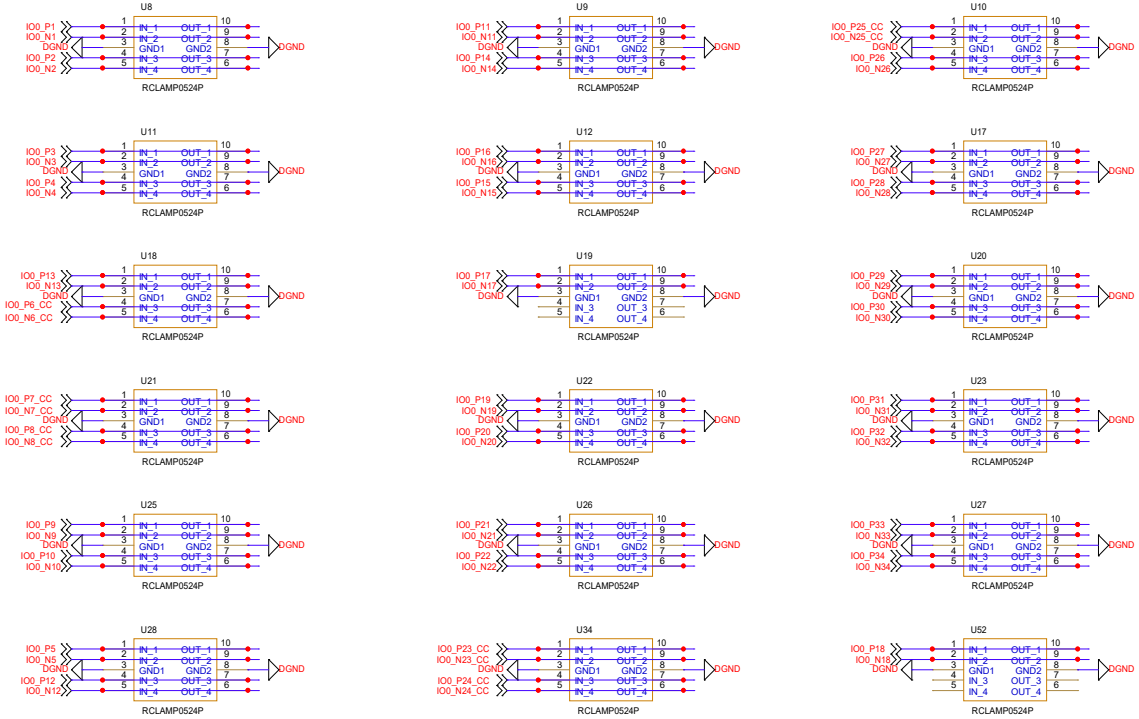


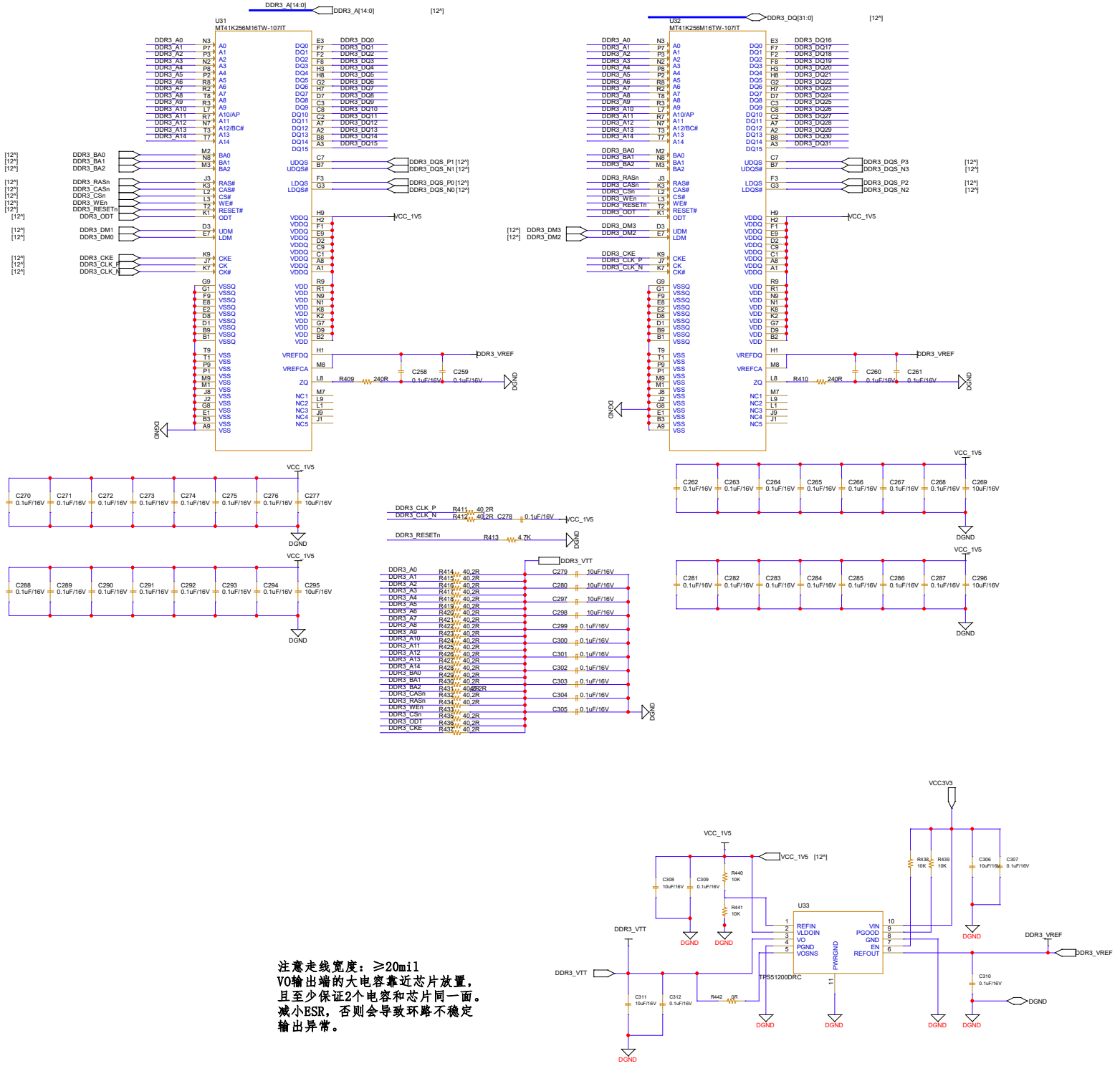

VCC_JTAG_VBUS
J8
TYPEC-304YSSW-ACP16
FTDI_USB_DP
FTDI_USB_DN
CC1_CONN
CC2_CONN
R601
R602
5.11K
DGND
U46A
FT2232HL
1 of 2
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
DM
DP
EECLK
EECS
EEDATA
OSCI
OSCO
PWREN#
REF
RESET#
SUSPEND#
TEST
VPHY
VPLL
VREGOUT
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
VCORE
VCORE_2
VCORE_3
VREGIN
VREGOUT_1V8
FT_JTAG_TCK
FT_JTAG_TDI
FT_JTAG_TDO
FT_JTAG_TMS
FT_TX
FT_RX
FT_UART_TX
FT_UART_RX
R583
R584
0R
R585
R586
12.0K,1%
1.0K
P3V3_FT
PVPHY_FT
PVPLL_FT
LED10
R4139
2.0K
C440
C441
10uF/16V
0.1uF/16V
U46B
2 of 2
VCCIO
VCCIO_2
VCCIO_3
VCCIO_4
AGND
GND
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
网络命名错误 ，丝印名同样需修改 。
J5
HEADER4
四个引脚用丝印标注
TX
RX
VCC
GND
PL_UART0_RX
PL_UART0_TX
VCC3V3
Z7_PL_JTAG_TCK
Z7_PL_JTAG_TDO
Z7_PL_JTAG_TMS
Z7_PL_JTAG_TDI
R641
R642
R660
R661
R662
R663
4.7K
U2
GND1 X1
GND2 X2
FA238,12.00MHZ
C442
C443
27pF
FTDI_OSCI
FTDI_OSCO
U47
93LC56B
VCC
NC
ORG_NC
VSS
CS
CLK
DI
DO
C2
0.1uF/16V
R588
R587
R589
10.0K
R590
2.0K
FTDI_EECS
FTDI_EECLK
FTDI_EEDATA
JTAG_USBC_3V3
C3
C36
C37
10uF/16V
0.1uF/16V
PVPHY_FT
C92
C128
C129
PVPLL_FT
C130
C131
C132
U42
AMS1117
VIN
VOUT
ADJ
C425
C426
R581
3.0K,1%
R582
4.3K,1%
Vout = Vref * (1+ Rbottom / Rtop) + Iadj * Rbottom
Vref = 1.25V .
Iadj = 55ua .



引脚定义

1 , 37 , 38 ： 地
2 : 5.0V
39 , 40 : 3.3V
13 14 : 差分时钟对
15 16 : 差分时钟对
17 18 : 差分时钟对
其余引脚 ： 3.3V通用IO





注意走线宽度：≥20mil
VO输出端的大电容靠近芯片放置，
且至少保证2个电容和芯片同一面。
减小ESR，否则会导致环路不稳定
输出异常。