DCC read amplifier (READ 3) TDA1380

FEATURES

- Single 3 V supply
- Low power consumption
- Differential inputs for low power head configuration
- Can be used with 1st, 2nd and 3rd generation digital signal processing ICs
- Automatic gain control for DCC preamplifiers
- Selectable input amplifiers for A or B side of cassette
- ACC playback via DCC preamplifiers
- Uncommitted amplifiers for equalization during ACC playback
- Low noise current sources for the sense currents of the DCC heads
- Generates reference sense current for temperature compensation of the write current, in recordable application with the TDA1381
- High feedback application possible (for adjustment minimization)
- Suitable for digital post-processor.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1380 amplifies, filters and multiplexes signals that are input from an 18-channel magnetoresistive thin film head (MRH) suitable for the DCC (Digital Compact Cassette) and ACC (Analog Compact Cassette) systems. The device also contains current sources to provide sense currents through the heads and amplifiers for magnetic feedback and biasing. Two uncommitted amplifiers are available for analog equalization.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1380	TQFP64[1]	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"*: (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS ON PINS[1]			MIN.	TYP.	MAX.	UNIT
		CS	SA	AB				
V_{DD}	supply voltage	–	–	–	2.7	3.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers	–	–	–	2.7	3.0	5.5	V
$I_{DDDCC} + I_{CCM}$	supply current DCC mode	1	0	X	28	39	53	mA
$I_{DDACC} + I_{CCM}$	supply current ACC mode	1	1	X	26	35	47	mA
I_{DDRS}	supply current reference sense current mode	0	0	X	0.6	1.2	1.6	mA
I_{DDAB}	supply current sense AB mode	0	1	1	1.5	2.7	3.7	mA
$I_{DDstb} + I_{CCM}$	supply current standby mode	0	1	0	–	0.2	0.3	mA
$P_{(tot)DCC}$	total power dissipation DCC mode; note 2	1	0	X	–	120	–	mW
$P_{(tot)ACC}$	total power dissipation ACC mode; note 2	1	1	X	–	105	–	mW
T_{amb}	operating ambient temperature	–	–	–	–30	–	+85	°C

Notes

1. In the conditions column 0 = LOW; 1 = HIGH; X = don't care.
2. $V_{DD} = V_{CCM} = 3$ V; $I_{DSEN} = 0$; $I_{FB} = 0$.

BLOCK DIAGRAM

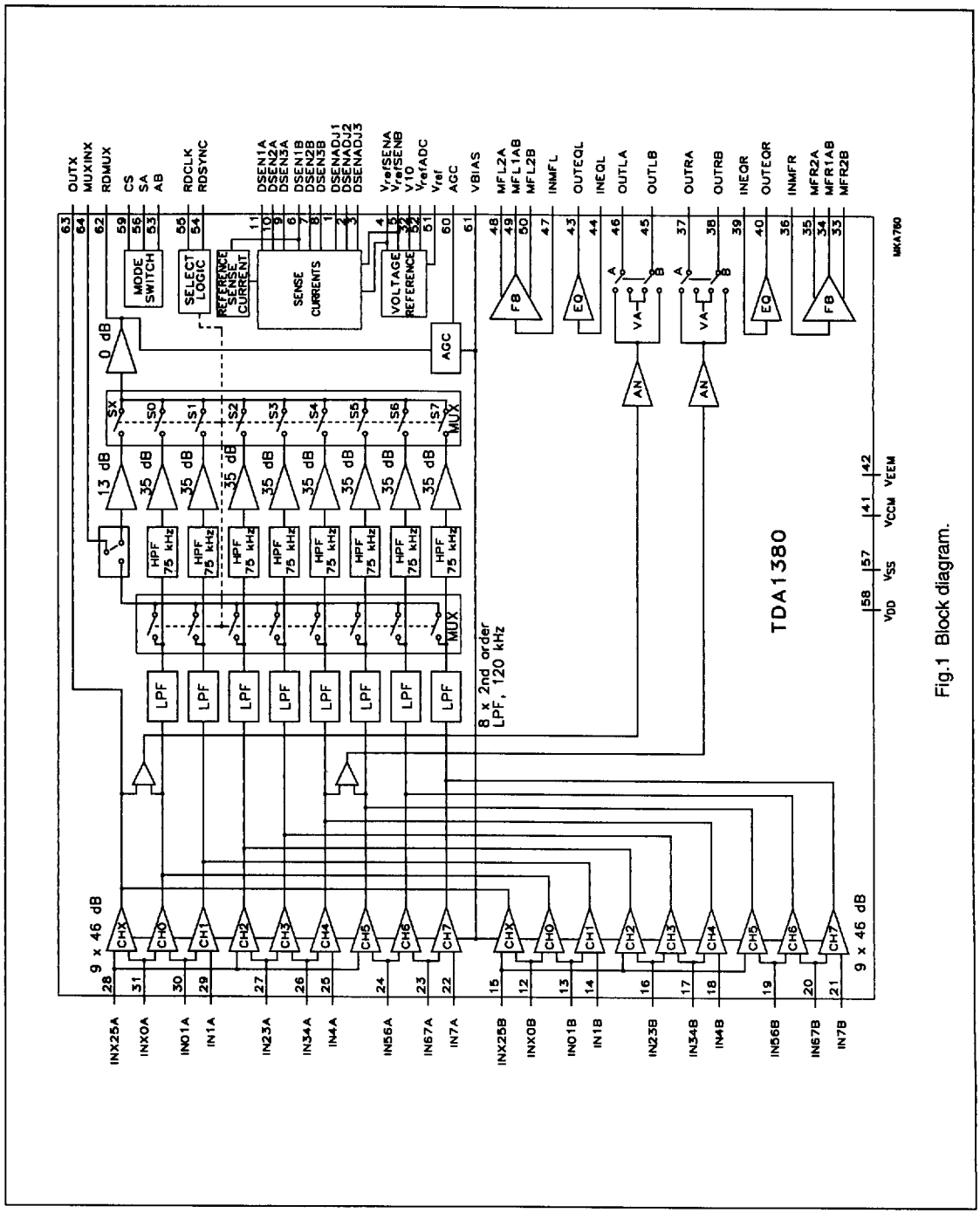


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DSENADJ1	1	adjustment pin for sense current 1 (A and B)
DSENADJ2	2	adjustment pin for sense current 2 (A and B)
DSENADJ3	3	adjustment pin for sense current 3 (A and B)
$V_{refSENA}$	4	reference voltage output sense (A)
$V_{refSENB}$	5	reference voltage output sense (B)
DSEN1B	6	sense current output 1 (B)
DSEN2B	7	sense current output 2 (B)
DSEN3B	8	sense current output 3 (B)
DSEN3A	9	sense current output 3 (A)
DSEN2A	10	sense current output 2 (A)
DSEN1A	11	sense current output 1 (A)
INX0B	12	auxiliary channel input/channel 0 input (B)
IN01B	13	channel 0 and 1 input (B)
IN1B	14	channel 1 input (B)
INX25B	15	channels AUX, 2 and 5 input (B)
IN23B	16	channels 2 and 3 input (B)
IN34B	17	channels 3 and 4 input (B)
IN4B	18	channel 4 input (B)
IN56B	19	channels 5 and 6 input (B)
IN67B	20	channels 6 and 7 input (B)
IN7B	21	channel 7 input (B)
IN7A	22	channel 7 input (A)
IN67A	23	channels 6 and 7 input (A)
IN56A	24	channels 5 and 6 input (A)
IN4A	25	channel 4 input (A)
IN34A	26	channels 3 and 4 input (A)
IN23A	27	channels 2 and 3 input (A)
INX25A	28	channels AUX, 2 and 5 input (A)
IN1A	29	channel 1 input (A)
IN01A	30	channels 0 and 1 input (A)
INX0A	31	auxiliary channel input/channel 0 input (A)
V10	32	reference voltage for DCC inputs
MFR2B	33	right channel feedback amplifier output 2 (B)
MFR1AB	34	right channel feedback amplifier output 1 (A and B)

SYMBOL	PIN	DESCRIPTION
MFR2A	35	right channel feedback amplifier output 2 (A)
INMFR	36	right channel feedback amplifier input
OUTRA	37	right channel ACC output (A)
OUTRB	38	right channel ACC output (B)
INEQR	39	right channel equalization amplifier input
OUTEQR	40	right channel equalization amplifier output
V_{CCM}	41	supply voltage for feedback amplifiers
V_{EEM}	42	ground for feedback amplifiers
OUTEQL	43	left channel equalization amplifier output
INEQL	44	left channel equalization amplifier input
OUTLB	45	left channel ACC output (B)
OUTLA	46	left channel ACC output (A)
INMFL	47	left channel feedback amplifier input
MFL2A	48	left channel feedback amplifier output 2 (A)
MFL1AB	49	left channel feedback amplifier output 1 (A and B)
MFL2B	50	left channel feedback amplifier output 2 (B)
V_{ref}	51	reference voltage output
V_{refADC}	52	ADC reference voltage output
AB	53	tape sector A or B selection input
RDSYNC	54	read sync pulse input
RDCLK	55	read clock pulse input
SA	56	select ACC mode input
V_{SS}	57	ground
V_{DD}	58	supply voltage
CS	59	chip select input
AGC	60	AGC time constant
VBIAS	61	preamplifier gain control voltage input
RDMUX	62	output of sampled and multiplexed auxiliary and main data signals
OUTX	63	auxiliary channel preamplifier output
MUXINX	64	auxiliary channel multiplexer input

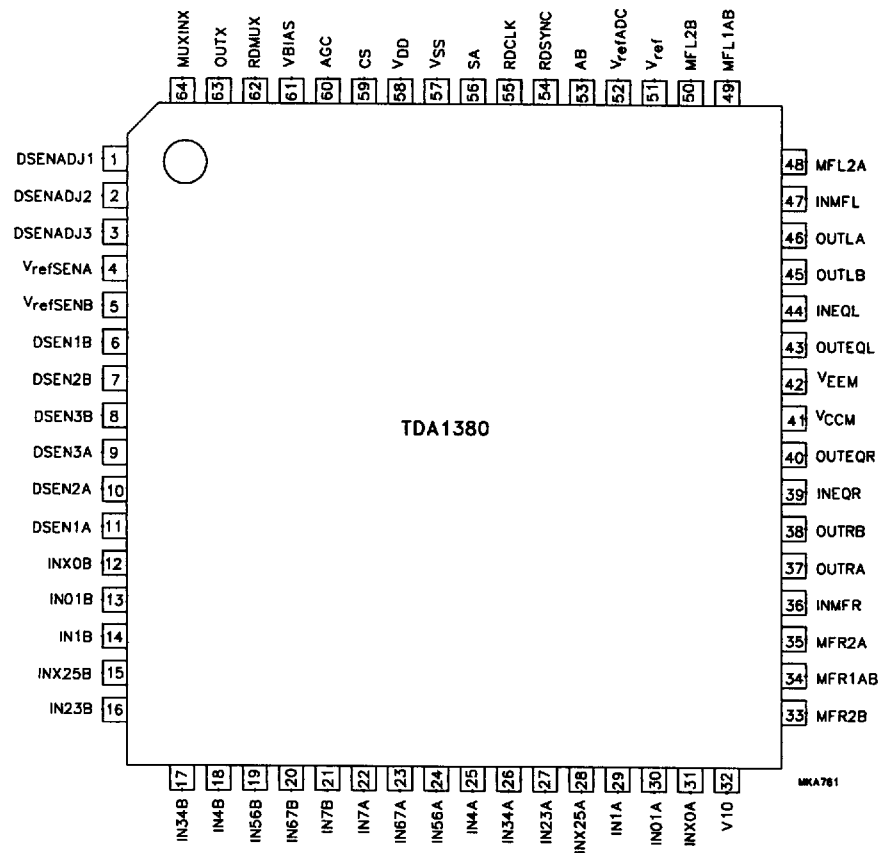


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

DCC data amplifiers and filters

The TDA1380 has 18 low-noise preamplifiers, which are connected to an 18-channel MRH. For each tape sector the MRH is partitioned into three strings of three heads (see Fig.11). Depending on the tape sector selection signal AB, nine preamplifiers for the A-sector, or nine preamplifiers for the B-sector of the tape are selected. Eight of the nine channels are for the DCC main data, and one for the auxiliary (AUX) data. The eight main data channels have pre-equalization for frequencies from 1 kHz up to 50 kHz (1st order highpass, –3 dB at 75 kHz), and lowpass filtering for anti-aliasing (2nd order active, –3 dB at 120 kHz). The AUX channel has a flat frequency response. The AUX data is continuously available at output OUTX. This output must be AC-coupled to the multiplexer input MUXINX. All inputs must be AC-coupled to the MRH. The inputs are internally biased at pin V10. The voltage at pin V10 is temperature dependent and is not intended for external use. Pin V10 has to be decoupled to the positive supply voltage (V_{DD}).

Automatic gain control

The DCC part is equipped with an AGC circuit which decreases the gain of the preamplifiers when the level at RDMUX exceeds a preset value. In this way an optimum voltage swing at the RDMUX output is obtained (for the ADC input of SAA2051, SAA2032, SAA2023 or SAA3323). The response time of the AGC can be set by an external capacitor connected to pin 60. There is a fixed relationship between the source and sink current at this pin, resulting in a fixed relationship between the decay time and the recover time of the preamplifier gain. The AGC is active only in the DCC mode and can be switched off by connecting pin 60 to V_{SS}.

Multiplexer

A multiplexing circuit switches the nine digital channels sequentially to the output. The AUX data is sampled during two clock periods, the eight main data channels are sampled during one clock period. The effective sample frequency is one tenth of the clock frequency at RDCLK. A timing overview is illustrated in Fig.4.

Analog amplifiers

For ACC playback the TDA1380 employs four DCC preamplifiers (per tape sector) for amplification of the left and right analog signals. Amplifiers CHX and CH0 are used for the left channel and CH4 and CH5 for the right channel. The buffered left and right channel outputs are available at four pins (see Table 1). Pins that carry no left and right channel signals will have a DC level V_A.

Table 1 ACC playback.

AB	TAPE SELECT	OUTLA	OUTLB	OUTRA	OUTRB	REMARKS
1	A	left	V_A	right	V_A	allows separate amplitude adjustment for sectors A and B
0	B	V_A	left	V_A	right	
1	A	left	note 1	right	note 1	allows one amplitude setting only for sectors A and B (DSP operation; high feedback operation)
0	B	left	note 1	right	note 1	

Note

1. At least one of OUTLB and OUTRB are externally connected to V_{DD}.

Feedback amplifiers

Two feedback amplifiers are available for driving a conductor in the MRH, thus providing magnetic feedback to improve the linearity of the analog audio response. In both the ACC and DCC mode, the feedback amplifiers are used for DC biasing of the MRH. The circuit principle of the feedback amplifiers is illustrated in Fig.9.

Equalization amplifiers

Two uncommitted operational amplifiers are available for pre-equalization of the left and right ACC outputs. These amplifiers are only operational during ACC playback. The non-inverting input is internally connected to a DC voltage which is approximately equal to V_{ref}. If the amplifiers are not used in the application, it is advised to connect the outputs to the inputs.

Current and voltage sources

Separate, adjustable low-noise current sources are available to provide the sense currents to the MRHs. The active current outputs are controlled by the mode switch (see Table 2). In the reference sense current mode, only one source is active (DSEN1B, pin 6). This current can be used for temperature measurement of the DCC head, thereby enabling control of the write current (TDA1381) when recording. The principle of the sense current sources is illustrated in Fig.8. The typical value of the output current is determined by resistors connected between the adjust pins and V_{SS}; where $I_{DSEN} = 0.33/R_{ADJUST}$.

The DC output voltages V_{ADC}, V_{ref}, V10, $V_{refSENA}$ and $V_{refSENB}$ are derived from an internal bandgap reference voltage source. The voltage V_{refADC} (referenced to V_{SS}) can be used as a reference voltage for analog-to-digital conversion of the RDMUX output.

Table 2 Sense current sources.

MODE	DIGITAL INPUTS(1)			AVAILABLE SENSE CURRENT	ACTIVE DC OUTPUTS
	CS	SA	AB		
Standby	0	1	0	–	–
Reference sense current	0	0	X	DSEN1B	–
Sense AB	0	1	1	DSEN1A; DSEN2A; DSEN3A DSEN1B; DSEN2B; DSEN3B	$V_{refSENA}$ $V_{refSENB}$
ACC playback A	1	1	1	DSEN1A; DSEN2A; DSEN3A	$V_{refSENA}$
ACC playback B	1	1	0	DSEN1B; DSEN2B; DSEN3B	$V_{refSENB}$
DCC playback A	1	0	1	DSEN1A; DSEN2A; DSEN3A	$V_{refSENA}$
DCC playback B	1	0	0	DSEN1B; DSEN2B; DSEN3B	$V_{refSENB}$

Note

1. Where X = don't care; 0 = LOW; 1 = HIGH.

Modes of operation

The amplifiers and sense current sources for the ACC and DCC parts can be switched ON/OFF separately by the mode switch signals CS, SA and AB. Also, a connection between OUTLB or OUTRB or both to V_{DD} is recognized as a single output ACC mode where the left and right outputs are present at OUTLA and OUTRA only.

Table 3 Modes of operation.

MODE	DIGITAL INPUT(1)			ACTIVE PARTS (see Fig.1)	ACTIVE DC REFERENCE OUTPUTS
	CS	SA	AB		
Standby	0	1	0		
Reference sense current	0	0	X	reference sense current source	V_{ref}
Sense AB	0	1	1	sense current sources	V_{ref}
ACC playback A/B	1	1	1 or 0	sense currents, data preamplifiers, AN, EQ and FB	V_{ref}; V10
ACC playback A/B via OUTLA and OUTRA only (note 2)	1	1	1 or 0	sense currents, data preamplifiers, AN, EQ and FB	V_{ref}; V10
DCC playback A/B	1	0	1 or 0	sense currents, data amplifiers and filters, multiplexer, AGC and FB	V_{ref}; V10; V_{refADC}
Test mode (note 3)	1	0	1 or 0	sense currents, data amplifiers and filters, multiplexer, AGC and FB	V_{ref}; V10; V_{refADC}

Notes

1. Where X = don't care; 0 = LOW; 1 = HIGH.
2. At least one of OUTLB or OUTRB are externally connected to V_{DD}.
3. INEQL or INEQR connected to V_{DD} (no user function).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to V_{SS} and V_{EEM}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	$V_{SS} = V_{EEM} = 0$ V	−0.3	5.5	V
V_{CCM}	supply voltage feedback amplifiers	$V_{SS} = V_{EEM} = 0$ V	−0.3	5.5	V
$V_{SS}-V_{EEM}$	difference in ground potential between pins 57 and 42		0	0	V
V_I	voltage input on any pin	$V_{DD} + 0.3 < 5.5$ V	−0.3	$V_{DD} + 0.3$	V
$I_{I(max)}$	maximum supply current (pins 41, 42, 57 and 58)		−	±120	mA
I_{FBmax}	maximum current for feedback amplifiers (pins 33 to 35 and 48 to 50)		−	±80	mA
$I_{sense(max)}$	maximum current on sense current source (pins 1 to 3 and 6 to 11)		−	±30	mA
$I_{n(max)}$	maximum current on any other pin		−	±10	mA
P_{tot}	total power dissipation		−	650	mW
T_{amb}	operating ambient temperature		−30	+85	°C
T_{stg}	storage temperature		−65	+50	°C
V_{es}	electrostatic handling		−3000	+3000	V

ELECTROSTATIC HANDLING

Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	60	K/W

CHARACTERISTICS

$V_{DD} = V_{CCM} = 3$ V; $V_{SS} = V_{EEM} = 0$ V; $T_{amb} = 25$ °C; $f_{clk} = 3.072$ MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	3.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers		2.7	3.0	5.5	V
I_{DDDCC}	supply current DCC mode	CS = 1; SA = 0	18	27	37	mA
I_{DDACC}	supply current ACC mode	CS = 1; SA = 1	16	23	30	mA
I_{DDRS}	supply current reference sense current mode	CS = 0; SA = 0	0.6	1.2	1.6	mA
I_{DDAB}	supply current sense AB mode	CS = 0; SA = 1; AB = 1	1.5	2.7	3.7	mA
I_{CCM}	supply current feedback amplifiers	CS = 1	7.5	12	17.5	mA
$I_{DDstb} + I_{CCM}$	supply current standby mode	CS = 0; AB = 0; SA = 1	–	0.2	0.3	mA
V_{refADC}	reference voltage for ADC	CS = 1; SA = 0; $R_L = 1$ kΩ	1.95	2.05	2.15	V
$V_{refSENA}$	sense A reference voltage	CS = 1; AB = 1; $I_O < 5$ µA; $I_{DSEN} = 10$ mA	1.0	1.1	1.2	V
$V_{refSENB}$	sense B reference voltage	CS = 1; AB = 0; $I_O < 5$ µA; $I_{DSEN} = 10$ mA	1.0	1.1	1.2	V
V_{ref}	reference voltage output	$I_O < 5$ µA; all modes except standby mode	1.18	1.25	1.32	V
V10	reference voltage for DCC inputs	CS = 1; $I_O < 5$ µA	0.9	1.0	1.1	V
DCC part						
DATA AMPLIFIERS, CHANNELS 0 TO 7; NOTE 1						
G_{50}	gain at 50 kHz		72	75	78	dB
ΔG_{10}	relative gain at 10 kHz	note 2	−14	−12	−10	dB
G_{100}	gain at 100 kHz		71	76	79	dB
ΔG_{300}	relative gain at 300 kHz	note 2	−22	−12	−3	dB
$V_{n(ref)}$	input referred noise voltage	$f_i = 50$ kHz; $R_{source} = 70$ Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 × standard deviation of input referred noise voltage	$f_i = 50$ kHz; $R_{source} = 70$ Ω	–	0.5	–	nV/√Hz
THD	total harmonic distortion	$f_i = 10$ kHz; $V_{62} = 0.35$ V (RMS)	–	−40	−30	dB
$Z_{i(d)}$	input impedance differential mode		–	7	–	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$Z_{i(c)}$	input impedance to V_{SS} common mode		–	7.5	–	kΩ
α_{CS}	channel separation	f_i = 10 kHz	30	40	–	dB
SVRR	supply voltage ripple rejection	f_i = 50 kHz; note 3	–	–20	–	dB
Auxiliary amplifier, channel X; note 1						
G_{63}	gain at OUTX (pin 63)	100 Hz to 100 kHz	43	46	49	dB
G_{62}	gain at RDMUX (pin 62)	100 Hz to 100 kHz; note 4	56	59	62	dB
$V_{n(ref)}$	input referred noise voltage	f_i = 50 kHz; R_{source} = 70 Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 x standard deviation input referred noise voltage	f_i = 50 kHz; R_{source} = 70 Ω	–	0.5	–	nV/√Hz
$V_{o(rms)}$	maximum output voltage (pin 63) (RMS value)	f_i = 10 kHz	0.35	–	–	V
THD	total harmonic distortion	f_i = 10 kHz; V_{63} = 0.35 V (RMS)	–	–40	–30	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz; note 3	–	–3	–	dB
$R_{L(DC)}$	DC load at pin 63	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load at pin 63	load connected to V_{SS}	–	–	100	pF
Output buffer, RDMUX (pin 62)						
$V_{62(rms)}$	maximum output voltage (RMS value)	R_L = 2 kΩ	0.35	–	–	V
V_{DC}	DC voltage level at pin 62		0.95	1.15	1.35	V
$\Delta V_{DC(os)}$	DC offset voltage between sampled outputs	note 5	–	–	200	mV
$R_{L(DC)}$	DC load at pin 62	load connected to V_{SS}	1.5	–	–	kΩ
$C_{L(AC)}$	AC load at pin 62	load connected to V_{SS}	–	–	100	pF
t_{set}	settling time of sampled outputs	C_L = 50 pF; within 10 mV	–	100	150	ns
$V_{62(M)}$	AGC detector level (peak value)	note 5	320	465	570	mV
AGC_{CR}	AGC control range		9	11	13	dB
I_{source}	AGC source current (pin 60)		16	21	26	µA
I_{sink}	AGC sink current (pin 60)		0.3	0.5	0.8	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Select logic inputs (RDCLK and RDSYNC) and mode switch inputs (CS, SA and AB)						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
I_{IL}	input leakage current		–2	0	+2	µA
C_I	input capacitance	note 7	–	–	10	pF
t_{su}	set-up time for RDSYNC	see Fig.3	35	–	–	ns
t_h	hold time for RDSYNC	see Fig.3	35	–	–	ns
t_r	rise time for RDCLK	see Fig.3	–	–	50	ns
V_{det}	ACC single output mode detection level (pins 38 and 45)		$V_{DD} - 0.45$	$V_{DD} - 0.35$	–	V
Sense current sources						
$I_{DSENmin}$	minimum output current	note 8	–	–	1	mA
$I_{DSENmax}$	maximum output current	note 8	20	–	–	mA
I_{DSEN1B}	reference sense current (pin 6)	note 9	2.7	3.0	3.3	mA
I_{ON}	output current noise	note 10	–	20	–	pA/√Hz
Z_{DSEN}	output impedance	note 10	20	–	–	kΩ
V_{DSEN}	DC voltage level of current outputs (pins 6 to 11)		1.0	–	–	V
ACC part						
ACC AMPLIFIERS						
G_{ACC}	ACC gain	20 Hz to 20 kHz	44	46	48	dB
$V_{n(ref)}$	input referred noise voltage	f_i = 10 kHz; R_{source} = 70 Ω	–	2.0	–	nV/√Hz
$\Delta V_{n(ref)}$	3 x standard deviation of input referred noise voltage	f = 10 kHz; R_{source} = 70 Ω	–	0.5	–	nV/√Hz
$V_{o(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.35	–	–	V
V_A	DC output voltage	see Table 1	0.6	0.9	1.2	V
THD	total harmonic distortion	f_i = 1 kHz; V_o = 0.35 V (RMS)	–	–40	–30	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz	–	tbf	–	dB
α_{CS}	channel separation	f_i = 1 kHz	40	–	–	dB
$R_{L(DC)}$	DC load (pins 37, 38 45 and 46)	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load (pins 37, 38 45 and 46)	load connected to V_{SS}	–	–	300	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Equalization operational amplifiers (EQ); note 11						
$V_{EQ(rms)}$	maximum output voltage (RMS value)	f_i = 1 kHz	0.35	–	–	V
B_{EQ}	bandwidth	at –3 dB	50	–	–	kHz
THD	total harmonic distortion	f_i = 1 kHz; V_O = 0.35 V (RMS)	–	–70	–55	dB
α_{CS}	channel separation	f_i = 1 kHz	60	–	–	dB
$R_{L(DC)}$	DC load at OUTEQL	load connected to V_{SS}	10	–	–	kΩ
$C_{L(AC)}$	AC load at OUTEQL	load connected to V_{SS}	–	–	300	pF
Feedback amplifiers (FB); note 12						
I_{FBmax}	maximum output current (RMS value)	f_i = 1 kHz	25	–	–	mA
THD	total harmonic distortion	f_i = 1 kHz; I_{FB} = 25 mA (RMS)	–	–60	–50	dB
B_{FB}	bandwidth	at –3 dB	50	–	–	kHz
V_{IFB}	DC voltage level input (pins 36 and 47)		–	1.15	–	V

Notes

1. AGC off (maximum gain; pin 60 connected to V_{SS}).
2. Gain relative to gain at f_i = 50 kHz (see Fig.5).
3. Heads connected according to the circuit of Fig.11 (see also Fig.6 for typical supply rejection).
4. OUTX AC-coupled to MUXINX via 100 nF capacitor.
5. The difference between minimum and maximum DC voltage level at the outputs of the data channels. To be measured at RDMUX.
6. Measured with continuous sine wave of 10 kHz at RDMUX, multiplexer in a fixed position. A 1 V (p-p) sine wave corresponds to a multiplexed DCC signal of 1.25 V (p-p).
7. Periodically sampled, not tested.
8. Pins 6 to 11. The output current is inversely proportional to the value of the resistor connected between the adjust pin DSENADJ1, DSENADJ2, DSENADJ3 and V_{SS}. A resistor of 33 Ω will give 10 mA (typ.) sense current. Other currents can be calculated: 0.33 V/R_{ADJUST}.
9. CS = 0, SA = 0; Resistor of 33 Ω connected between DSENADJ1 and V_{SS}. Typical reference sense current is 100 mV/R_{ADJUST}.
10. From 10 to 100 kHz, IDSEN = 10 mA, a 10 µF capacitor connected between $V_{refSENA}$ and V_{SS}, a 10 µF capacitor connected between $V_{refSENB}$ and V_{SS}.
11. Closed loop configuration, unity gain, in accordance with Fig.10.
12. Closed loop, unity gain, R_L = 25 Ω, in accordance with Fig.9.

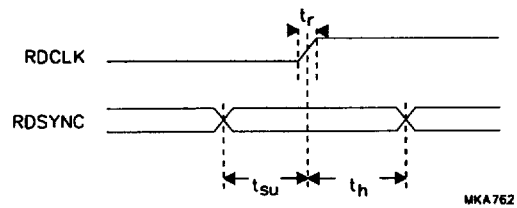


Fig.3 Timing relationship between edges of RDCLK and RDSYNC.

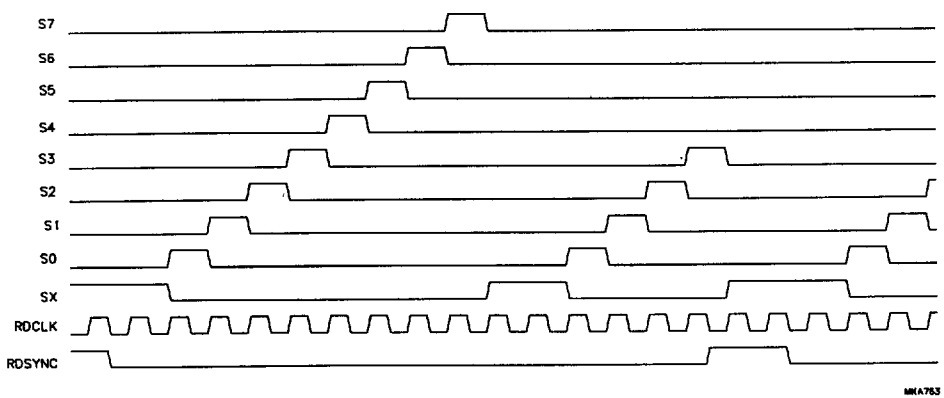


Fig.4 Multiplexer timing diagram.

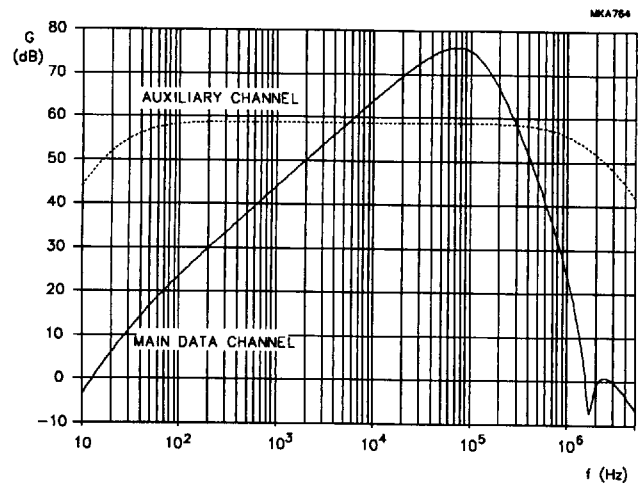


Fig.5 Typical gain of the auxiliary and main data channel (AGC off).

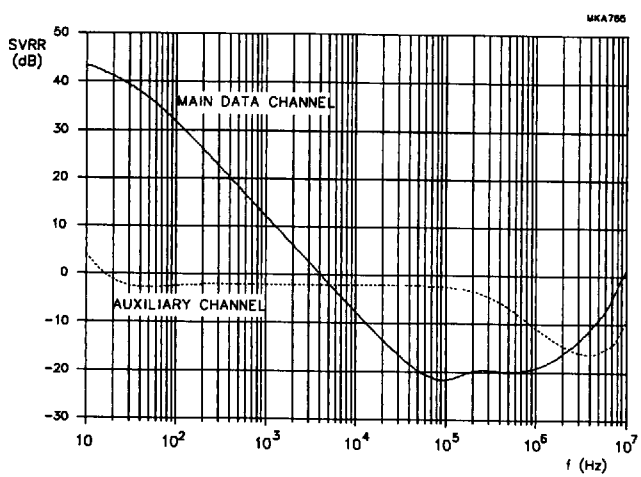


Fig.6 Typical supply rejection of the auxiliary and main data channel (AGC off).

TEST AND APPLICATION INFORMATION

The TDA1380 can be set to the TEST mode by connecting INEQL or INEQR (or both) to V_{DD}. In this mode the switch at pin MUXINX enables monitoring of the input stage and lowpass filter of each data amplifier and also allows input to the highpass filters and following stages. The test multiplexer operates in phase with the output multiplexer. Measurement of the gain of the data channels can be performed in two steps: step 1, gain from the inputs to MUXINX; step 2, gain from MUXINX to RDMUX.

Figure 7 illustrates how to use pin MUXINX in the TEST mode, $C_L < 20$ pF, $R_L > 100$ kΩ, $C_i > 47$ nF and $R_{bias} = 1$ kΩ. The DC voltage, when driving MUXINX, should be 0.7 V higher than the measured DC level of the preamplifier output in order to shut off the emitter follower.

The impedance of the sense current source outputs can be measured from the difference in sense current when applying different voltages to the sense current output. This voltage can vary from 1 V to V_{DD}. Figure 8 illustrates the principle of the sense current sources.

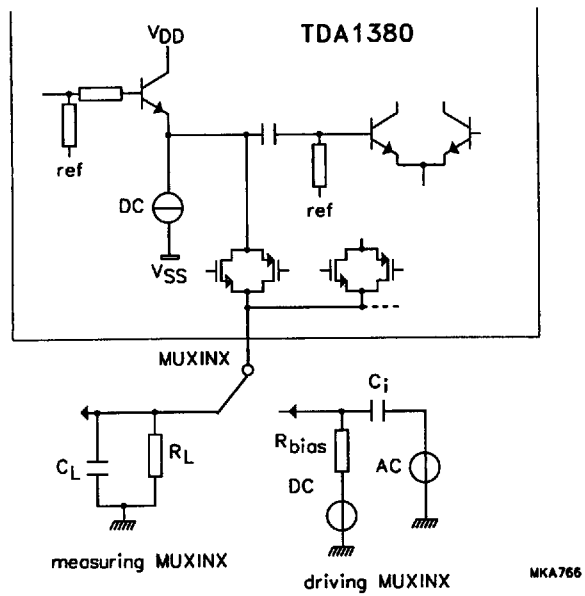


Fig.7 Use of the MUXINX pin in the TEST mode.

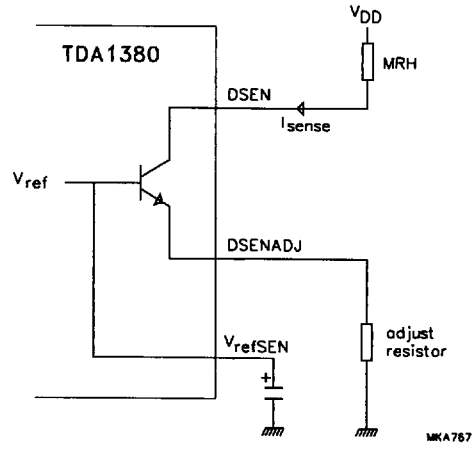


Fig.8 Principle of the sense current sources.

The feedback amplifiers consist of three operational amplifiers providing one input and a differential output with respect to an internal 1.15 V reference. The active output A or B is selected by the tape sector selection signal AB.

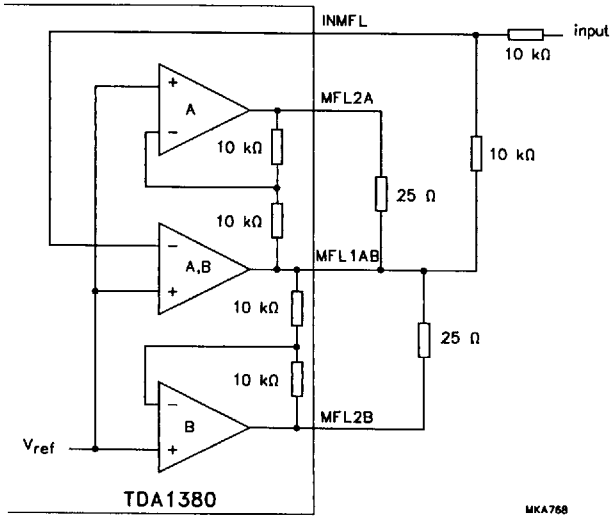


Fig.9 Principle of the feedback amplifiers and TEST circuit.

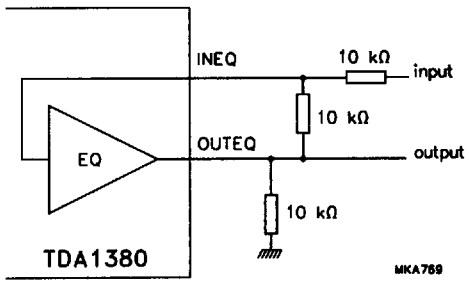


Fig.10 Test circuit of the equalization amplifiers.

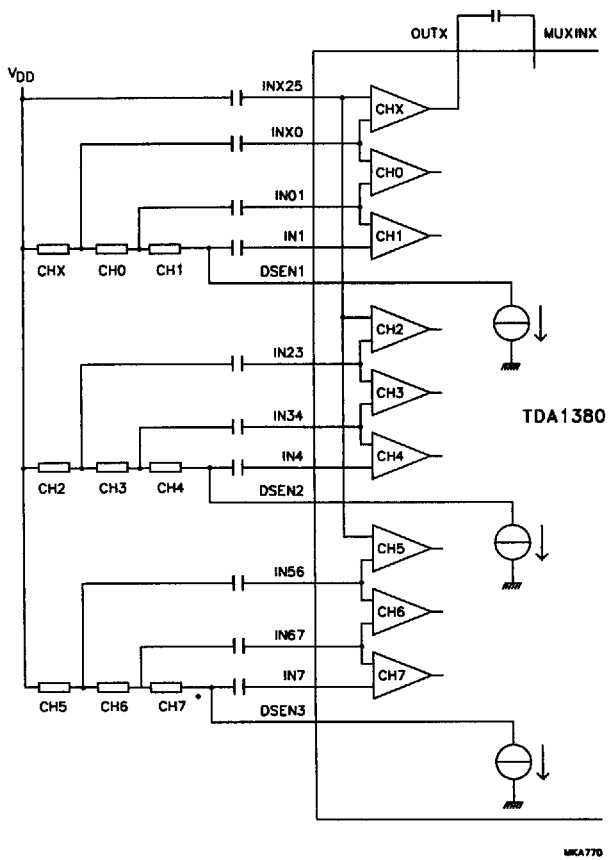
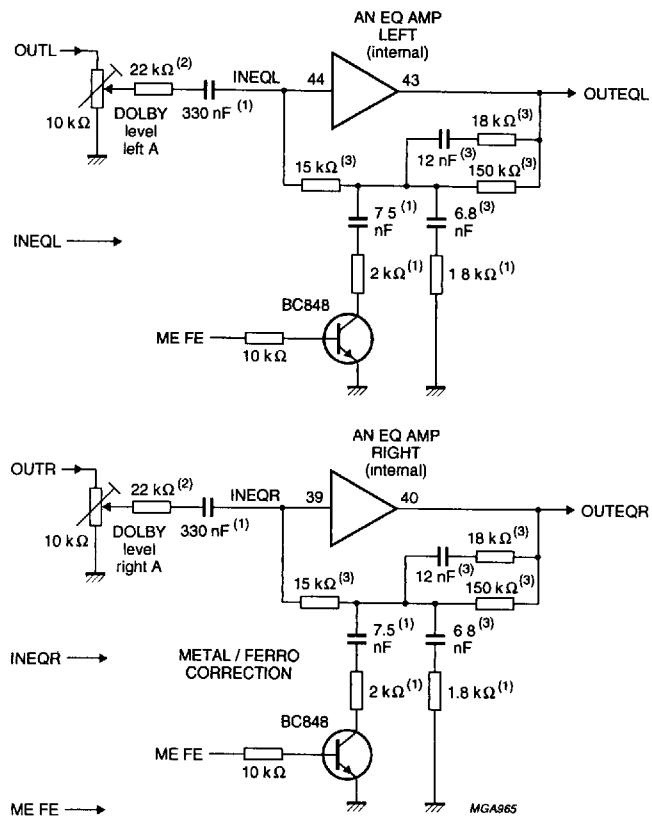


Fig.11 Connection of the TDA1380 to the MRH (partial).



Frequency compensation values are totally dependent on head frequency response characteristics.

(1) Less than 10%

(2) Less than 5%

(3) Less than 2%

Fig.12 Analog equalizer.

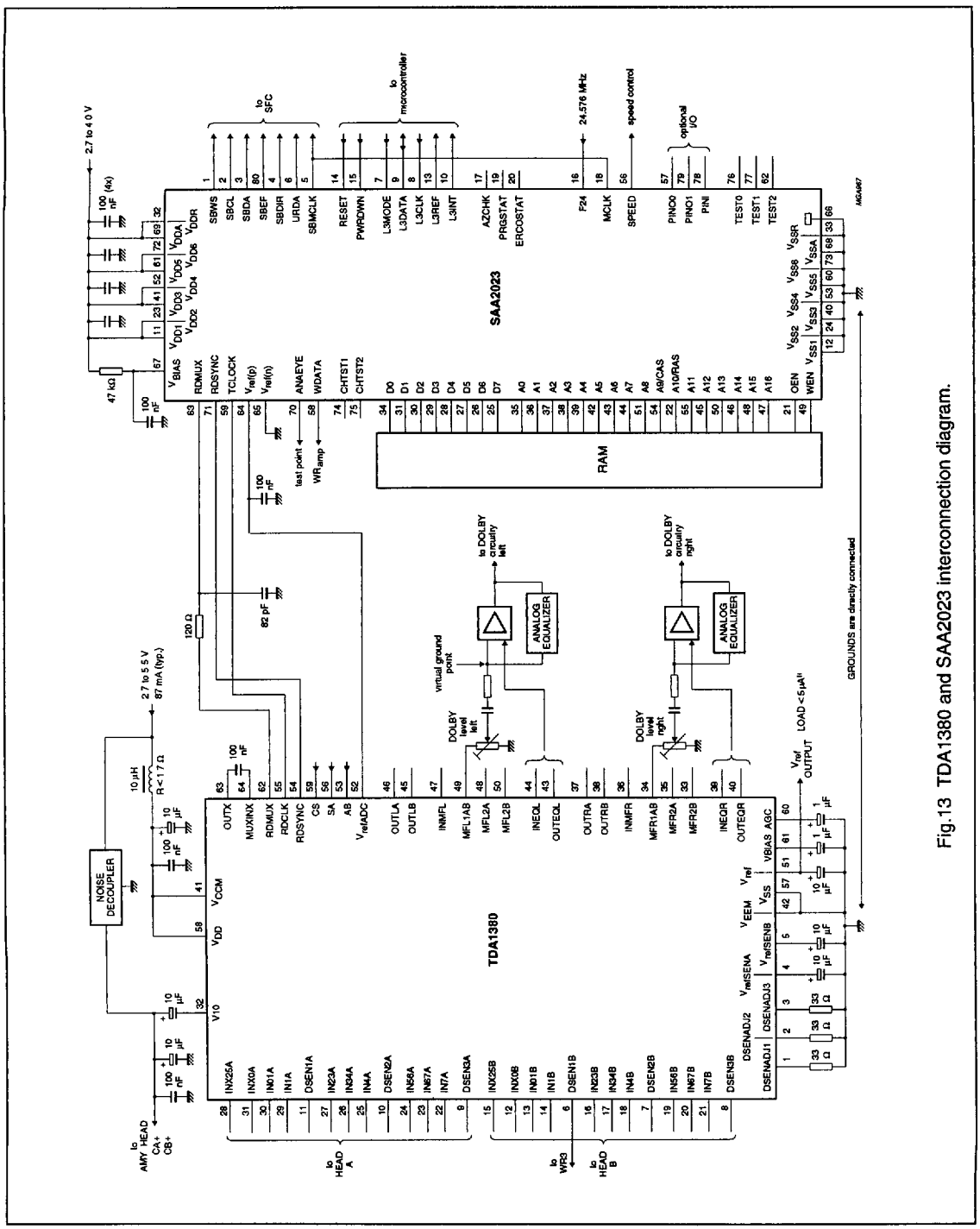
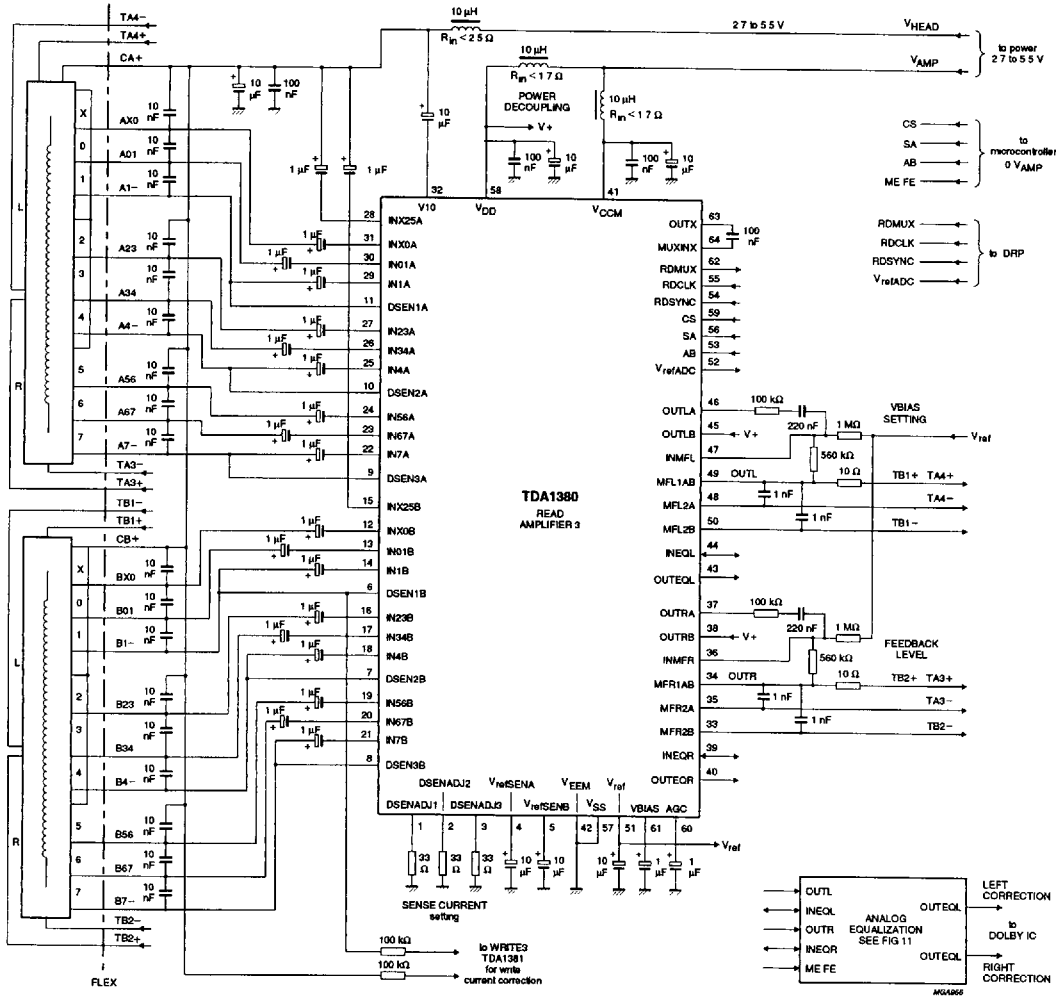


Fig.13 TDA1380 and SAA2023 interconnection diagram.



Power V_{HEAD} and power V_{AMP} have to be very clean in the frequency range 0 to 1 kHz.
With respect to power consumption:

(1) V_{HEAD}; $3 \times I_{sense} \times V_{HEAD}$.

(2) V_{AMP}; ≤ 42 mA at 3 V

(3) START-UP I_{peak}, 150 mA at V_{HEAD}.

Fig.14 Application diagram.