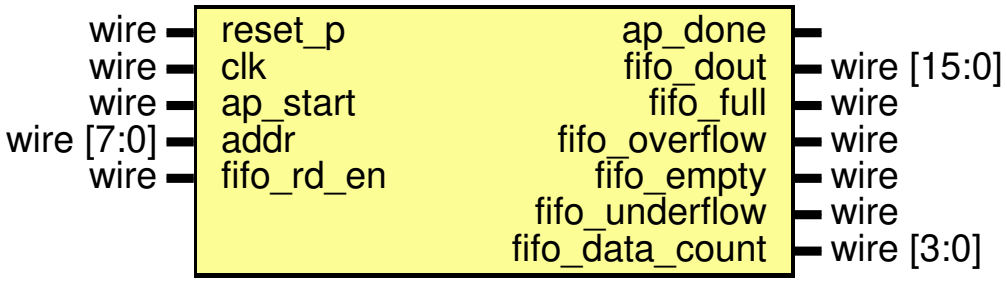
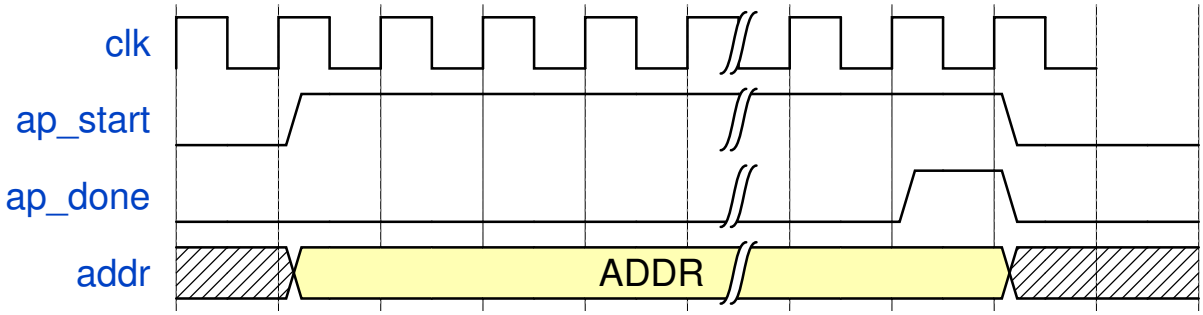
Entity: credit_07

Diagram



Description

Example for complex credit



Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
reset_p	input	wire	1 - reset
clk	input	wire	clock
ap_start	input	wire	1 - start of transaction
ap_done	output		1 - transaction done
addr	input	wire [7:0]	address in the RAM_0
fifo_rd_en	input	wire	1 - read data from output FIFO
fifo_dout	output	wire [15:0]	Data from output FIFO
fifo_full	output	wire	1 - output FIFO is full
fifo_overflow	output	wire	1 - writing to full FIFO is fixed
fifo_empty	output	wire	1 - output FIFO is empty
fifo_underflow	output	wire	1 - reading from empty FIFO is fixed
fifo_data_count	output	wire [3:0]	Data count in the output FIFO

Signals, constants and types

Signals

Name	Type	Description

rstp	logic	
rstp_z	logic [3:0]	
stp	logic [3:0]	
transaction_enable	logic	
transaction_start	logic	
credit_cnt	logic [7:0]	
ram1_n	logic [3:0]	
ram1_n_vld	logic	
ram1_d	logic [15:0]	
ram1_d_vld	logic	

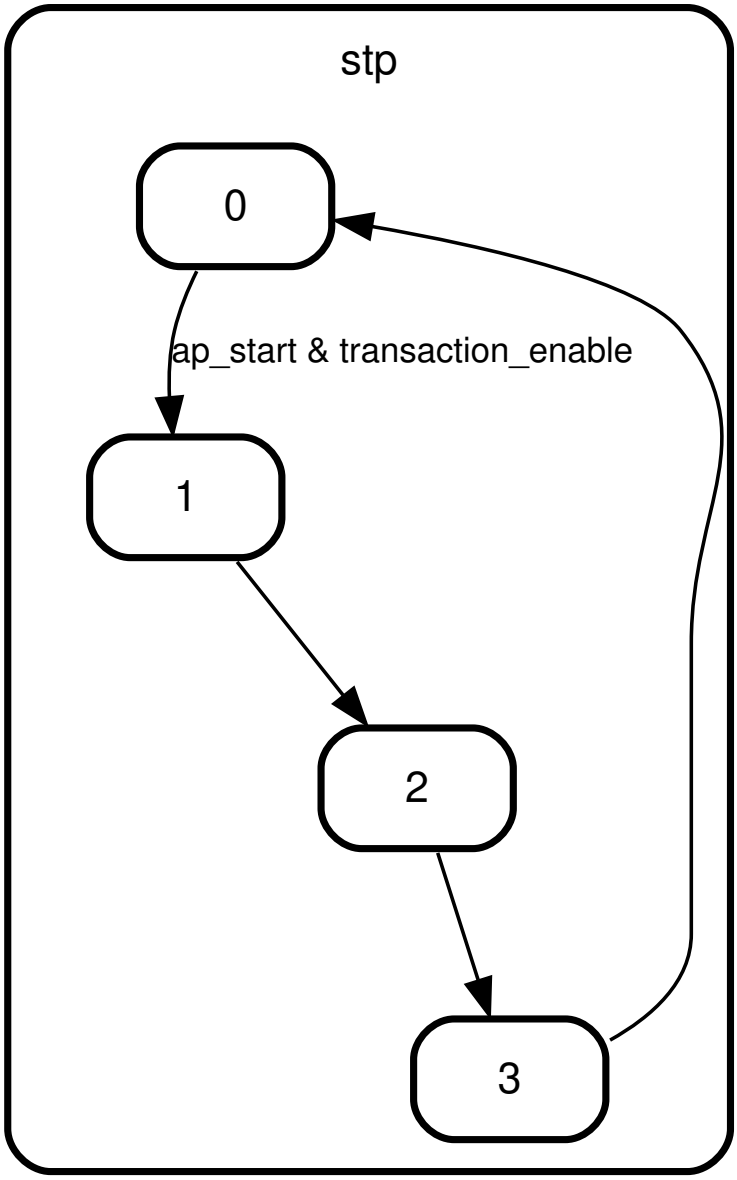
Processes

- **unnamed**: ***(@(posedge clk))***
- **unnamed**: ***(@(posedge clk))***

Instantiations

- **fifo**: fifo_32x16fw

State machines


stp
0
ap_start & transaction_enable
1
2
3