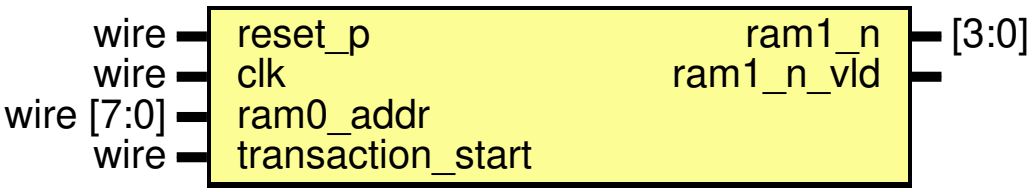
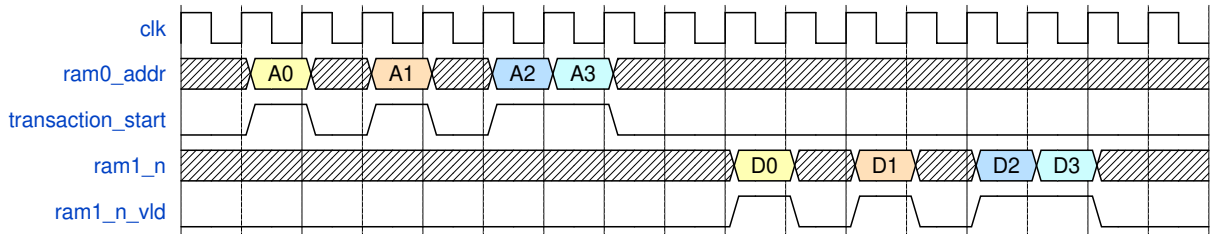
Entity: cr_ram0

Diagram



Description

RAM0 - imitaor



Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
reset_p	input	wire	1 - reset
clk	input	wire	clock
ram0_addr	input	wire [7:0]	address of word
transaction_start	input	wire	1 - start of transaction
ram1_n	output	[3:0]	Numbers of words for read from RAM1
ram1_n_vld	output		1 - valid data on ram1_n

Signals, constants and types

Signals

Name	Type	Description
rstp	logic	
mem	integer	
data_z0	logic [3:0]	
data_z1	logic [3:0]	
data_z2	logic [3:0]	
data_vld_z0	logic	
data_vld_z1	logic	
data_vld_z2	logic	

Processes

- **unnamed**: ***(@ (posedge clk))***