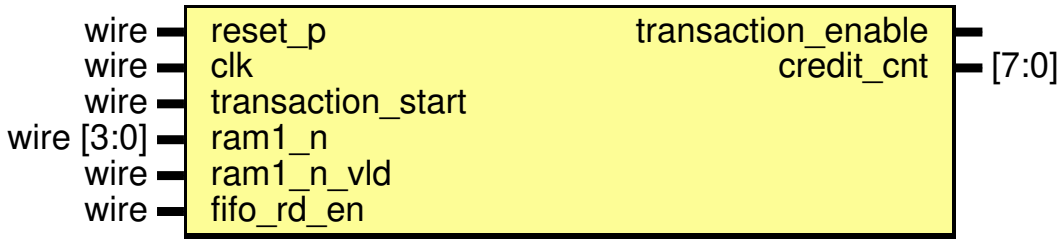
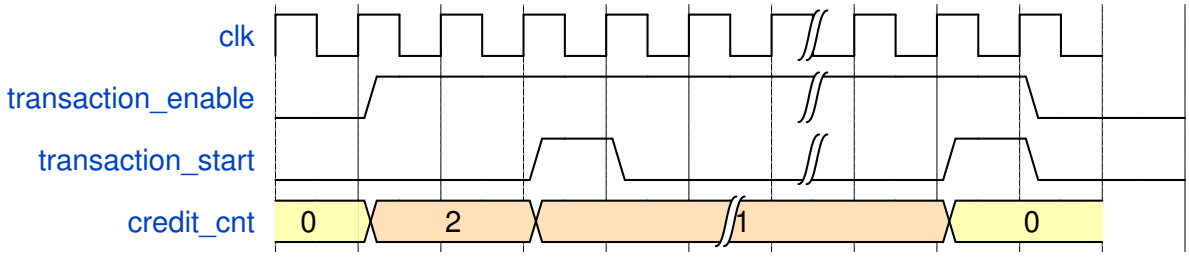
Entity: cr_cnt

Diagram



Description

Credit conter



Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
reset_p	input	wire	1 - reset
clk	input	wire	clock
transaction_enable	output		1 - credit is avaliabled, transaction is enabled
transaction_start	input	wire	1 - start of transaction
ram1_n	input	wire [3:0]	Numbers of words for read from RAM1
ram1_n_vld	input	wire	1 - valid data on ram1_n
fifo_rd_en	input	wire	1 - read data from output FIFO
credit_cnt	output	[7:0]	count of avaliable credits

Signals, constants and types

Signals

Name	Type	Description
rstp	logic	
stp	logic [3:0]	
cnt	logic [7:0]	
delta	logic [7:0]	

Processes

- **unnamed**: ***(@(posedge clk))***
- **unnamed**: ***( )***
- **unnamed**: ***(@(posedge clk))***