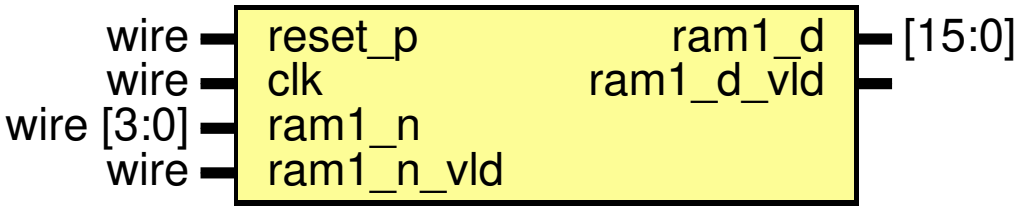
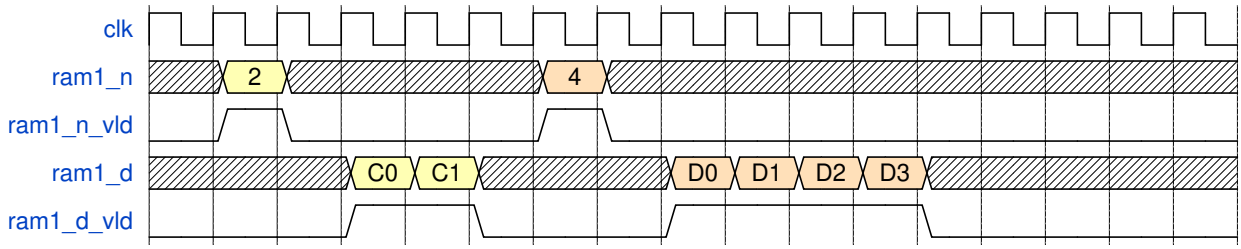
Entity: cr_ram1

Diagram



Description

RAM1 - imitator



Generics and ports

Table 1.1 Generics

Table 1.2 Ports

Port name	Direction	Type	Description
reset_p	input	wire	1 - reset
clk	input	wire	clock
ram1_n	input	wire [3:0]	Numbers of words for read from RAM1
ram1_n_vld	input	wire	1 - valid data on ram1_n
ram1_d	output	[15:0]	Data from RAM1
ram1_d_vld	output		1 - valid data on ram1_d

Signals, constants and types

Signals

Name	Type	Description
rstp	logic	
data_z0	logic [15:0]	
data_z1	logic [15:0]	
data_z2	logic [15:0]	
data_vld_z0	logic	
data_vld_z1	logic	
data_vld_z2	logic	
pkg_cnt	integer	

Processes

- **unnamed**: ***(@ (posedge clk))***