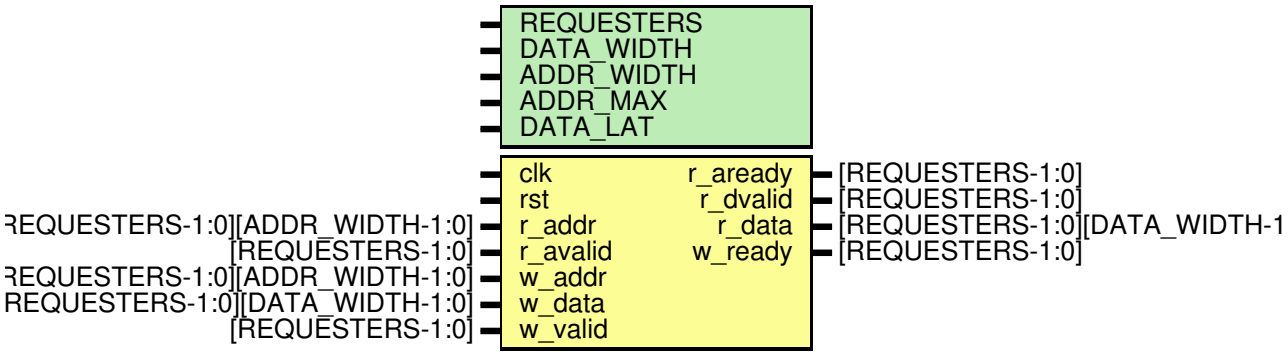
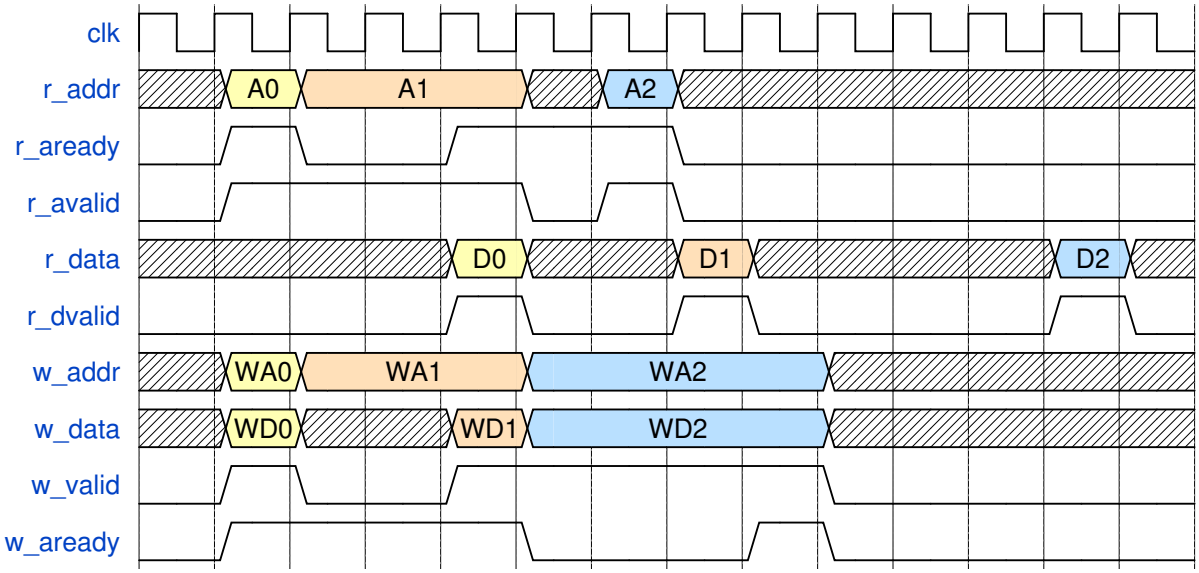
# Entity: multimemory

## Diagram




## Description

Template module for multibank memory




## Generics and ports

### Table 1.1 Generics

| Generic name | Type | Value | Description |
|---|---|---|---|
| REQUESTERS | | 3 | Number of ports |
| DATA_WIDTH | | 32 | Width of data bus |
| ADDR_WIDTH | | 4 | Width of address bus |
| ADDR_MAX | | undefined | 2 ^ ADDR_WIDTH -1 - maximum of address |
| DATA_LAT | | 2 | ( >1 ) delay in cycles between data request and data output |

### Table 1.2 Ports

| Port name | Direction | Type | Description |
|---|---|---|---|
| clk | input | | Clock |
| rst | input | | 1 - reset |
| r_addr | input | [REQUESTERS-1:0][ADDR_WIDTH-1:0] | Address for read request |
| r_avalid | input | [REQUESTERS-1:0] | 1 - request for read |

| | | | |
|---|---|---|---|
| r_aready | output | [REQUESTERS-1:0] | 1 - avaliable for read request |
| r_dvalid | output | [REQUESTERS-1:0] | 1 - valid answer for read request |
| r_data | output | [REQUESTERS-1:0][DATA_WIDTH-1:0] | answer for read request |
| w_addr | input | [REQUESTERS-1:0][ADDR_WIDTH-1:0] | Address for write request |
| w_data | input | [REQUESTERS-1:0][DATA_WIDTH-1:0] | Data for write request |
| w_valid | input | [REQUESTERS-1:0] | 1 - request for write |
| w_ready | output | [REQUESTERS-1:0] | 1 - avaliable for write request |

# Signals, constants and types

## Constants

| Name | Type | Value | Description |
|---|---|---|---|
| ADDR_MAX | | undefined | 2 ^ ADDR_WIDTH -1 - maximum of address |
| DATA_LAT | | 2 | ( >1 ) delay in cycles between data request and data output |