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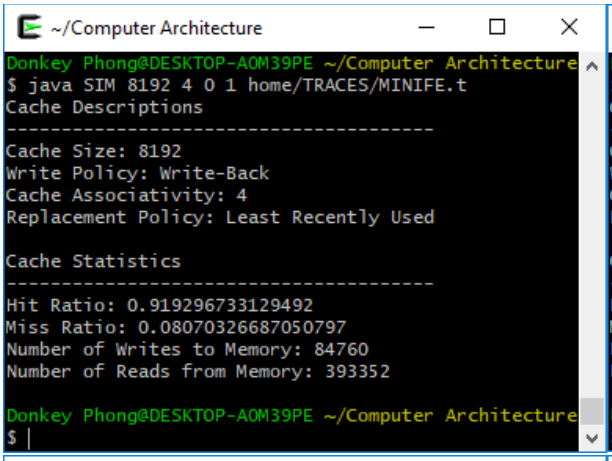
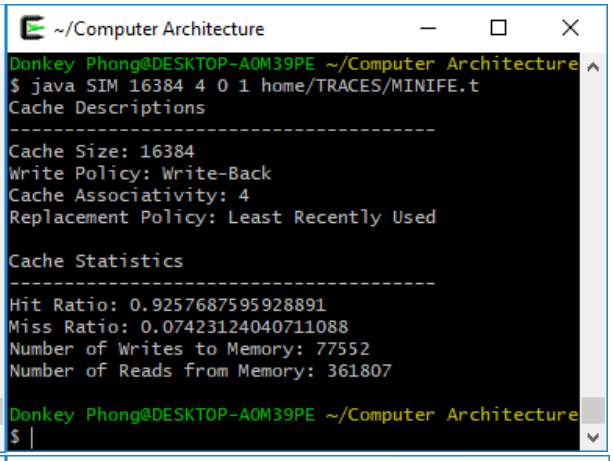
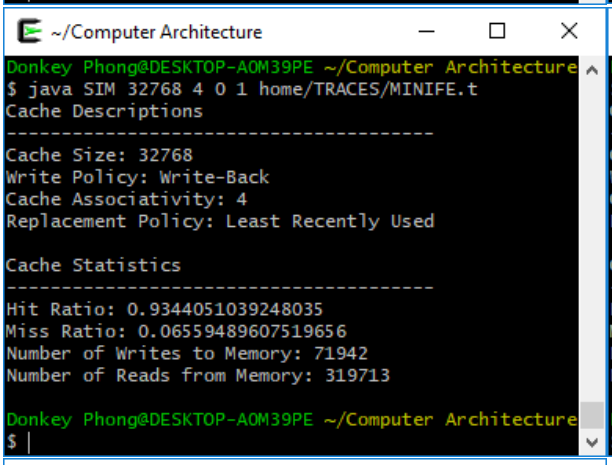
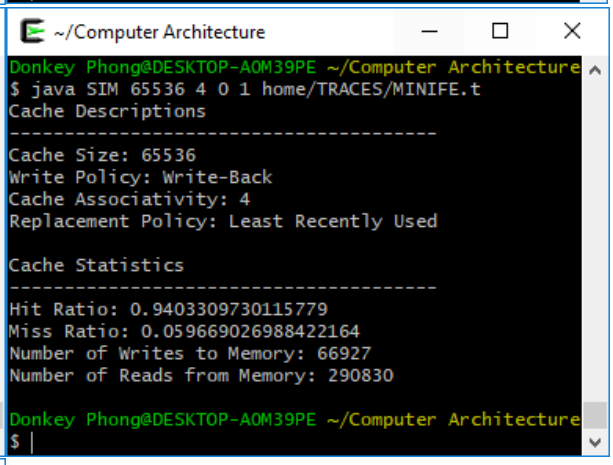
Part A:

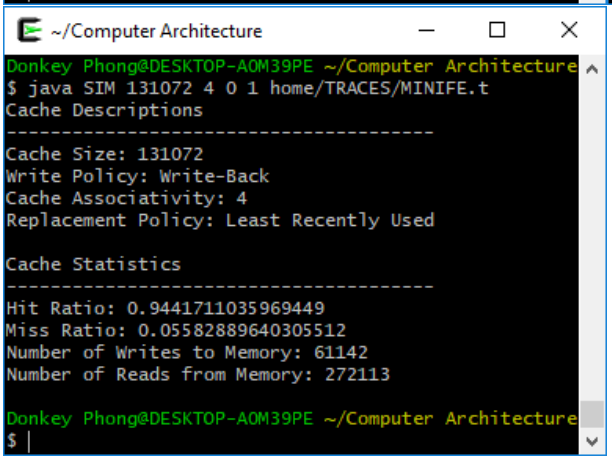
MiniFE:











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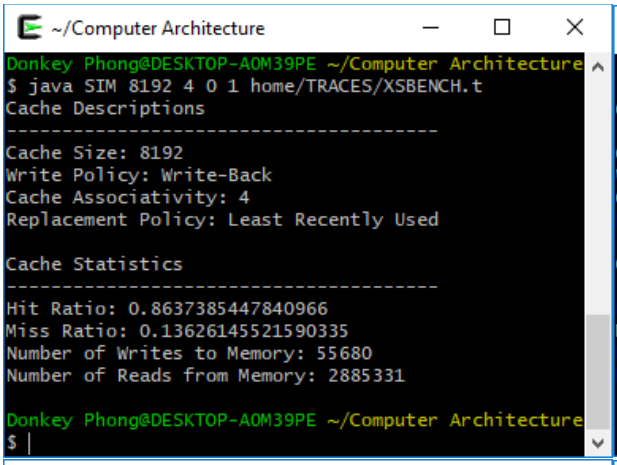
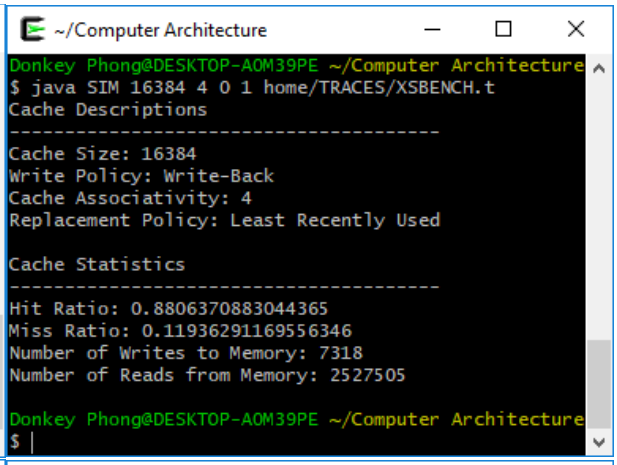
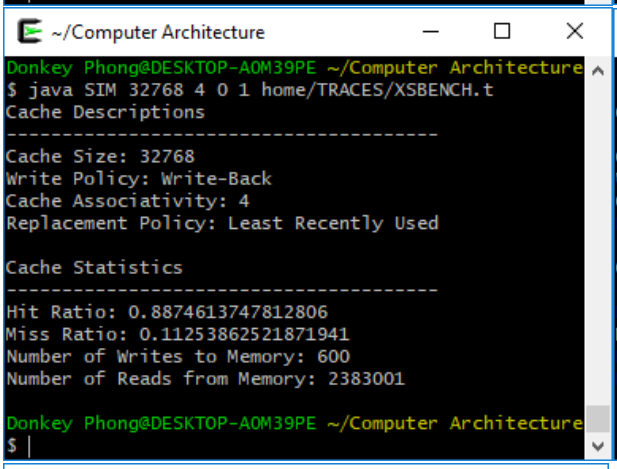
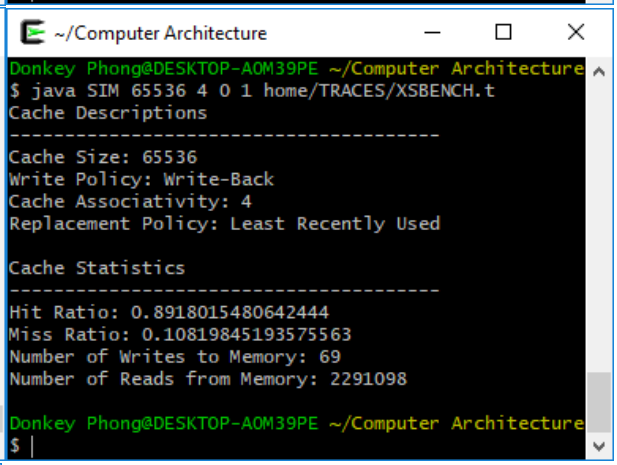
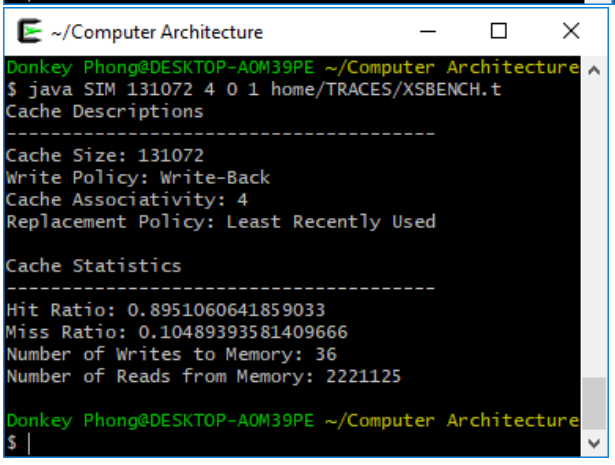
XSBench:











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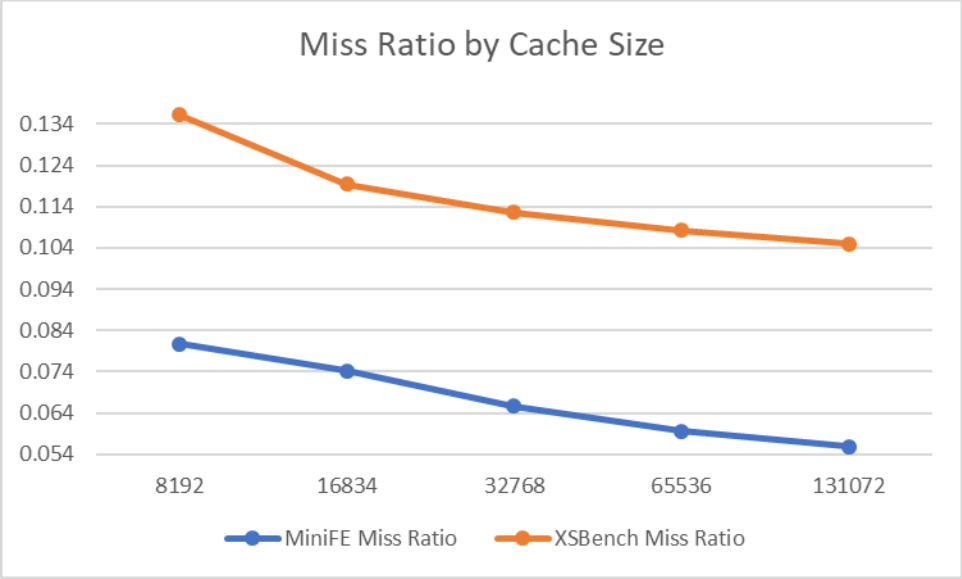

Looking at the trends for the miss ratio of both MiniFE and XSBench, the miss ratio decreases as the cache size is increased. The number of hits increases while the number of misses decreases as the size of the cache increases. This is probably due to having more rows to access to.

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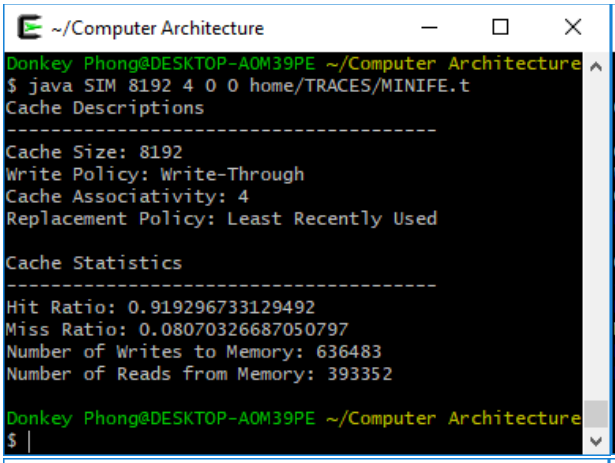
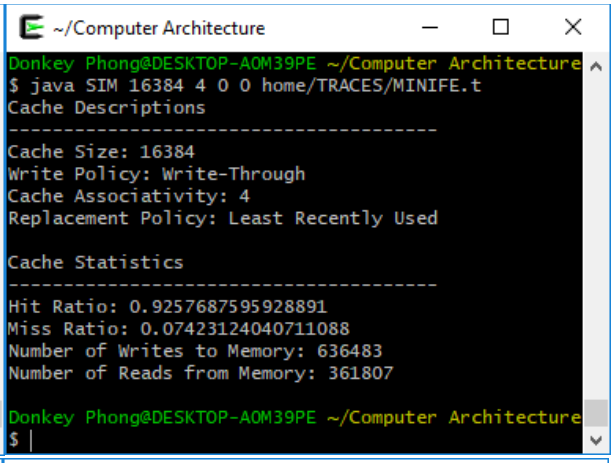
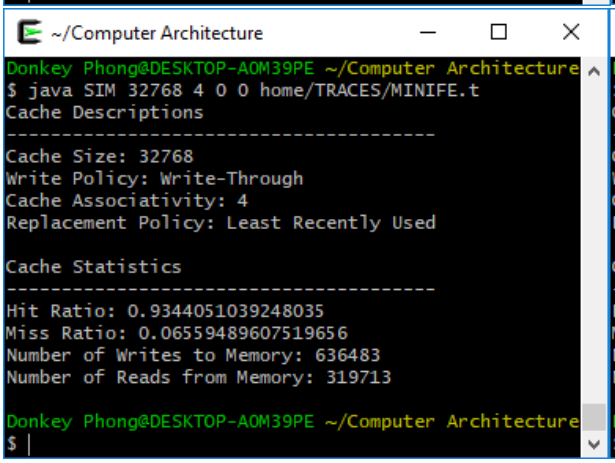
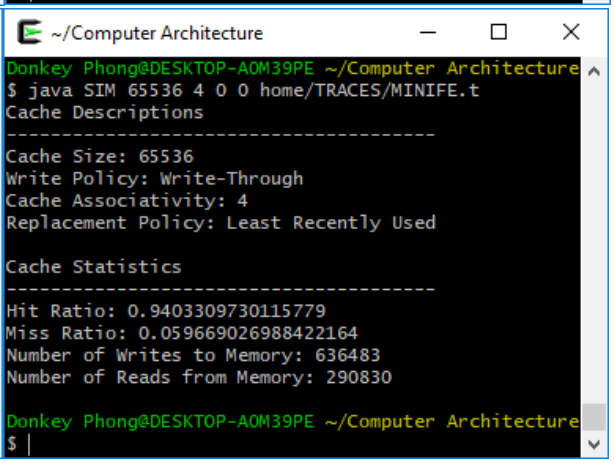
Part B:

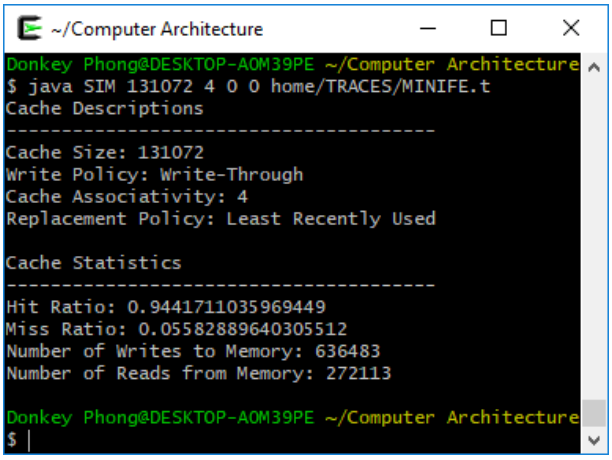
MiniFE:











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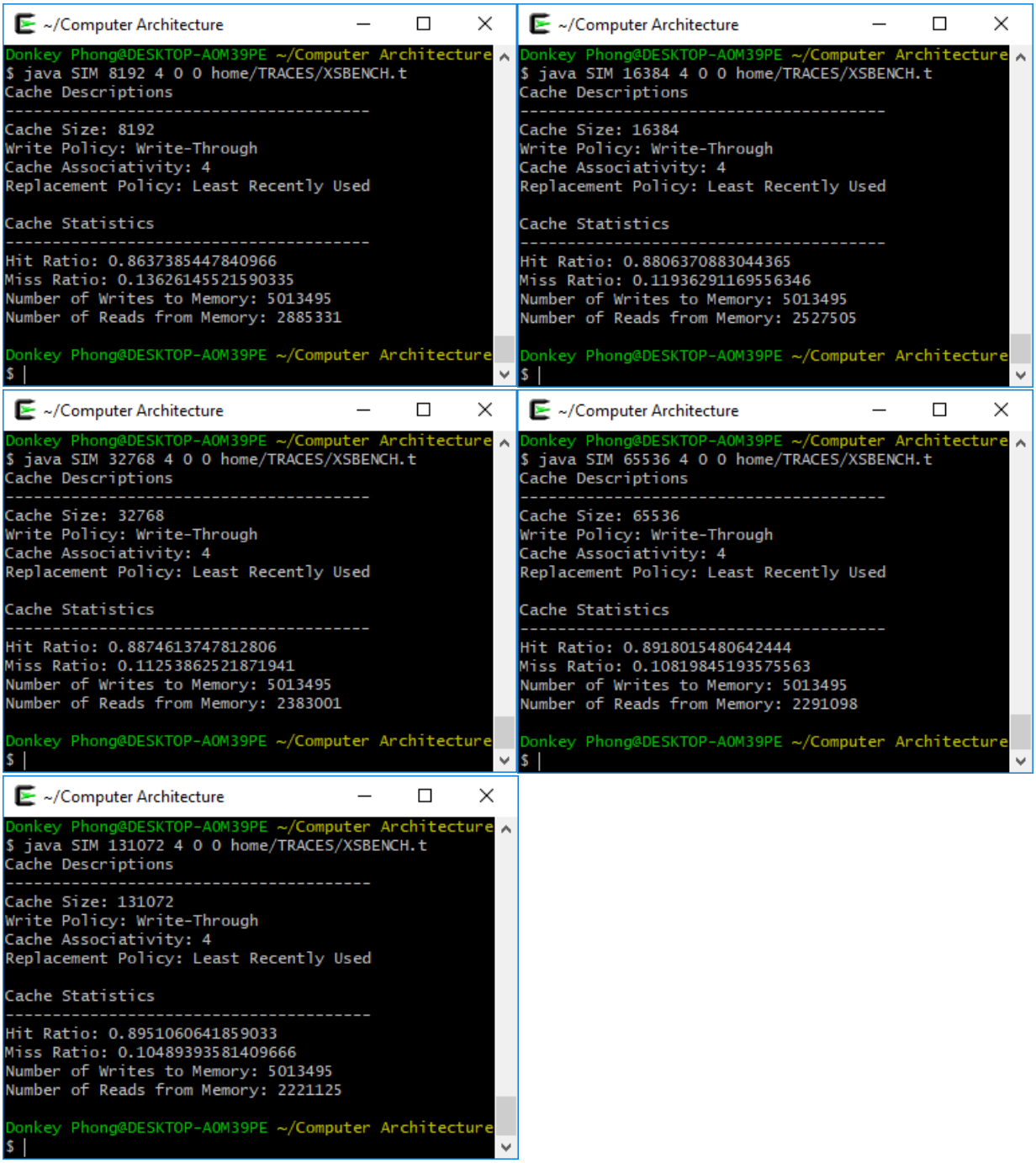
XSBench:



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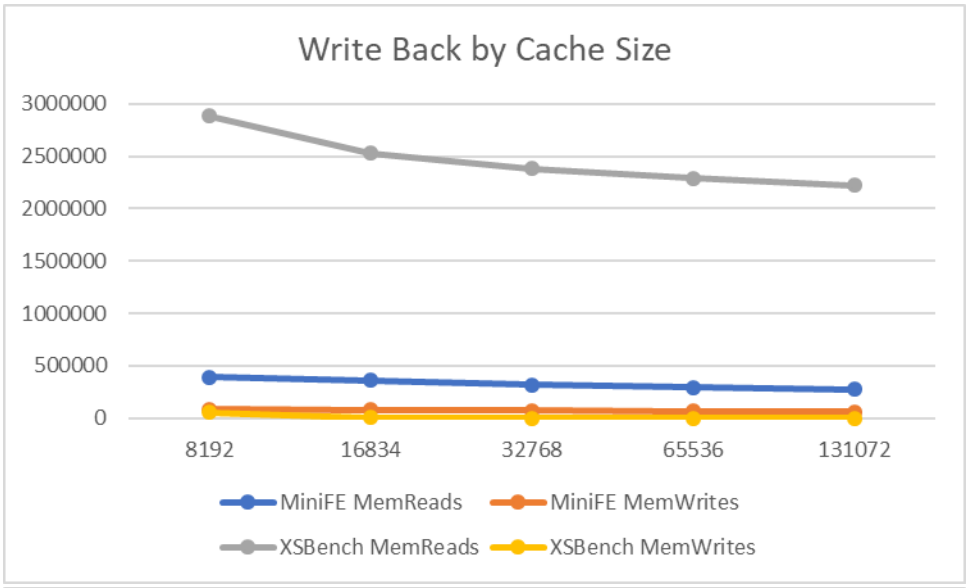

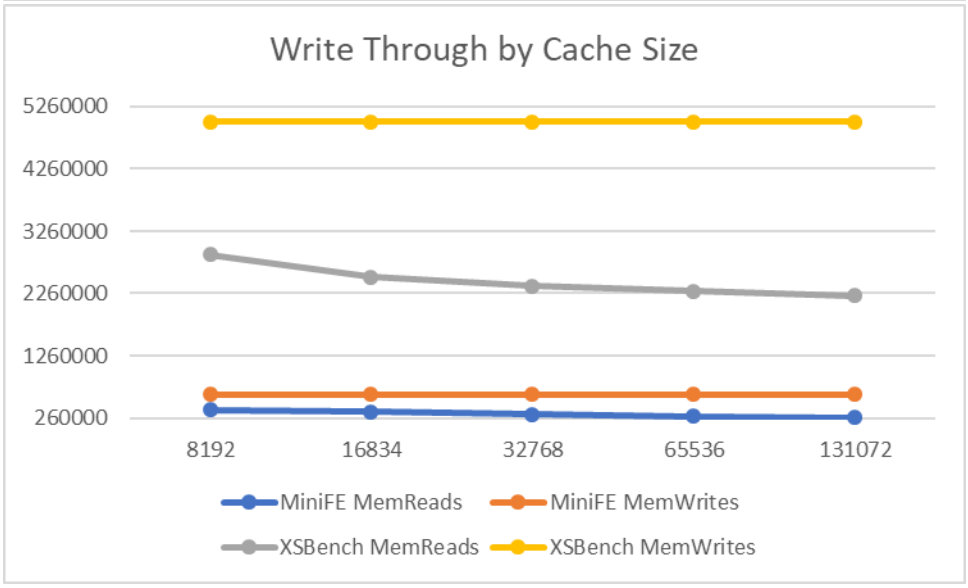

There seems to be more memory writes for a write through than write back. The only thing that drastically changes is the XSBench's memory writes going by the write back and write through trends. The amount of writes and reads decreases as the cache size increases. This is probably due to having more hits and less misses.

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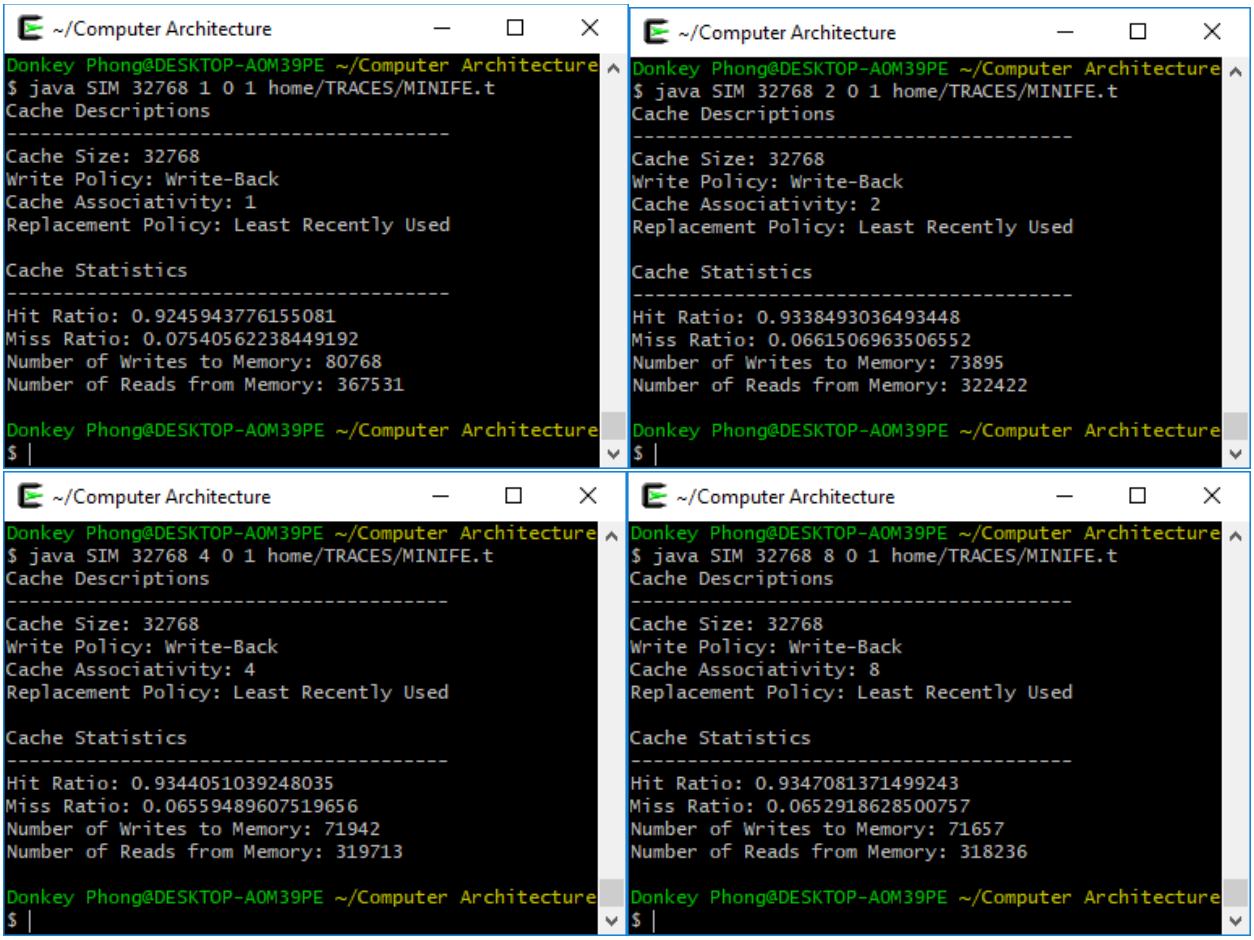
Part C:

MiniFE:



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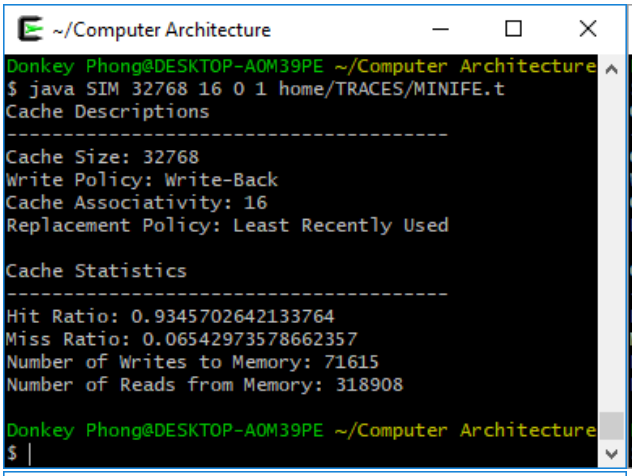

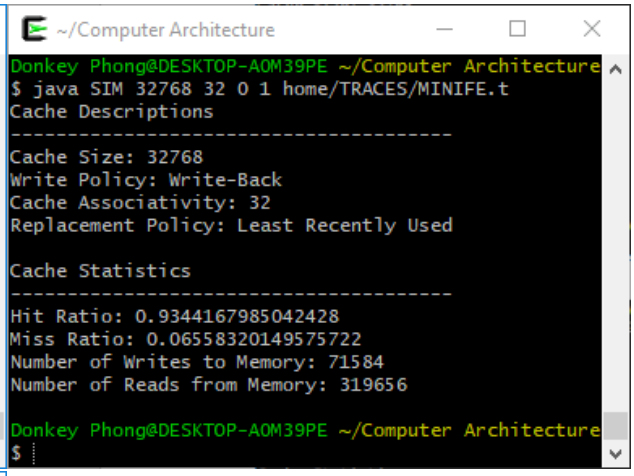

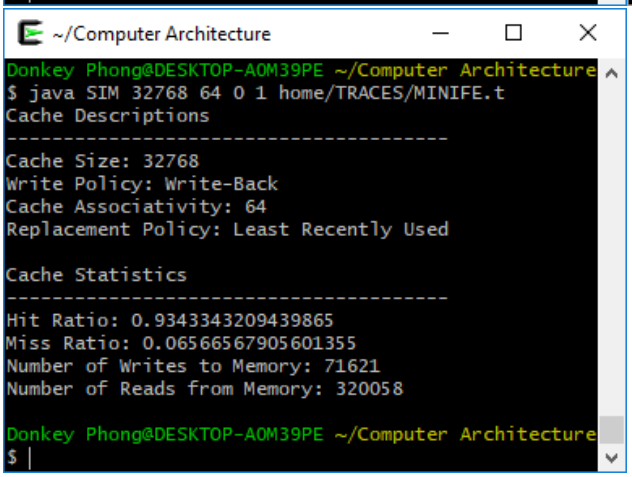

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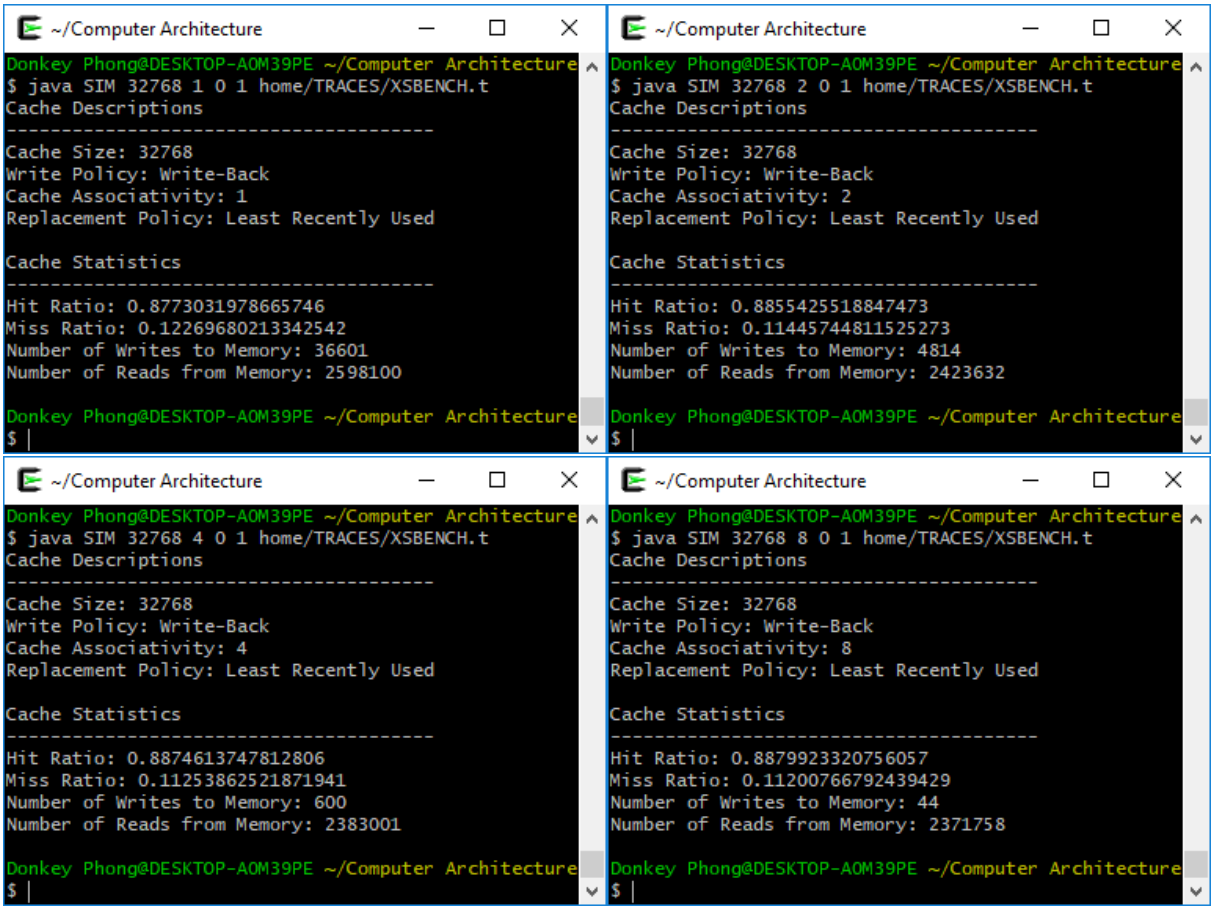
XSBench:



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~/Computer Architecture

```
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 16 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
---------------------------------------
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 16
Replacement Policy: Least Recently Used

Cache Statistics
---------------------------------------
Hit Ratio: 0.8880944810240736
Miss Ratio: 0.11190551897592634
Number of Writes to Memory: 35
Number of Reads from Memory: 2369595

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$
```

~/Computer Architecture

```
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 32 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
---------------------------------------
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 32
Replacement Policy: Least Recently Used

Cache Statistics
---------------------------------------
Hit Ratio: 0.8882158035615745
Miss Ratio: 0.11178419643842555
Number of Writes to Memory: 35
Number of Reads from Memory: 2367026

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$
```

~/Computer Architecture

```
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 64 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
---------------------------------------
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 64
Replacement Policy: Least Recently Used

Cache Statistics
---------------------------------------
Hit Ratio: 0.888246783547795
Miss Ratio: 0.11175321645220504
Number of Writes to Memory: 35
Number of Reads from Memory: 2366370

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$
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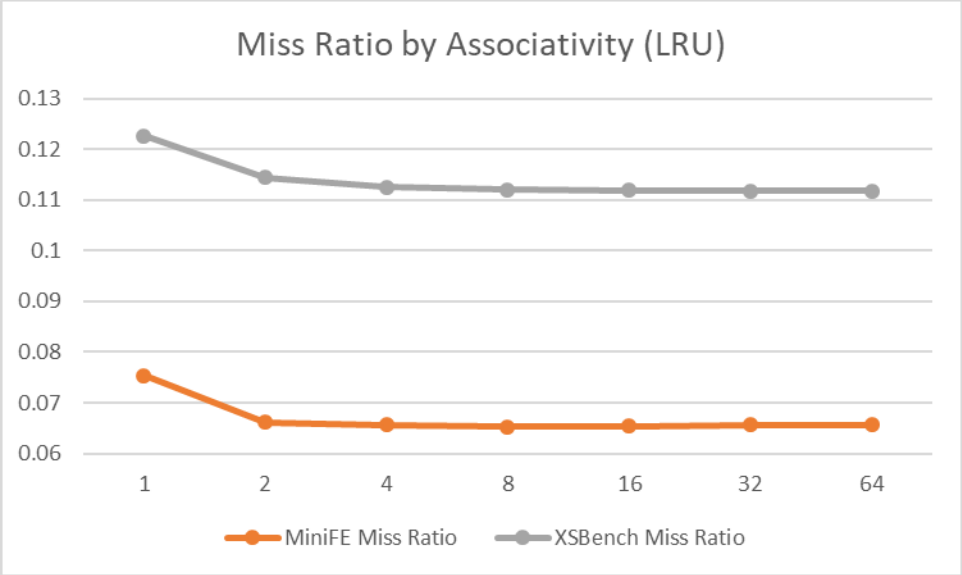

Miss ratio decreases as associativity approaches 8 but then increases slightly after 8 making a bell curve like trend for MiniFE. Miss ratio keeps decreasing after 8 for XSBench. This is probably due to XSBench having more hits than misses.

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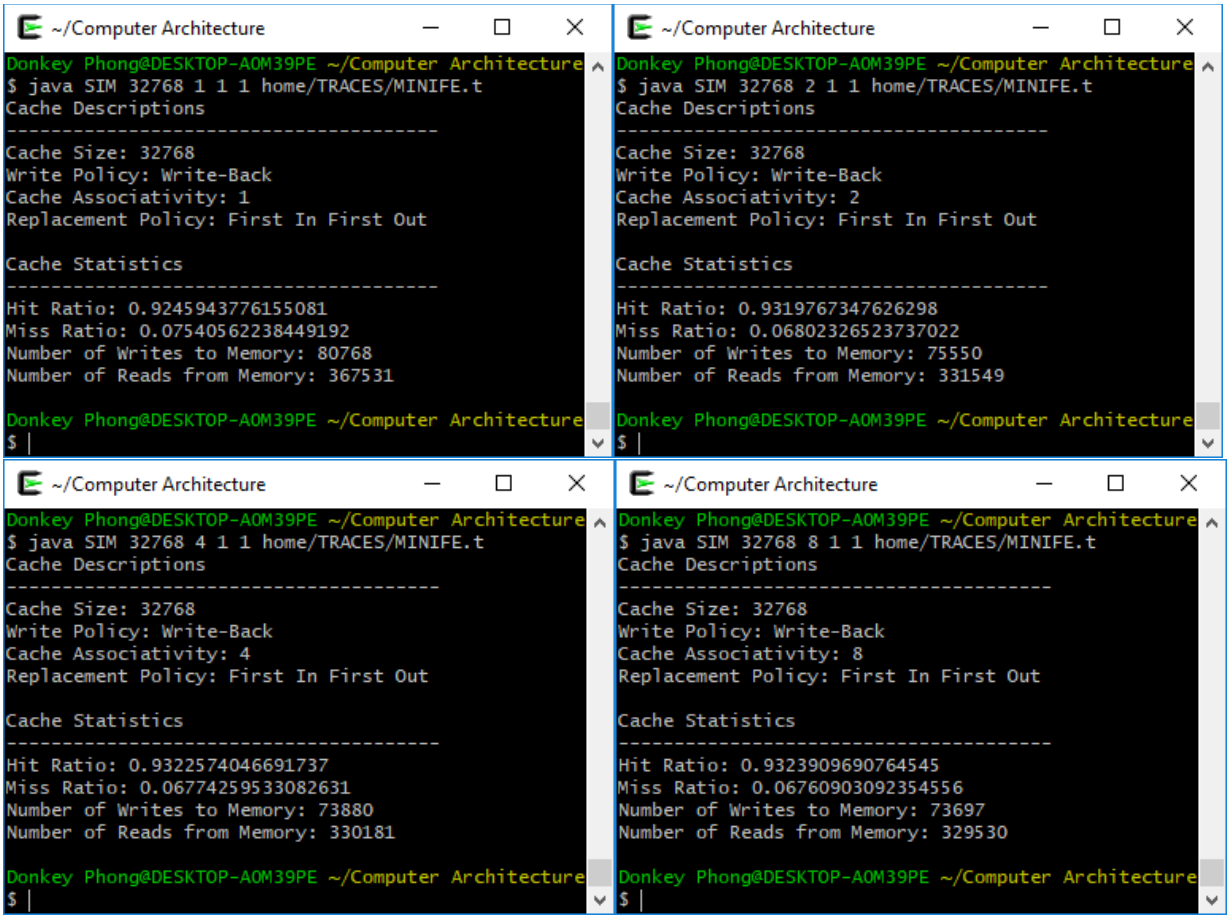
Part D:

MiniFE:



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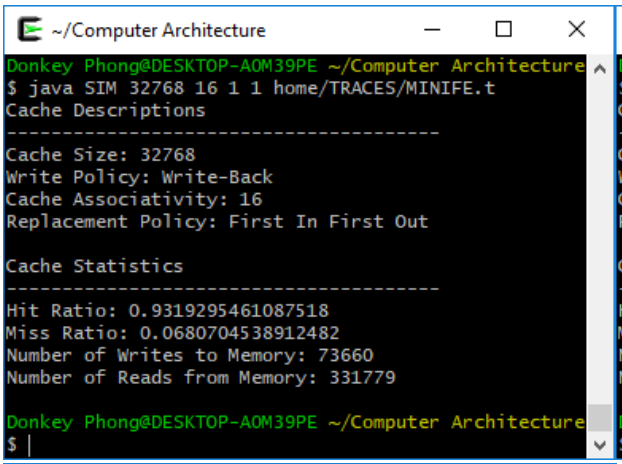

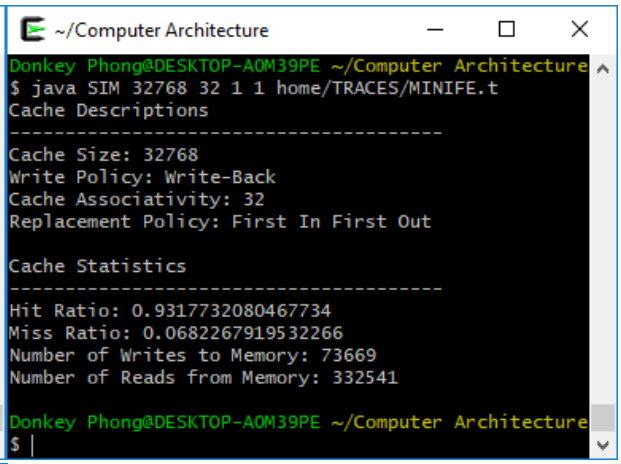

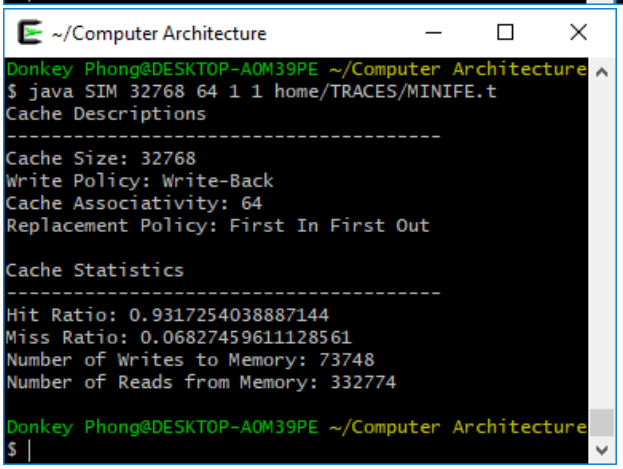

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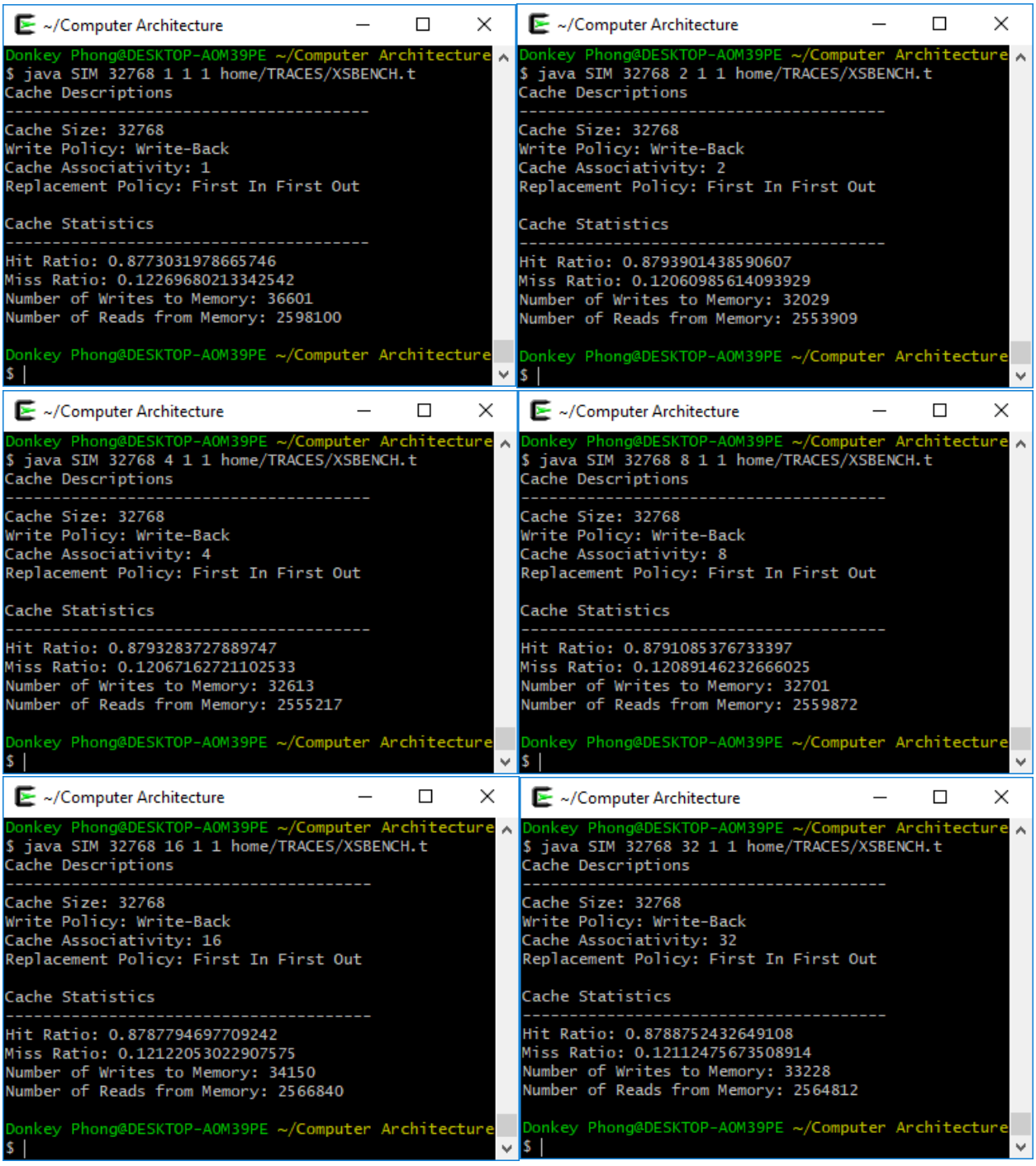
XSBench:



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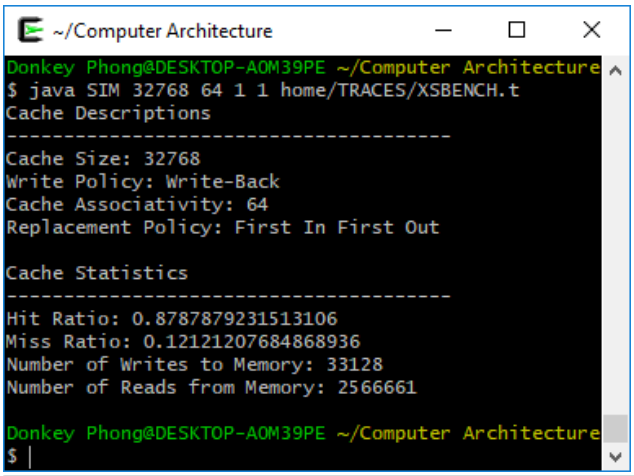

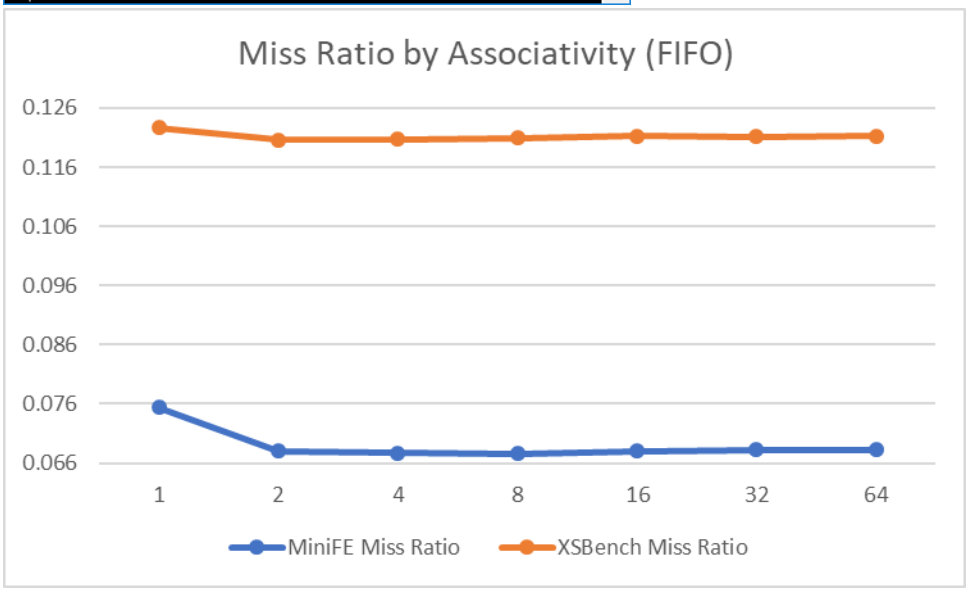

Comparing the miss ratio for both FIFO and LRU, LRU seems to be better for getting less miss ratio but with a chance of having more if the cache size is increased. The miss ratio for FIFO seems to be consistent after associativity of 1. Both LRU and FIFO have the same miss ratio at associativity of 1.