

Phong Nguyenho
Ph094398

Part A:

MiniFE:

<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 8192 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 8192 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.919296733129492 Miss Ratio: 0.08070326687050797 Number of Writes to Memory: 84760 Number of Reads from Memory: 393352 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 16384 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 16384 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9257687595928891 Miss Ratio: 0.07423124040711088 Number of Writes to Memory: 77552 Number of Reads from Memory: 361807 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9344051039248035 Miss Ratio: 0.06559489607519656 Number of Writes to Memory: 71942 Number of Reads from Memory: 319713 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 65536 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 65536 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9403309730115779 Miss Ratio: 0.059669026988422164 Number of Writes to Memory: 66927 Number of Reads from Memory: 290830 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 131072 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 131072 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9441711035969449 Miss Ratio: 0.05582889640305512 Number of Writes to Memory: 61142 Number of Reads from Memory: 272113 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	

Phong Nguyenho
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XSbench:

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 8192 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 8192
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8637385447840966
Miss Ratio: 0.13626145521590335
Number of Writes to Memory: 55680
Number of Reads from Memory: 2885331

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 16384 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 16384
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8806370883044365
Miss Ratio: 0.11936291169556346
Number of Writes to Memory: 7318
Number of Reads from Memory: 2527505

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8874613747812806
Miss Ratio: 0.11253862521871941
Number of Writes to Memory: 600
Number of Reads from Memory: 2383001

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 65536 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 65536
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

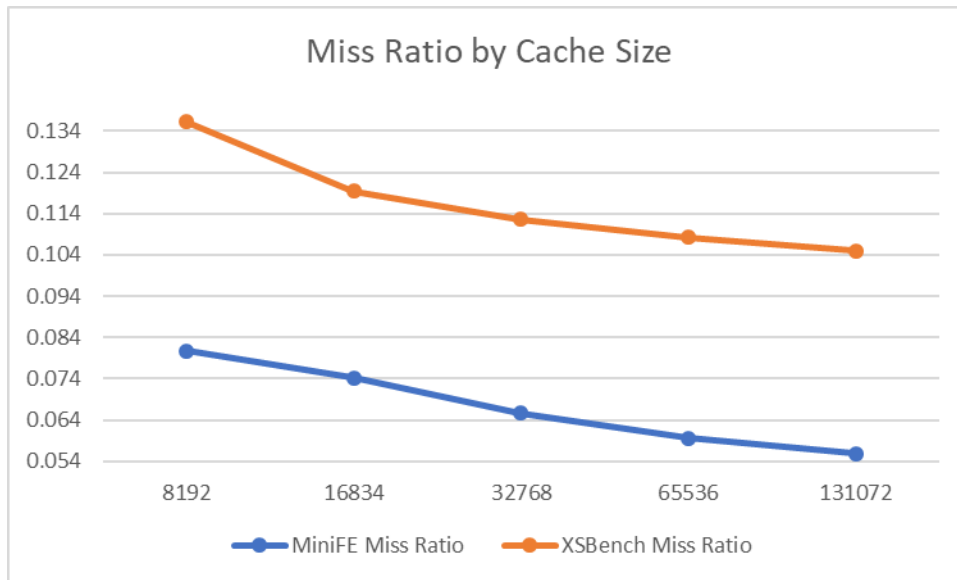
Cache Statistics
-----
Hit Ratio: 0.8918015480642444
Miss Ratio: 0.10819845193575563
Number of Writes to Memory: 69
Number of Reads from Memory: 2291098

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 131072 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 131072
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8951060641859033
Miss Ratio: 0.10489393581409666
Number of Writes to Memory: 36
Number of Reads from Memory: 2221125

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```



Looking at the trends for the miss ratio of both MiniFE and XSBench, the miss ratio decreases as the cache size is increased. The number of hits increases while the number of misses decreases as the size of the cache increases. This is probably due to having more rows to access to.

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Part B:

MiniFE:

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 8192 4 0 0 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 8192
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.919296733129492
Miss Ratio: 0.08070326687050797
Number of Writes to Memory: 636483
Number of Reads from Memory: 393352

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 16384 4 0 0 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 16384
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9257687595928891
Miss Ratio: 0.07423124040711088
Number of Writes to Memory: 636483
Number of Reads from Memory: 361807

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 4 0 0 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9344051039248035
Miss Ratio: 0.06559489607519656
Number of Writes to Memory: 636483
Number of Reads from Memory: 319713

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 65536 4 0 0 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 65536
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9403309730115779
Miss Ratio: 0.059669026988422164
Number of Writes to Memory: 636483
Number of Reads from Memory: 290830

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 131072 4 0 0 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 131072
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9441711035969449
Miss Ratio: 0.05582889640305512
Number of Writes to Memory: 636483
Number of Reads from Memory: 272113

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```

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XSbench:

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 8192 4 0 0 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 8192
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8637385447840966
Miss Ratio: 0.13626145521590335
Number of Writes to Memory: 5013495
Number of Reads from Memory: 2885331

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 16384 4 0 0 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 16384
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8806370883044365
Miss Ratio: 0.11936291169556346
Number of Writes to Memory: 5013495
Number of Reads from Memory: 2527505

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 4 0 0 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8874613747812806
Miss Ratio: 0.11253862521871941
Number of Writes to Memory: 5013495
Number of Reads from Memory: 2383001

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 65536 4 0 0 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 65536
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

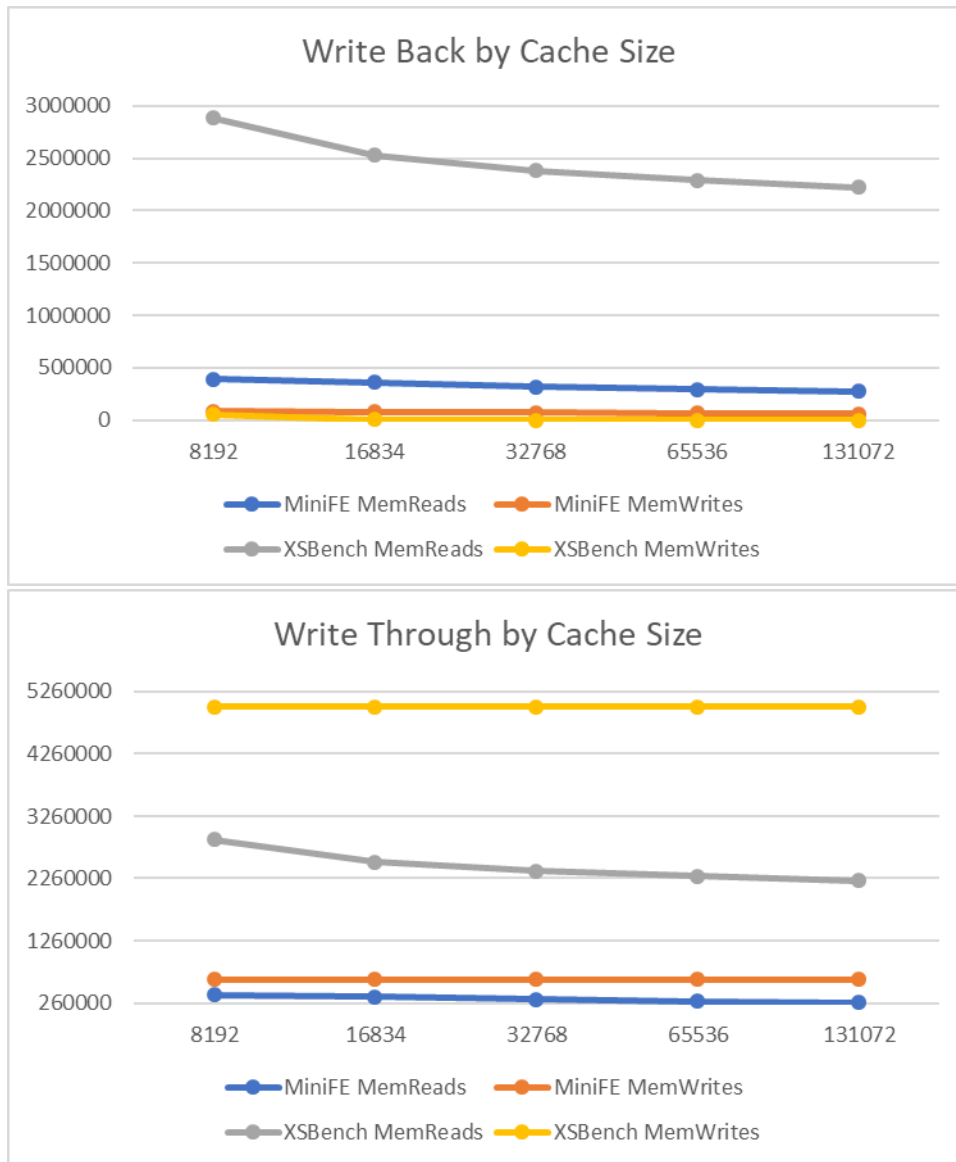
Cache Statistics
-----
Hit Ratio: 0.8918015480642444
Miss Ratio: 0.10819845193575563
Number of Writes to Memory: 5013495
Number of Reads from Memory: 2291098

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 131072 4 0 0 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 131072
Write Policy: Write-Through
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8951060641859033
Miss Ratio: 0.10489393581409666
Number of Writes to Memory: 5013495
Number of Reads from Memory: 2221125

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```



There seems to be more memory writes for a write through than write back. The only thing that drastically changes is the XSBench's memory writes going by the write back and write through trends. The amount of writes and reads decreases as the cache size increases. This is probably due to having more hits and less misses.

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Part C:

MiniFE:

<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 1 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 1 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9245943776155081 Miss Ratio: 0.07540562238449192 Number of Writes to Memory: 80768 Number of Reads from Memory: 367531 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 2 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 2 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9338493036493448 Miss Ratio: 0.0661506963506552 Number of Writes to Memory: 73895 Number of Reads from Memory: 322422 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 4 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9344051039248035 Miss Ratio: 0.06559489607519656 Number of Writes to Memory: 71942 Number of Reads from Memory: 319713 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 8 0 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 8 Replacement Policy: Least Recently Used Cache Statistics ----- Hit Ratio: 0.9347081371499243 Miss Ratio: 0.0652918628500757 Number of Writes to Memory: 71657 Number of Reads from Memory: 318236 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>

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```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 16 0 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 16
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9345702642133764
Miss Ratio: 0.06542973578662357
Number of Writes to Memory: 71615
Number of Reads from Memory: 318908

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 32 0 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 32
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9344167985042428
Miss Ratio: 0.06558320149575722
Number of Writes to Memory: 71584
Number of Reads from Memory: 319656

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 64 0 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 64
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.9343343209439865
Miss Ratio: 0.06566567905601355
Number of Writes to Memory: 71621
Number of Reads from Memory: 320058

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```


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XSbench:

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 1 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 1
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8773031978665746
Miss Ratio: 0.12269680213342542
Number of Writes to Memory: 36601
Number of Reads from Memory: 2598100

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 2 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 2
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8855425518847473
Miss Ratio: 0.11445744811525273
Number of Writes to Memory: 4814
Number of Reads from Memory: 2423632

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 4 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 4
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8874613747812806
Miss Ratio: 0.11253862521871941
Number of Writes to Memory: 600
Number of Reads from Memory: 2383001

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 8 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 8
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8879923320756057
Miss Ratio: 0.11200766792439429
Number of Writes to Memory: 44
Number of Reads from Memory: 2371758

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 16 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 16
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.8880944810240736
Miss Ratio: 0.11190551897592634
Number of Writes to Memory: 35
Number of Reads from Memory: 2369595

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 32 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 32
Replacement Policy: Least Recently Used

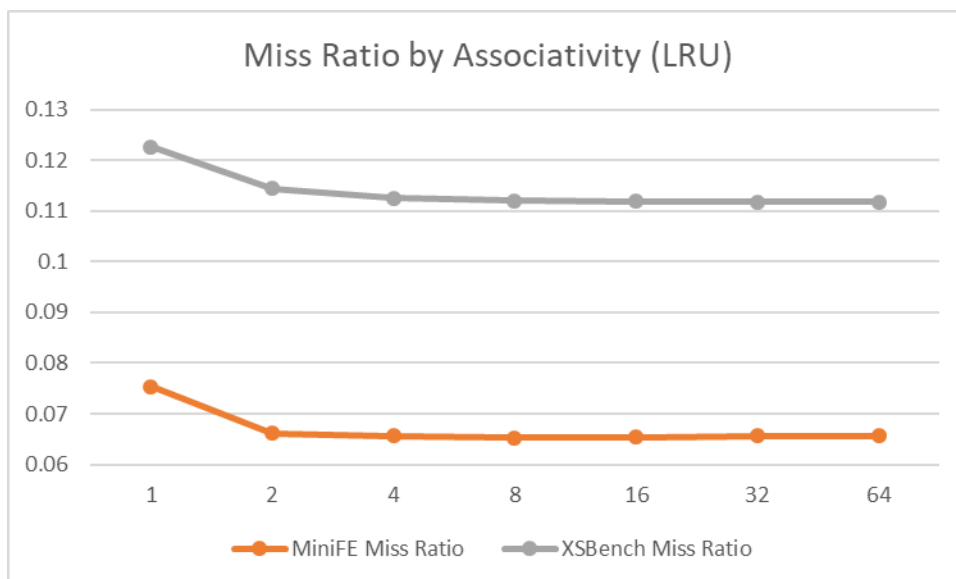
Cache Statistics
-----
Hit Ratio: 0.8882158035615745
Miss Ratio: 0.11178419643842555
Number of Writes to Memory: 35
Number of Reads from Memory: 2367026

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 64 0 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 64
Replacement Policy: Least Recently Used

Cache Statistics
-----
Hit Ratio: 0.888246783547795
Miss Ratio: 0.11175321645220504
Number of Writes to Memory: 35
Number of Reads from Memory: 2366370

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```



Miss ratio decreases as associativity approaches 8 but then increases slightly after 8 making a bell curve like trend for MiniFE. Miss ratio keeps decreasing after 8 for XSBench. This is probably due to XSBench having more hits than misses.

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Part D:

MiniFE:

<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 1 1 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 1 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.9245943776155081 Miss Ratio: 0.07540562238449192 Number of Writes to Memory: 80768 Number of Reads from Memory: 367531 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 2 1 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 2 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.9319767347626298 Miss Ratio: 0.06802326523737022 Number of Writes to Memory: 75550 Number of Reads from Memory: 331549 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 4 1 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.9322574046691737 Miss Ratio: 0.06774259533082631 Number of Writes to Memory: 73880 Number of Reads from Memory: 330181 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 8 1 1 home/TRACES/MINIFE.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 8 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.9323909690764545 Miss Ratio: 0.06760903092354556 Number of Writes to Memory: 73697 Number of Reads from Memory: 329530 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>

Phong Nguyenho
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```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 16 1 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 16
Replacement Policy: First In First Out

Cache Statistics
-----
Hit Ratio: 0.9319295461087518
Miss Ratio: 0.0680704538912482
Number of Writes to Memory: 73660
Number of Reads from Memory: 331779

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 32 1 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 32
Replacement Policy: First In First Out

Cache Statistics
-----
Hit Ratio: 0.9317732080467734
Miss Ratio: 0.0682267919532266
Number of Writes to Memory: 73669
Number of Reads from Memory: 332541

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |

~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 64 1 1 home/TRACES/MINIFE.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 64
Replacement Policy: First In First Out

Cache Statistics
-----
Hit Ratio: 0.9317254038887144
Miss Ratio: 0.06827459611128561
Number of Writes to Memory: 73748
Number of Reads from Memory: 332774

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```

Phong Nguyenho
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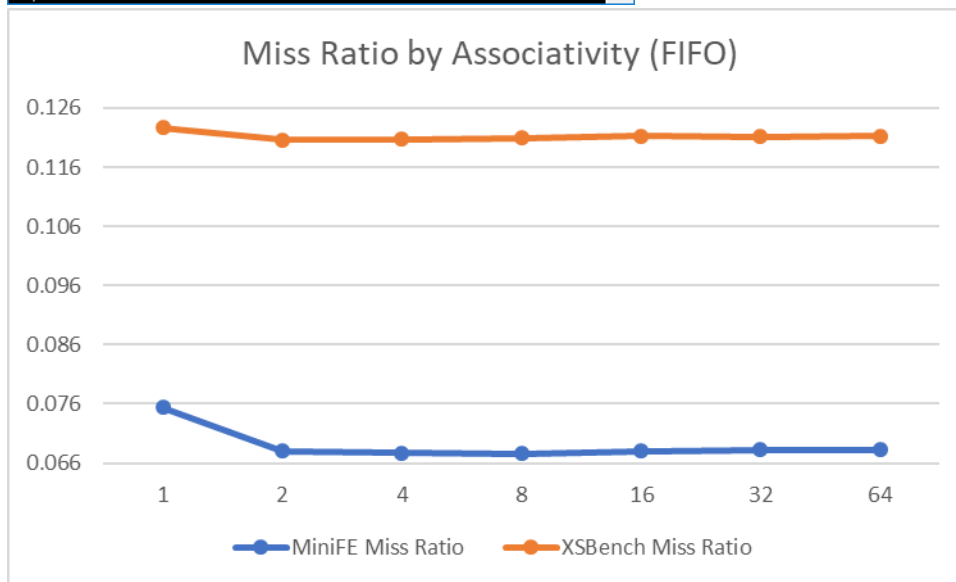
XSbench:

<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 1 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 1 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8773031978665746 Miss Ratio: 0.12269680213342542 Number of Writes to Memory: 36601 Number of Reads from Memory: 2598100 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 2 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 2 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8793901438590607 Miss Ratio: 0.12060985614093929 Number of Writes to Memory: 32029 Number of Reads from Memory: 2553909 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 4 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 4 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8793283727889747 Miss Ratio: 0.12067162721102533 Number of Writes to Memory: 32613 Number of Reads from Memory: 2555217 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 8 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 8 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8791085376733397 Miss Ratio: 0.12089146232666025 Number of Writes to Memory: 32701 Number of Reads from Memory: 2559872 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>
<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 16 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 16 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8787794697709242 Miss Ratio: 0.12122053022907575 Number of Writes to Memory: 34150 Number of Reads from Memory: 2566840 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>	<pre>~/Computer Architecture Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ java SIM 32768 32 1 1 home/TRACES/XSBENCH.t Cache Descriptions ----- Cache Size: 32768 Write Policy: Write-Back Cache Associativity: 32 Replacement Policy: First In First Out Cache Statistics ----- Hit Ratio: 0.8788752432649108 Miss Ratio: 0.12112475673508914 Number of Writes to Memory: 33228 Number of Reads from Memory: 2564812 Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture \$ </pre>

```
~/Computer Architecture
Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ java SIM 32768 64 1 1 home/TRACES/XSBENCH.t
Cache Descriptions
-----
Cache Size: 32768
Write Policy: Write-Back
Cache Associativity: 64
Replacement Policy: First In First Out

Cache Statistics
-----
Hit Ratio: 0.8787879231513106
Miss Ratio: 0.12121207684868936
Number of Writes to Memory: 33128
Number of Reads from Memory: 2566661

Donkey Phong@DESKTOP-A0M39PE ~/Computer Architecture
$ |
```



Comparing the miss ratio for both FIFO and LRU, LRU seems to be better for getting less miss ratio but with a chance of having more if the cache size is increased. The miss ratio for FIFO seems to be consistent after associativity of 1. Both LRU and FIFO have the same miss ratio at associativity of 1.