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Lecture 01: INTRODUCTION

PROF. INDRANIL SENGUPTA
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Main Objectives of the Course

Hardware Modeling Using Verilog

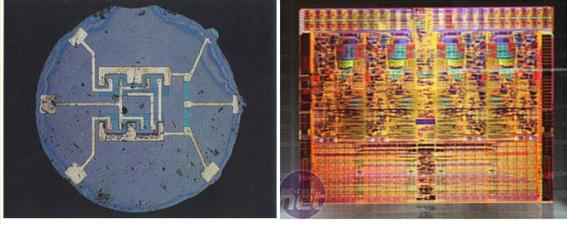
1. Learn about the Verilog hardware description language.
2. Understand the difference between behavioral and structural design styles.
3. Learn to write test benches and analyze simulation results.
4. Learn to model combinational and sequential circuits.
5. Distinguish between good and bad coding practices.
6. Case studies with some complex designs.

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VLSI Design Process

- Design complexity increasing rapidly
 - Increased size and complexity
 - Fabrication technology improving
 - CAD tools are essential
 - Conflicting requirements like area, speed, and energy consumption
- The present trend
 - Standardize the design flow
 - Emphasis on low-power design, and increased performance

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First Planar IC (1961) and Intel Nehalem Quad Core Die

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Moore's Law

- Exponential growth
- Design complexity increases rapidly
- Automated tools are essential
- Must follow well-defined design flow

<img alt="A log-linear plot of Transistors vs Year showing Moore's Law. The Y-axis is logarithmic from 1,000 to 10,000,000,000. The X-axis is linear from 1970 to 2015. Data points show a clear exponential growth trend, with labels for various chip generations like 8080, 8085, 8086, 80286, 8030, 8040, 8048, 8050, 8051, 8052, 8053, 8054, 8055, 8056, 8057, 8058, 8059, 8060, 8061, 8062, 8063, 8064, 8065, 8066, 8067, 8068, 8069, 8070, 8071, 8072, 8073, 8074, 8075, 8076, 8077, 8078, 8079, 8080, 8081, 8082, 8083, 8084, 8085, 8086, 8087, 8088, 8089, 8090, 8091, 8092, 8093, 8094, 8095, 8096, 8097, 8098, 8099, 80100, 80101, 80102, 80103, 80104, 80105, 80106, 80107, 80108, 80109, 80110, 80111, 80112, 80113, 80114, 80115, 80116, 80117, 80118, 80119, 80120, 80121, 80122, 80123, 80124, 80125, 80126, 80127, 80128, 80129, 80130, 80131, 80132, 80133, 80134, 80135, 80136, 80137, 80138, 80139, 80140, 80141, 80142, 80143, 80144, 80145, 80146, 80147, 80148, 80149, 80150, 80151, 80152, 80153, 80154, 80155, 80156, 80157, 80158, 80159, 80160, 80161, 80162, 80163, 80164, 80165, 80166, 80167, 80168, 80169, 80170, 80171, 80172, 80173, 80174, 80175, 80176, 80177, 80178, 80179, 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VLSI Design Flow

- Standardized design procedure
 - Starting from the design idea down to the actual implementation.
- Encompasses many steps:
 - Specification
 - Synthesis
 - Simulation
 - Layout
 - Testability analysis
 - and many more

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- Need to use Computer Aided Design (CAD) tools.
 - Based on Hardware Description Language (HDL).
 - HDLs provide formats for representing the outputs of various design steps.
 - A CAD tool transforms its HDL input into a HDL output that contains more detailed information about the hardware.
 - Behavioral level to register transfer level
 - Register transfer level to gate level
 - Gate level to transistor level
 - Transistor level to the layout level

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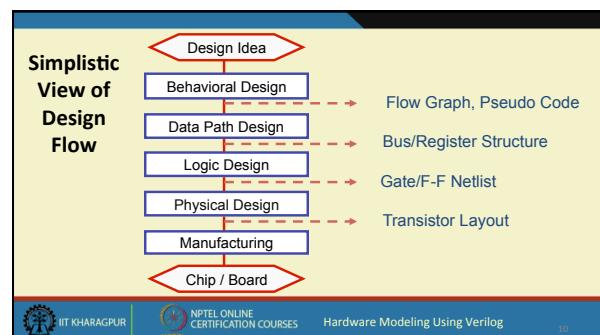
Two Competing HDLs

- Verilog
- VHDL

Designs are created typically using HDLs, which get transformed from one level of abstraction to the next as the design flow progresses.

There are other HDLs like SystemC, SystemVerilog, and many more ...

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Steps in the Design Flow

- Behavioral design
 - Specify the functionality of the design in terms of its *behavior*.
 - Various ways of specifying:
 - Boolean expression or truth table.
 - Finite-state machine behavior (e.g. state transition diagram or table).
 - In the form of a high-level algorithm.
 - Needs to be synthesized into more detailed specifications for hardware realization.

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- Data path design
 - Generate a netlist of register transfer level components, like registers, adders, multiplexers, decoders, etc.
 - A **netlist** is a directed graph, where the vertices indicate components, and the edges indicate interconnections.
 - A netlist specification is also referred to as **structural design**.
 - Netlist may be specified at various levels, where the components may be functional modules, gates or transistors.
 - Systematically transformed from one level to the next.

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- Logic design
 - Generate a netlist of gates/flip-flops or standard cells.
 - A standard cell is a pre-designed circuit module (like gates, flip-flops, multiplexer, etc.) at the layout level.
 - Various logic optimization techniques are used to obtain a cost effective design.
 - There may be conflicting requirements during optimization:
 - Minimize number of gates.
 - Minimize number of gate levels (i.e. delay).
 - Minimize signal transition activities (i.e. dynamic power).

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- Physical design and Manufacturing
 - Generate the final layout that can be sent for fabrication.
 - The layout contains a large number of regular geometric shapes corresponding to the different fabrication layers.
 - Alternatively, the final target may be Field Programmable Gate Array (FPGA), where technology mapping from the gate level netlist is used.
 - Can be programmed in-field.
 - Much greater flexibility, but less speed.

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Other Steps in the Design Flow

- Simulation for verification
 - At various levels: logic level, switch level, circuit level
- Formal verification
 - Used to verify the designs through formal techniques
- Testability analysis and Test pattern generation
 - Required for testing the manufactured devices

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END OF LECTURE 01

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Lecture 02: DESIGN REPRESENTATION

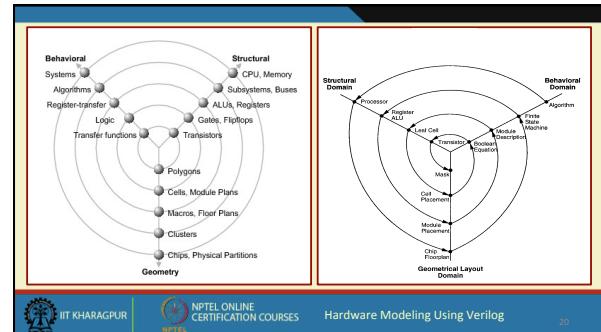
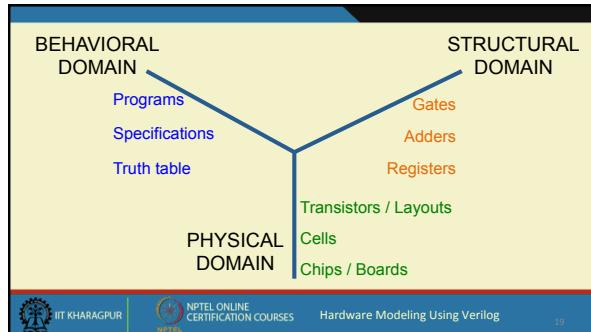
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Design Representation

- A design can be represented at various levels from three different points of view:
 1. Behavioral
 2. Structural
 3. Physical
- Can be conveniently expressed by [Y-diagram](#).

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Behavioral Representation

- Specifies how a particular design should respond to a given set of inputs.
- May be specified by:
 - Boolean equations
 - Tables of input and output values
 - Algorithms written in standard HLL like C
 - Algorithms written in special HDL like Verilog or VHDL

Behavioral Representation :: Example

Full Adder:

- two operand inputs A and B
- a carry input C
- a carry output Cy
- a sum output S

Express in terms of Boolean expressions:

$$S = A \cdot B' \cdot C' + A' \cdot B' \cdot C + A' \cdot B \cdot C' + A \cdot B \cdot C = A \oplus B \oplus C$$

$$Cy = A \cdot B + A \cdot C + B \cdot C$$

- Express in Verilog in terms of Boolean expressions

```
module carry (S, Cy, A, B, C);
  input A, B, C;
  output S, Cy;
  assign S = A ^ B ^ C;
  assign Cy = (A & B) | (B & C) | (C & A);
endmodule
```

- Express in Verilog in terms of truth table (only Cy is shown)

```
primitive carry (Cy, A, B, C);
  input A, B, C;
  output Cy;
  table
    // A   B   C   Cy
    1   1   ?   :   1 ;
    1   ?   1   :   1 ;
    ?   1   1   :   1 ;
    0   0   ?   :   0 ;
    0   ?   0   :   0 ;
    ?   0   0   :   0 ;
  endtable
endprimitive
```

Structural Representation

- Specifies how components are interconnected.
- In general, the description is a list of modules and their interconnection.
 - Called *netlist*.
 - Can be specified at various levels.

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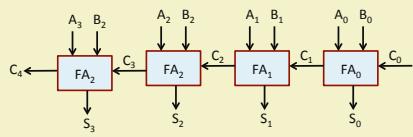
- At the structural level, the levels of abstraction are:
 - The module (functional) level
 - The gate level
 - The transistor level
 - Any combination of above
- In each successive level more detail is revealed about the implementation.

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Example: A 4-bit Ripple Carry Adder

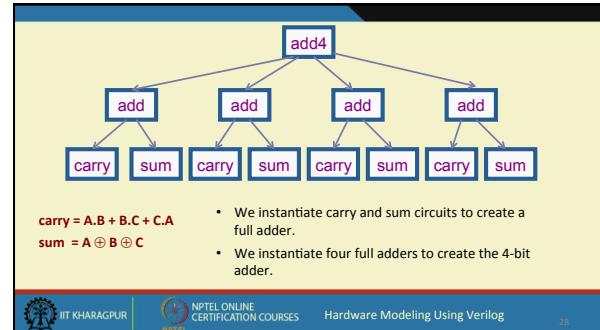


- Consists of four full adders.
- Each full adder consists of a sum circuit and a carry circuit.

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```
module add (cy_out, sum, a, b, cy_in);
  input a, b, cy_in;
  output sum, cy_out;
  sum s1 (sum, a, b, cy_in);
  carry c1 (cy_out, a, b, cy_in);
endmodule

module add4 (s, cy4,
  input [3:0] x, y;
  output [3:0] s;
  output cy4;
  wire [2:0] cy_out;
  add B0 (cy_out[0], s[0], x[0], y[0], ci);
  add B1 (cy_out[1], s[1], x[1], y[1], cy_out[0]);
  add B2 (cy_out[2], s[2], x[2], y[2], cy_out[1]);
  add B3 (cy4, s[3], x[3], y[3], cy_out[2]);
endmodule
```

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```
module sum (sum, a, b, cy_in);
  input a, b, cy_in;
  output sum;
  sum s1 (sum, a, b, cy_in);
  carry c1 (cy_out, a, b, cy_in);
endmodule

module carry (cy_out, a, b, cy_in);
  input a, b, cy_in;
  output cy_out;
  wire t1, t2, t3;
  and g1 (t1, a, b);
  and g2 (t2, a, c);
  and g3 (t3, b, c);
  or g4 (cy_out, t1, t2, t3);
endmodule
```

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Physical Representation

- The lowest level of physical specification.
 - Photo-mask information required by the various processing steps in the fabrication process.
- At the module level, the physical layout for the 4-bit adder may be defined by a rectangle or polygon, and a collection of ports.
- At the layout level, there can be a large number of rectangles or polygons.



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- Partial physical description for 4-bit adder in Verilog

```
module add4;
  input x[3:0], y[3:0], cy_in;
  output s[3:0], cy4;
  boundary [0, 0, 130, 500];
  port x[0] aluminum width = 1 origin = [0, 35];
  port y[0] aluminum width = 1 origin = [0, 85];
  port cy_in polysilicon width = 2 origin = [70, 0];
  port s[0] aluminum width = 1 origin = [120, 65];

  add a0 origin = [0, 0];
  add a1 origin = [0, 120];
endmodule
```



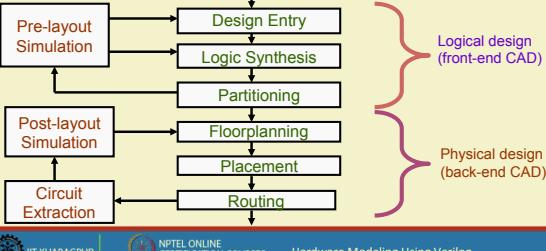
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Digital IC Design Flow: A quick look



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END OF LECTURE 02

Lecture 03: GETTING STARTED WITH VERILOG

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Why do we use Verilog?

- To describe a digital system as a set of *modules*.
 - Each of the modules will have an interface to other modules, in addition to its description.
- Two ways to specify a module:
 - By specifying its internal logical structure (called *structural representation*).
 - By describing its behavior in a program-like manner (called *behavioral representation*).
- The modules are interconnected using *nets*, which allow them to work with each other.



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What next?

- After specifying the system in Verilog, we can do two things:
 - Simulate the system and verify the operation.
 - Just like running a program written in some high-level language.
 - Requires a *test bench* or *test harness*, that specifies the inputs that are to be applied and the way the outputs are to be displayed.
 - Use a synthesis tool to map it to hardware.
 - Converts it to a netlist of low-level primitives.
 - The hardware can be *Application Specific Integrated Circuit* (ASIC).
 - Or else, it can be *Field Programmable Gate Array* (FPGA).



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- When the design is mapped to hardware, we do not need test bench for simulation any more.
- Signals can be actually applied from some source (e.g. signal generator), and response evaluated by some equipment (e.g. oscilloscope or logic analyzer).



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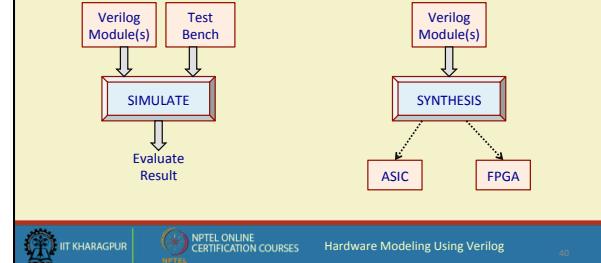
- Using ASIC as hardware target?
 - When high performance and high packing density is required.
 - When the manufactured hardware is expected to be used in large numbers (e.g. processor chips).
- Using FPGA as hardware target?
 - When fast turnaround time is required to validate the design.
 - The mapping can be done in the laboratory itself with a FPGA kit and associated software.
 - There is a tradeoff in performance.



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How to Simulate?

- Free software available:
 - Icarus Verilog (<http://verilog.icarus.com>)
 - GTKWave (<http://gtkwave.sourceforge.net>)
- Commercial software (with free versions available):
 - From Xilinx (ISE, Vivado)
 - Many more.



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How to Synthesize?

- For FPGA as target, specific software is required:
 - Xilinx ISE or Vivado for Xilinx FPGA kits.
 - Similar software available from other FPGA vendors.
- For ASIC as target, commercial CAD tools exist:
 - Tool suite from Cadence.
 - Tool suite from Synopsys.
 - Several others ...



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Scope of this Course

- We shall be discussing features of the Verilog language, and verifying the design through simulation.
 - How to design combinational and sequential digital circuits?
 - How to verify the functionality through simulation?
- We shall not be discussing the synthesis tools; however:
 - Shall discuss various tricks that help in synthesis.
 - Shall discuss the common design flow – first code the modules in behavioral design style, and then translate selected subset of modules to structural design style.



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How to Simulate Verilog Module(s)

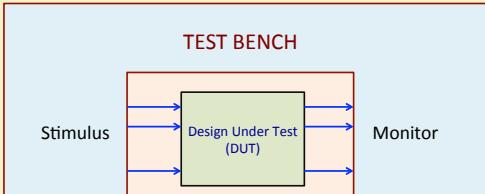
- Using a test bench to verify the functionality of a design coded in Verilog (called Design-under-Test or DUT), comprising of:
 - A set of stimulus for the DUT.
 - A monitor, which captures or analyzes the outputs of the DUT.
- Requirement:
 - The inputs of the DUT need to be connected to the test bench.
 - The outputs of the DUT needs also to be connected to the test bench.



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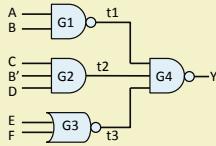


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An Example



```
module example (A,B,C,D,E,F,Y);
  input A,B,C,D,E,F;
  output Y;
  wire t1, t2, t3, Y;
  nand #1 G1 (t1,A,B);
  and #2 G2 (t2,C,-B,D);
  nor #1 G3 (t3,E,F);
  nand #1 G4 (Y,t1,t2,t3);
endmodule
```

We can combine declarations of same type of gate together:

```
nand #1 G1 (t1,A,B),
      G4 (Y,t1,t2,t3);
```



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```
module testbench;
  reg A,B,C,D,E,F; wire Y;
  example DUT(A,B,C,D,E,F,Y);

  initial
    begin
      monitor ($stime," A=%b, B=%b, C=%b,
      D=%b, E=%b, F=%b, Y=%b",
      A,B,C,D,E,F,Y);
      #5 A=1; B=0; C=0; D=1; E=0; F=0;
      #5 A=0; B=0; C=1; D=1; E=0; F=0;
      #5 A=1; C=0;
      #5 F=1;
      #5 $finish;
    end
  endmodule
```

```
example.v
module example
  (A,B,C,D,E,F,Y);
  wire t1, t2, t3, Y;
  nand #1 G1 (t1,A,B);
  and #2 G2 (t2,C,-B,D);
  nor #1 G3 (t3,E,F);
  nand #1 G4 (Y,t1,t2,t3);
endmodule
```

example-test.v

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Simulation results:

```
0 A=x, B=x, C=x, D=x, E=x, F=x, Y=x
5 A=1, B=0, C=0, D=1, E=0, F=0, Y=x
8 A=1, B=0, C=0, D=1, E=0, F=0, Y=1
10 A=0, B=0, C=1, D=1, E=0, F=0, Y=1
13 A=0, B=0, C=1, D=1, E=0, F=0, Y=0
15 A=1, B=0, C=0, D=1, E=0, F=0, Y=0
18 A=1, B=0, C=0, D=1, E=0, F=0, Y=1
20 A=1, B=0, C=0, D=1, E=0, F=1, Y=1
```

Command in Verilog:

a) iverilog -o mysim example.v example-test.v

b) vvp mysim

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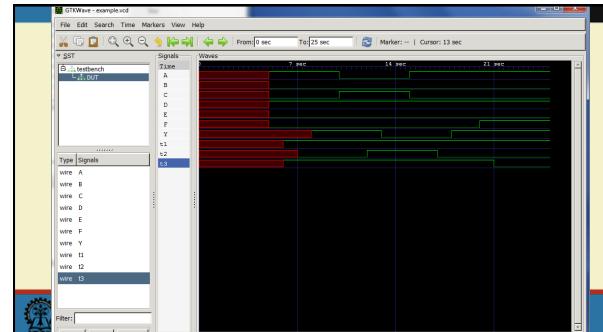
To display the waveforms

Run the command:
gtkwave example.vcd

```
module testbench;
reg A,B,C,D,E,F; wire Y;
example DUT(A,B,C,D,E,F,Y);

initial
begin
$dumpfile ("example.vcd");
$dumpvars (0,testbench);
$monitor ($time," A=%b, B=%b, C=%b,
D=%b, E=%b, F=%b, Y=%b",
A,B,C,D,E,F,Y);
#5 A=1; B=0; C=0; D=1; E=0; F=0;
#5 A=0; B=0; C=1; D=1; E=0; F=0;
#5 A=1; C=0;
#5 F=1;
#5 $finish;
end
endmodule
```

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END OF LECTURE 03

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Lecture 04: VLSI DESIGN STYLES (PART 1)

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VLSI Design Cycle

- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost

System Specifications

Manual Automation

Chip

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VLSI Design Cycle (contd.)

1. System specification
2. Functional design
3. Logic design
4. Circuit design
5. Physical design
6. Design verification
7. Fabrication
8. Packaging, testing, and debugging

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Physical Design

- Converts a circuit description into a geometric description.
 - This description is used for fabrication of the chip.
- Basic steps in the physical design cycle:
 - Partitioning, floorplanning and placement
 - Routing
 - Static timing analysis
 - Signal integrity and crosstalk analysis
 - Physical verification and signoff

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Various Design Styles

- Programmable Logic Devices
 - Field Programmable Gate Array (FPGA)
 - Gate Array
- Standard Cell (Semi-Custom Design)
- Full-Custom Design

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Which Design Style to Use?

- Basically a tradeoff among several design parameters.
 - Hardware cost
 - Circuit delay
 - Time required
- Optimizing on these parameters is often conflicting.

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Field Programmable Gate Array (FPGA)

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What does FPGA offer?

- User / Field Programmability.
 - Array of logic cells connected via routing channels.
 - Different types of cells:
 - Special I/O cells.
 - Logic cells (Mainly lookup tables (LUT) with associated registers).
 - Interconnection between cells:
 - Using SRAM based switches.
 - Using anti-fuse elements.

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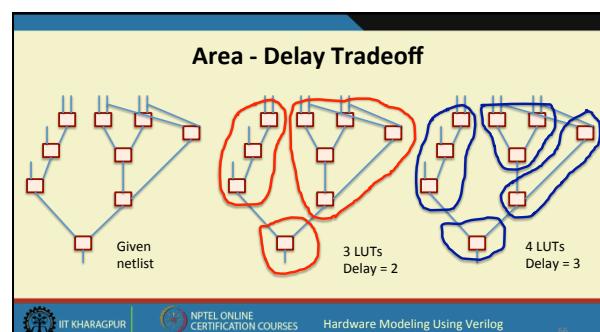
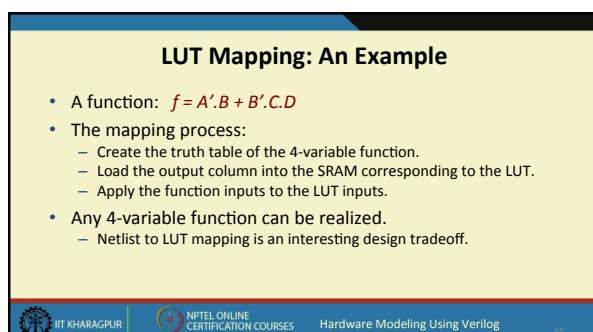
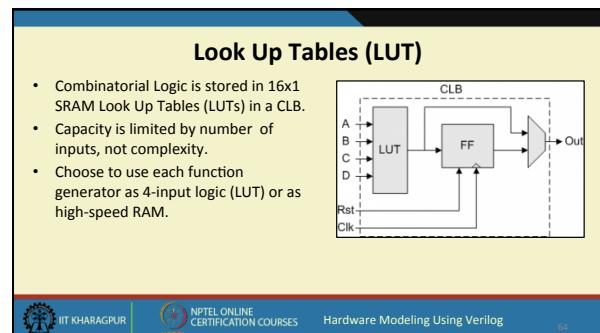
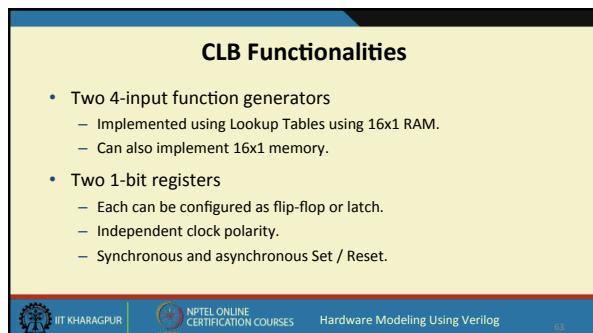
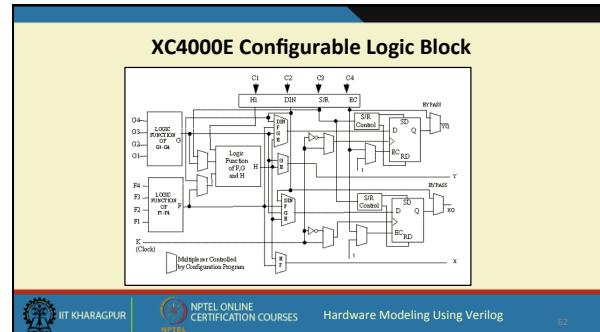
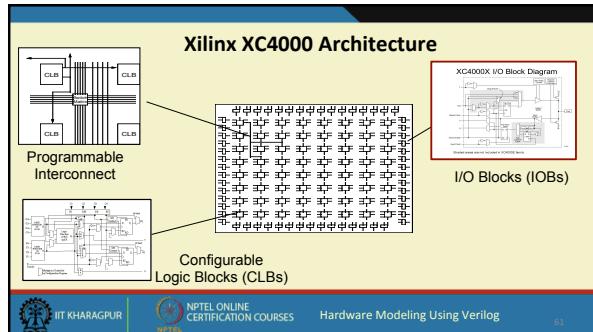
Ease of Use

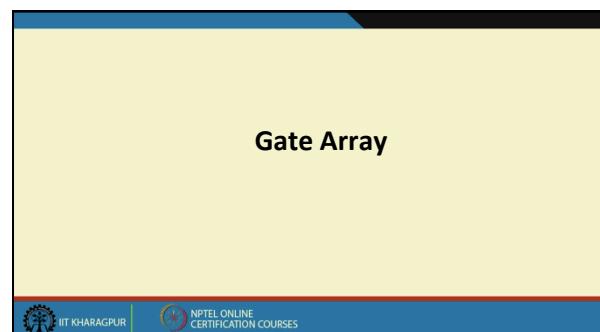
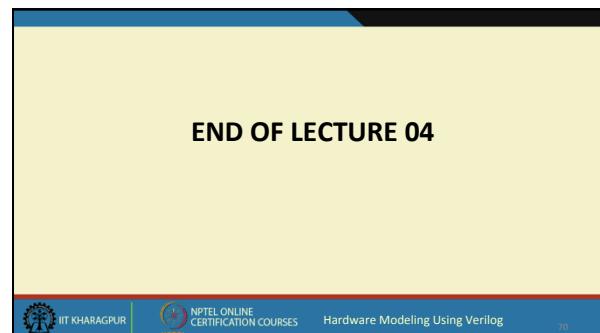
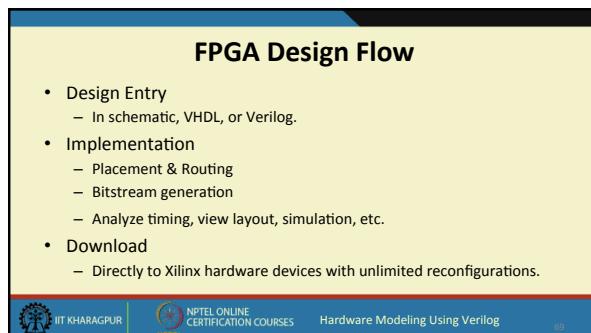
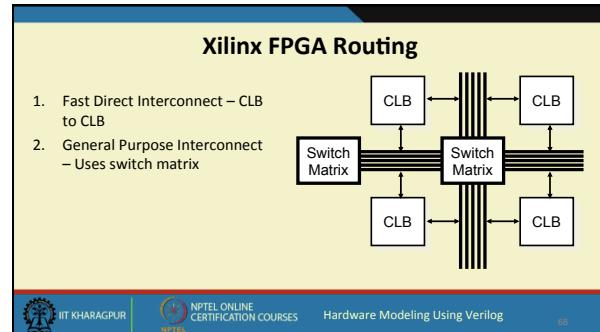
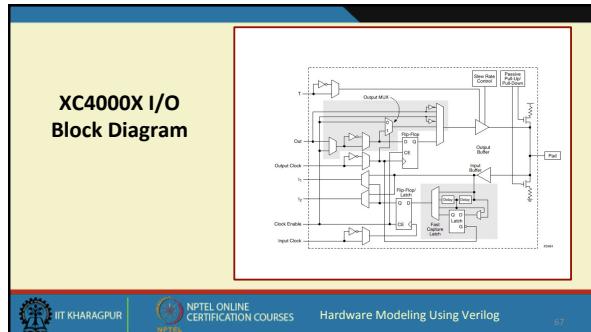
- FPGA chips are manufactured by a number of vendors:
 - Xilinx, Altera, Actel, etc.
 - Products vary widely in capability.
- FPGA development boards and CAD software available from many sellers.
 - Allows rapid prototyping in laboratory.

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Introduction

- In view of the speed of prototyping capability, the gate array (GA) comes after the FPGA.
- Design implementation of
 - FPGA chip is done with user programming,
 - Gate array is done with metal mask design and processing.

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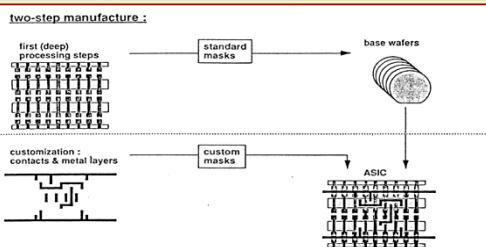
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- Gate array implementation requires a two-step manufacturing process:
 - a) The first phase, which is based on generic (standard) masks, results in an array of uncommitted transistors on each GA chip.
 - b) These uncommitted chips can be customized later, which is completed by defining the metal interconnects between the transistors of the array.

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- The GA chip utilization factor is higher than that of FPGA.
 - The used chip area divided by the total chip area.
- Chip speed is also higher.
 - More customized design can be achieved with metal mask designs.
- Typical gate array chips can implement millions of logic gates.

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Standard Cell Based Design

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Introduction

- One of the most prevalent design styles.
 - Also called semi-custom design style.
 - Requires developing full custom mask set.
- Basic idea:
 - Commonly used logic cells are developed, and stored in a standard cell library.
 - Typical library may contain a few hundred cells (*Inverters, NAND gates, NOR gates, AOI gates, OAI gates, 2-to-1 MUX, D-latches, flip-flops, etc.*).

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Characteristic of the Cells

- Each cell is designed with a fixed height.
 - To enable automated placement of the cells, and routing of inter-cell connections.
 - A number of cells can be abutted side-by-side to form rows.
- The power and ground rails typically run parallel to upper and lower boundaries of cell.
 - Neighboring cells share a common power and ground bus.
- The input and output pins are located on the upper and lower boundaries of the cell.



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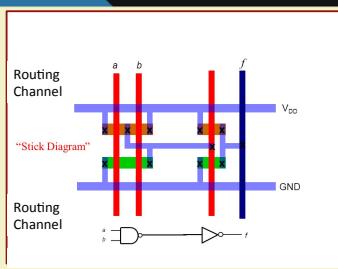
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Standard Cell Example

Made to stack side by side

- Fixed height
- Width can vary
- Can abut at V_{DD} and GND



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Floorplan for Standard Cell Design

- Inside the I/O frame which is reserved for I/O cells, the chip area contains rows or columns of standard cells.
 - Between cell rows are channels for routing.
 - Over-the-cell routing is also possible.
- The physical design and layout of logic cells ensure that
 - When placed into rows, their heights match.
 - Neighboring cells can abut side-by-side, which provides natural connections for power and ground lines in each row.

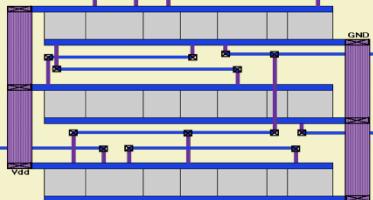


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Standard Cell Layout

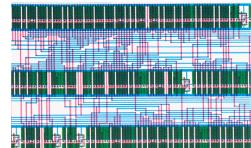


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Standard Cell Layout



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Full Custom Design



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Introduction

- Standard-cells based design is often called semi custom design.
 - The cells are pre-designed for general use.
- In the full custom design, the entire mask design is done anew without use of any library.
 - The development cost of such a design style is prohibitively high.
 - The concept of design reuse is becoming popular to reduce design cycle time and cost.

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- The most rigorous full custom design can be the design of a memory cell.
 - Static or dynamic.
 - Since the same layout design is replicated, there would not be any alternative to high density memory chip design.
- For logic chip design, a good compromise can be achieved by combining different design styles on the same chip.
 - Standard cells, data-path cells and PLAs.

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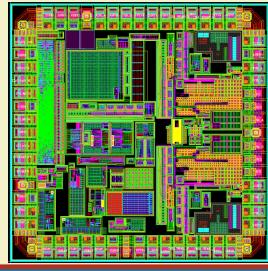
- In real full-custom layout in which the geometry, orientation and placement of every transistor is done individually by the designer.
 - Design productivity is usually very low (typically 10 to 20 transistors per day, per designer).
- In digital CMOS VLSI, full-custom design is rarely used due to the high labor cost.
 - Exceptions to this include the design of high-volume products such as memory chips, high-performance microprocessors and FPGA masters.

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A full custom layout

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Comparison Among Various Design Styles

	Design Style			
	FPGA	Gate array	Standard cell	Full custom
Cell size	Fixed	Fixed	Fixed height	Variable
Cell type	Programmable	Fixed	Variable	Variable
Cell placement	Fixed	Fixed	In row	Variable
Interconnect	Programmable	Variable	Variable	Variable
Design time	Very fast	Fast	Medium	Slow

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