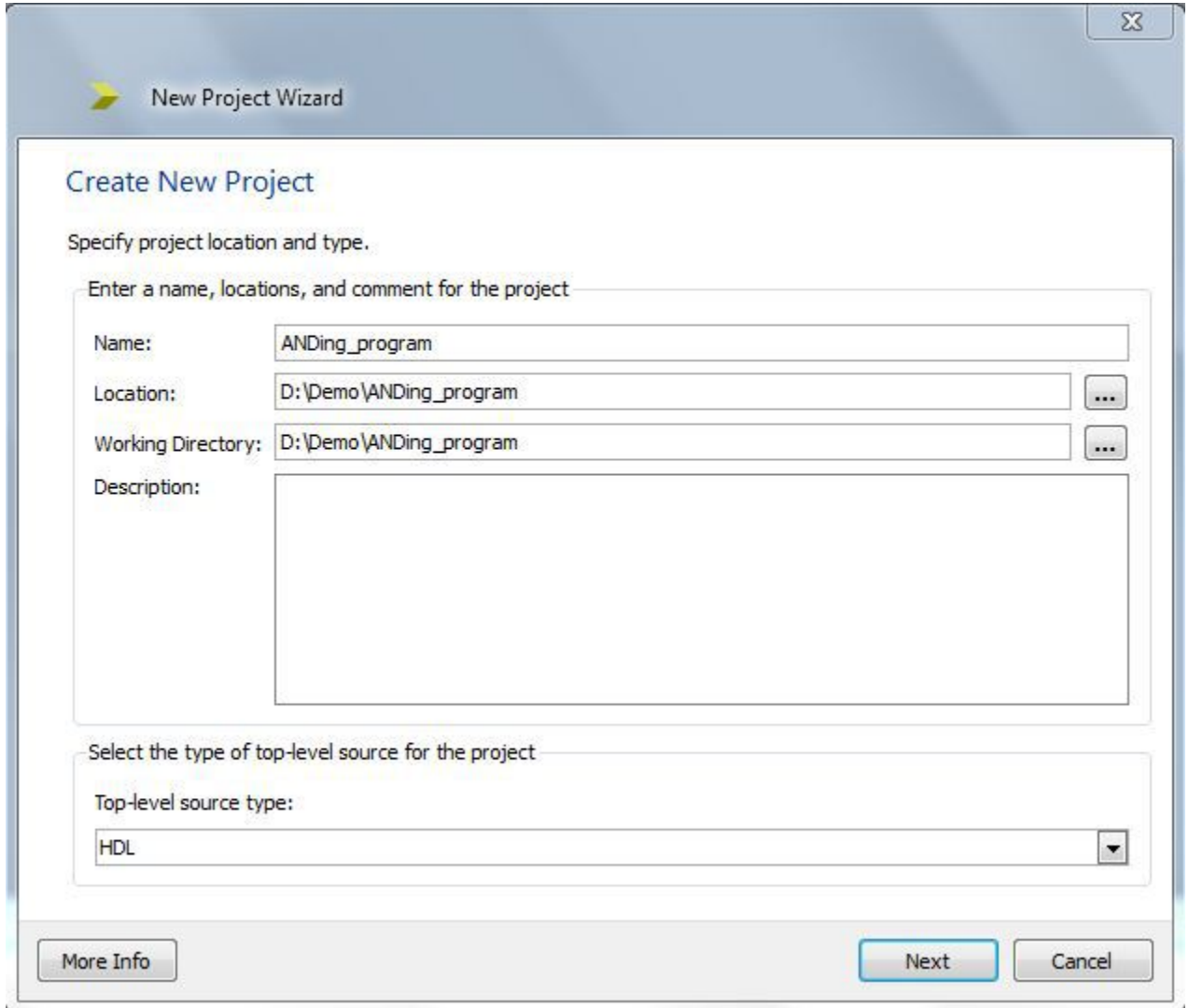


STEP1: Open Xilinx ISE and create a new project.

The image shows the 'New Project Wizard' dialog box in Xilinx ISE. The title bar says 'New Project Wizard' with a yellow arrow icon. The main heading is 'Create New Project'. Below it, the instruction 'Specify project location and type.' is shown. The first section, 'Enter a name, locations, and comment for the project', contains four fields: 'Name:' with the value 'ANDing_program', 'Location:' with 'D:\Demo\ANDing_program' and a browse button (...), 'Working Directory:' with 'D:\Demo\ANDing_program' and a browse button (...), and a large empty 'Description:' text area. The second section, 'Select the type of top-level source for the project', contains a 'Top-level source type:' dropdown menu currently set to 'HDL'. At the bottom, there are three buttons: 'More Info', 'Next' (highlighted with a blue border), and 'Cancel'.

Select path of your working project directory and enter name of project.

click on **Next**

Step 2: Select the Family, Device, Package and Speed of Xilinx board and also select your programming language(Verilog/VHDL). Here i am using Verilog language.

New Project Wizard

Project Settings

Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan6
Device	XC6SLX16
Package	CSG324
Speed	-3
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93

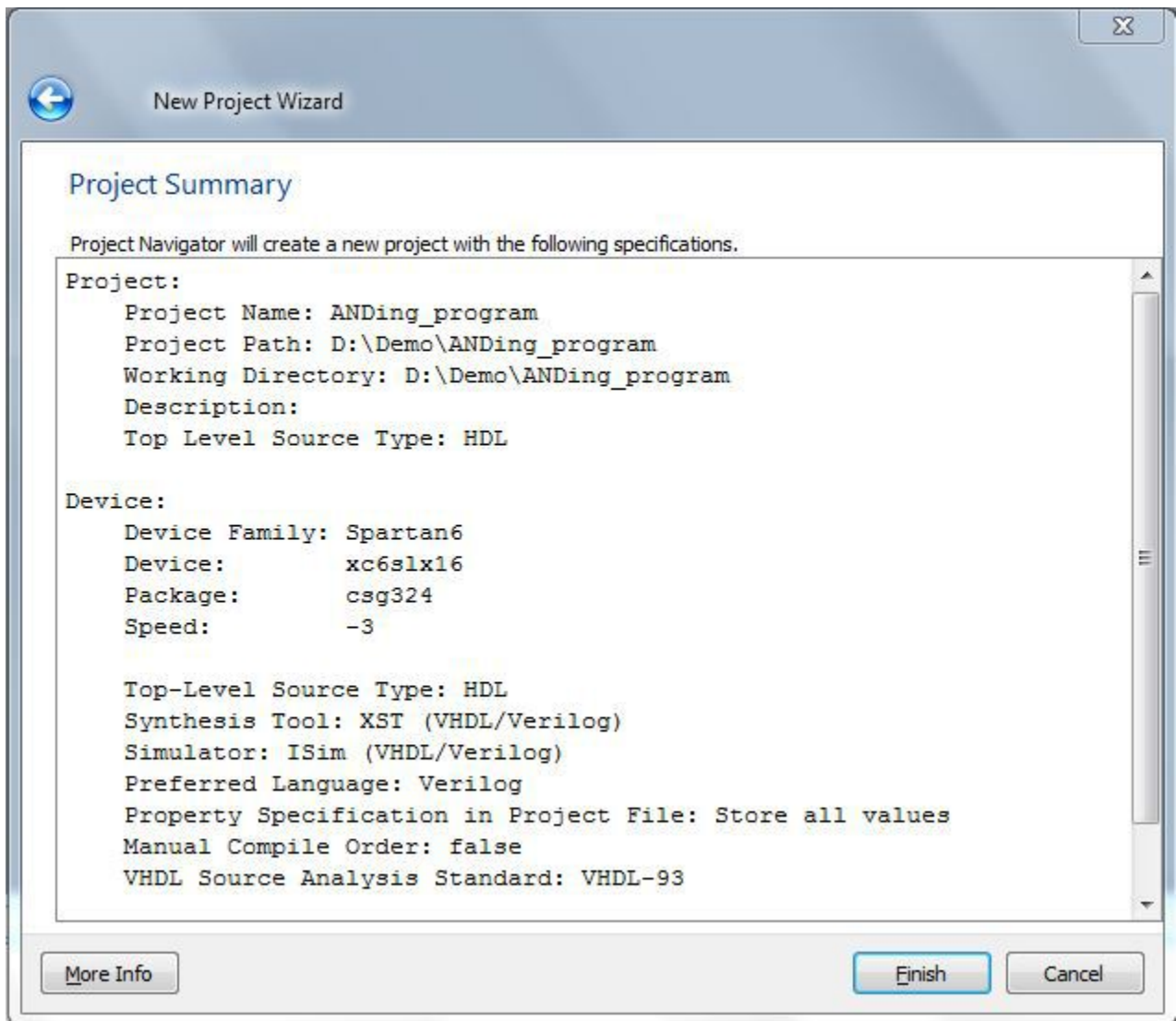
More Info

Next

Cancel

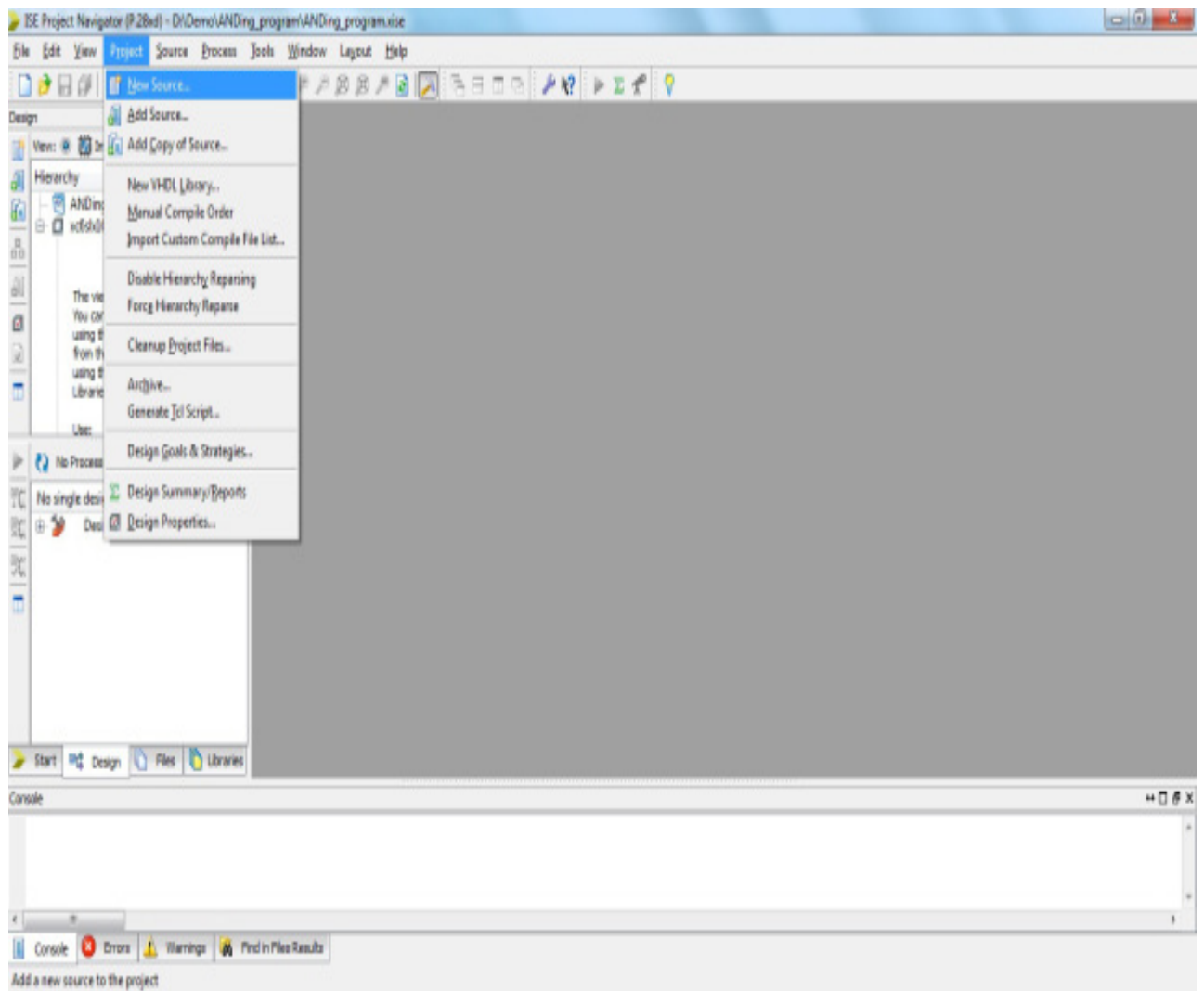
click on **Next**

Project summery window occurs.

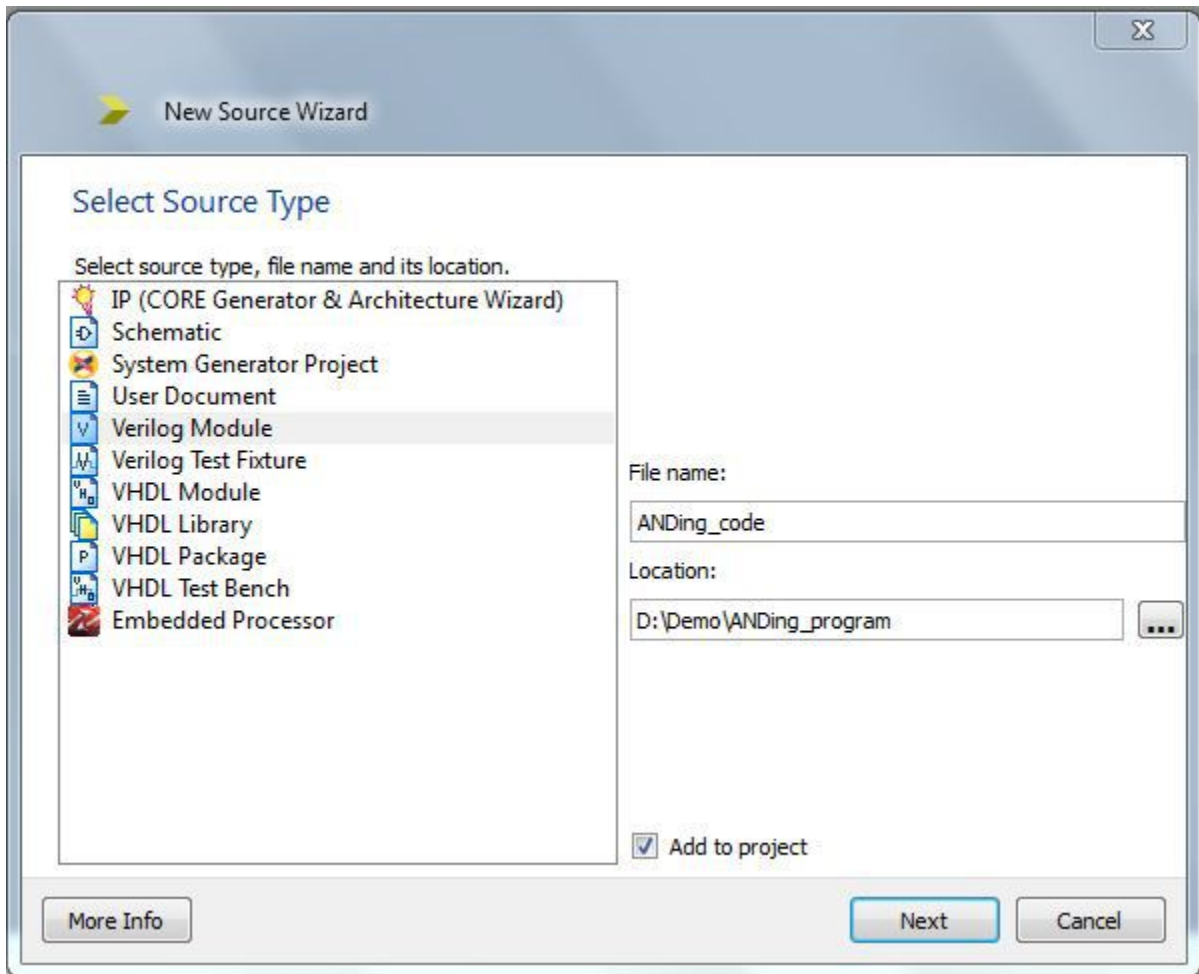


Click on **Finish**

Step 3: Click on **Project > New Source**





Step 4: Select Source type is **Verilog Module** and enter the file name (**ANDing_code**).



Click on **Next**

Step 5: Define Module Window.

Here we can define inputs & outputs and its bit/bus size. In ANDing example there are two inputs and output of single bit each. Also define clock signal for clocking operation.

New Source Wizard

Define Module

Specify ports for module.

Module name ANDing_code

Port Name	Direction	Bus	MSB	LSB
clk	input	<input type="checkbox"/>		
input_a	input	<input type="checkbox"/>		
input_b	input	<input type="checkbox"/>		
output_c	output	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		
	input	<input type="checkbox"/>		

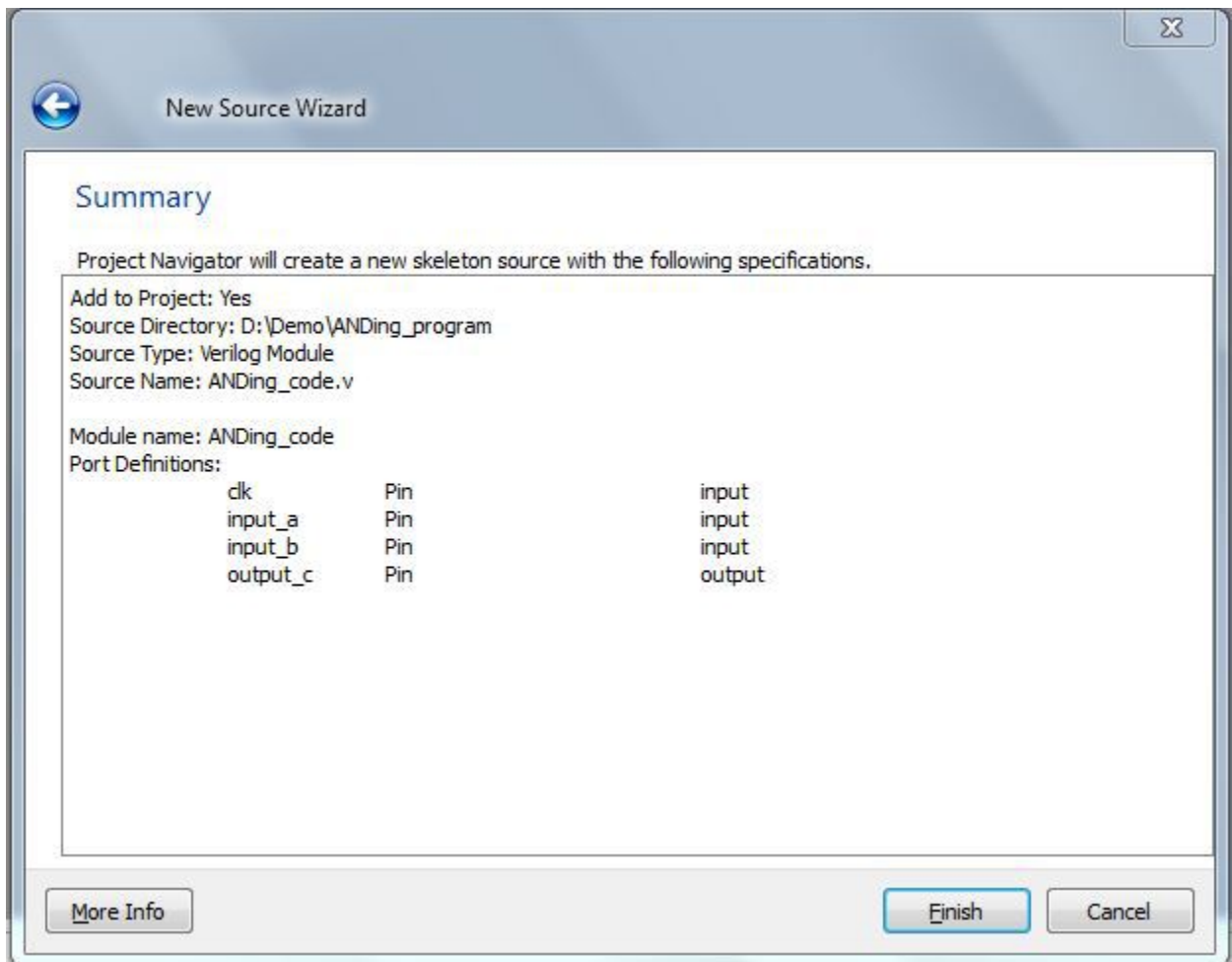
More Info

Next

Cancel

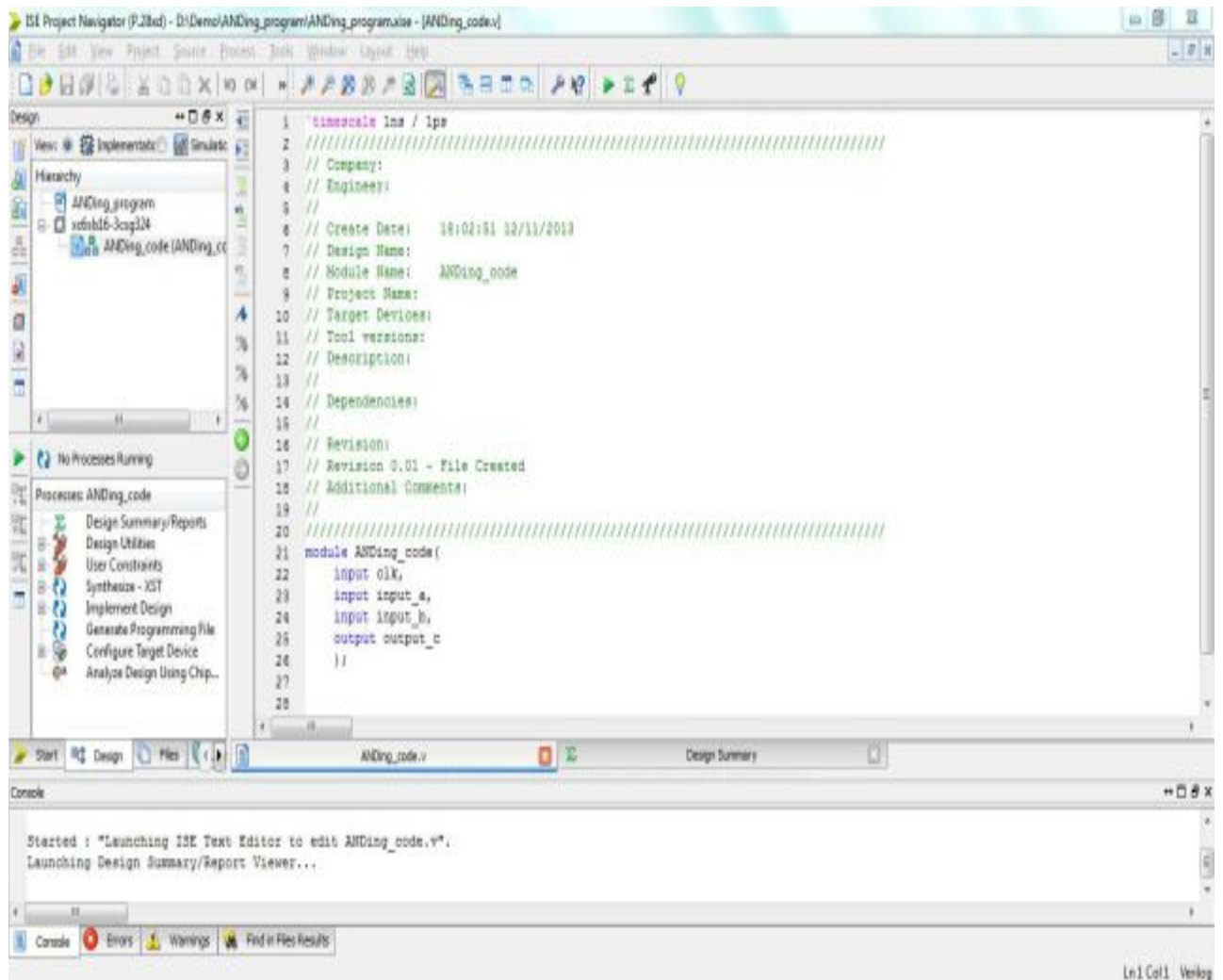
Click on **Next**.

Step 6: Summery Window



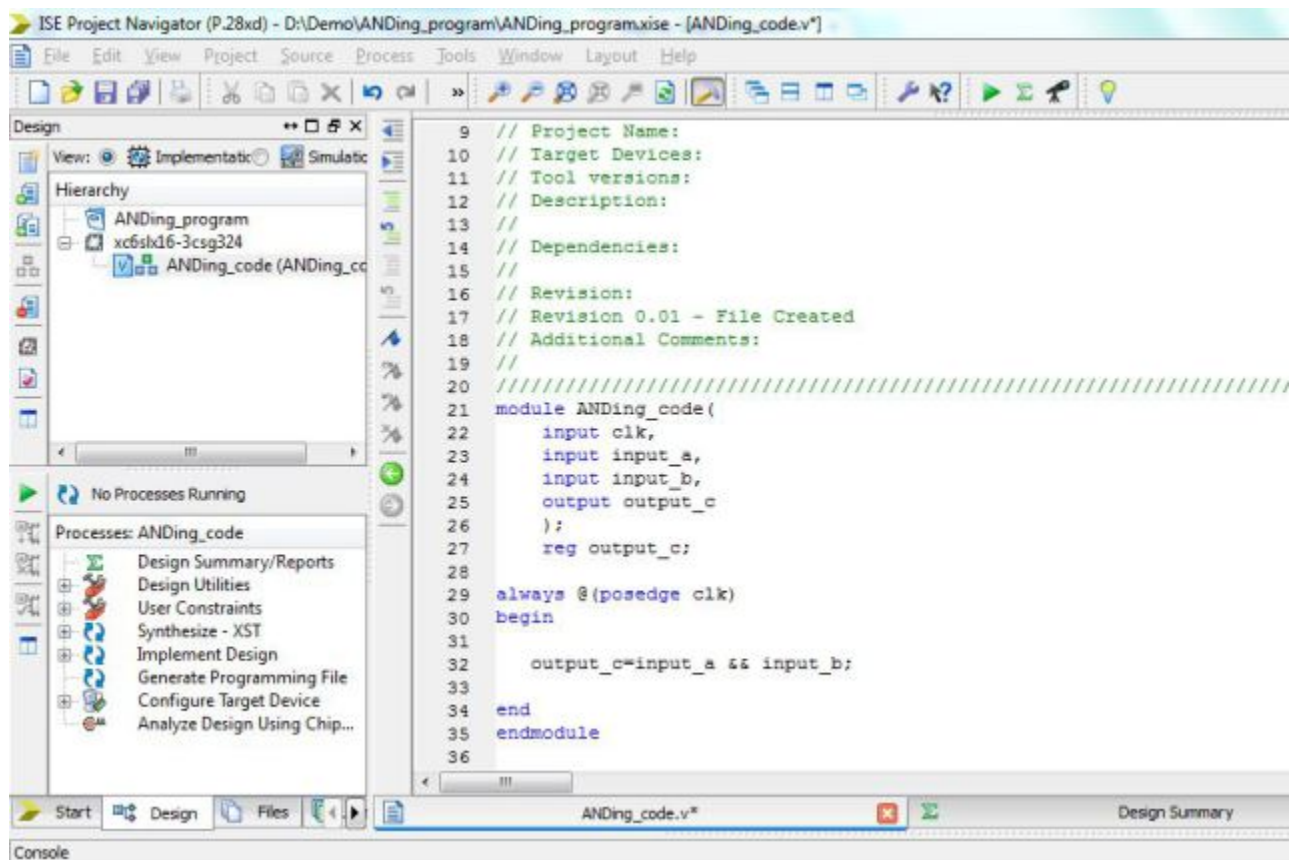
Click on **Finish**.

Step 7: The Project Navigator window looks like below window.

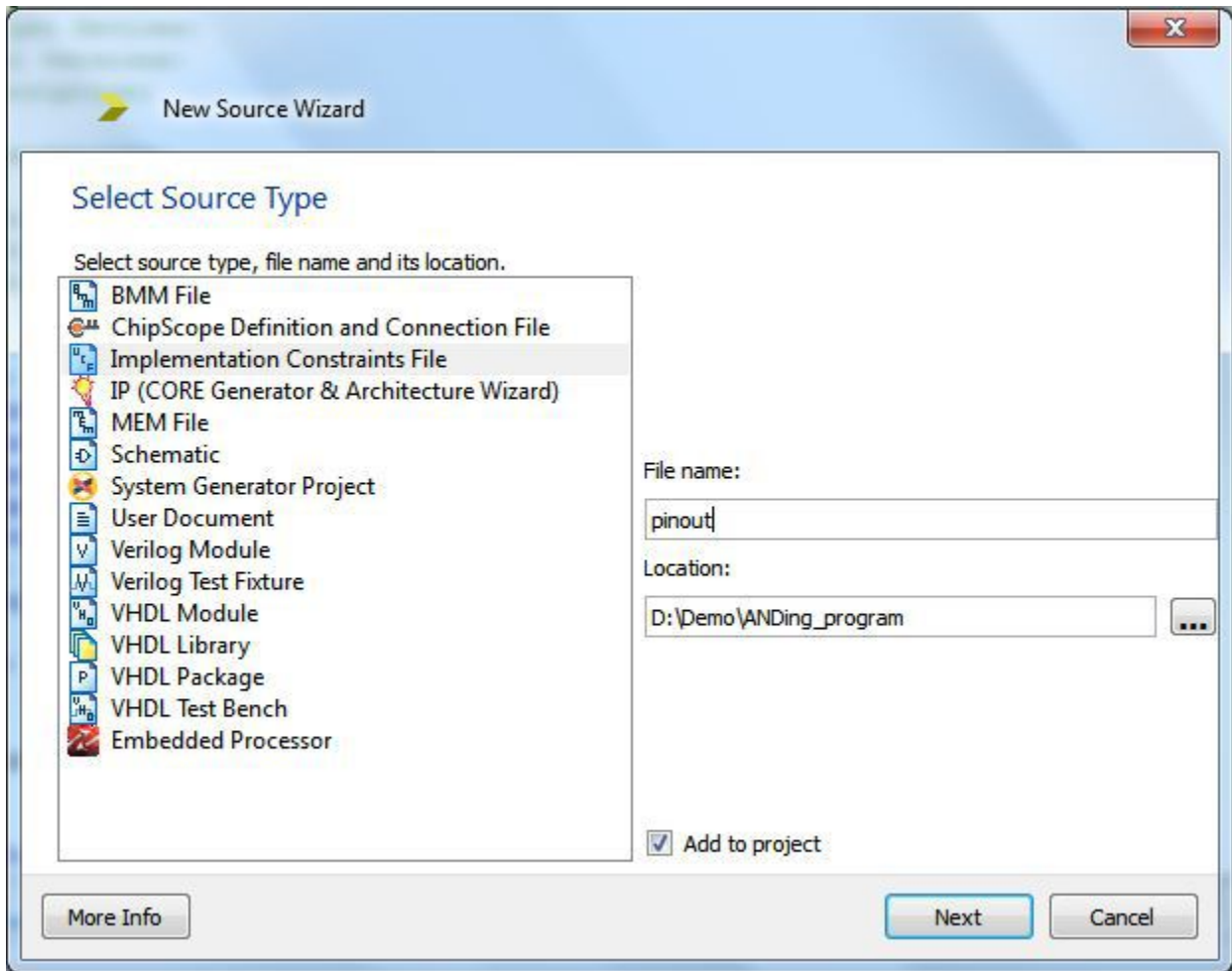


All the inputs and outputs are already defined in Define Module window so these inputs and outputs are seen in project navigator.

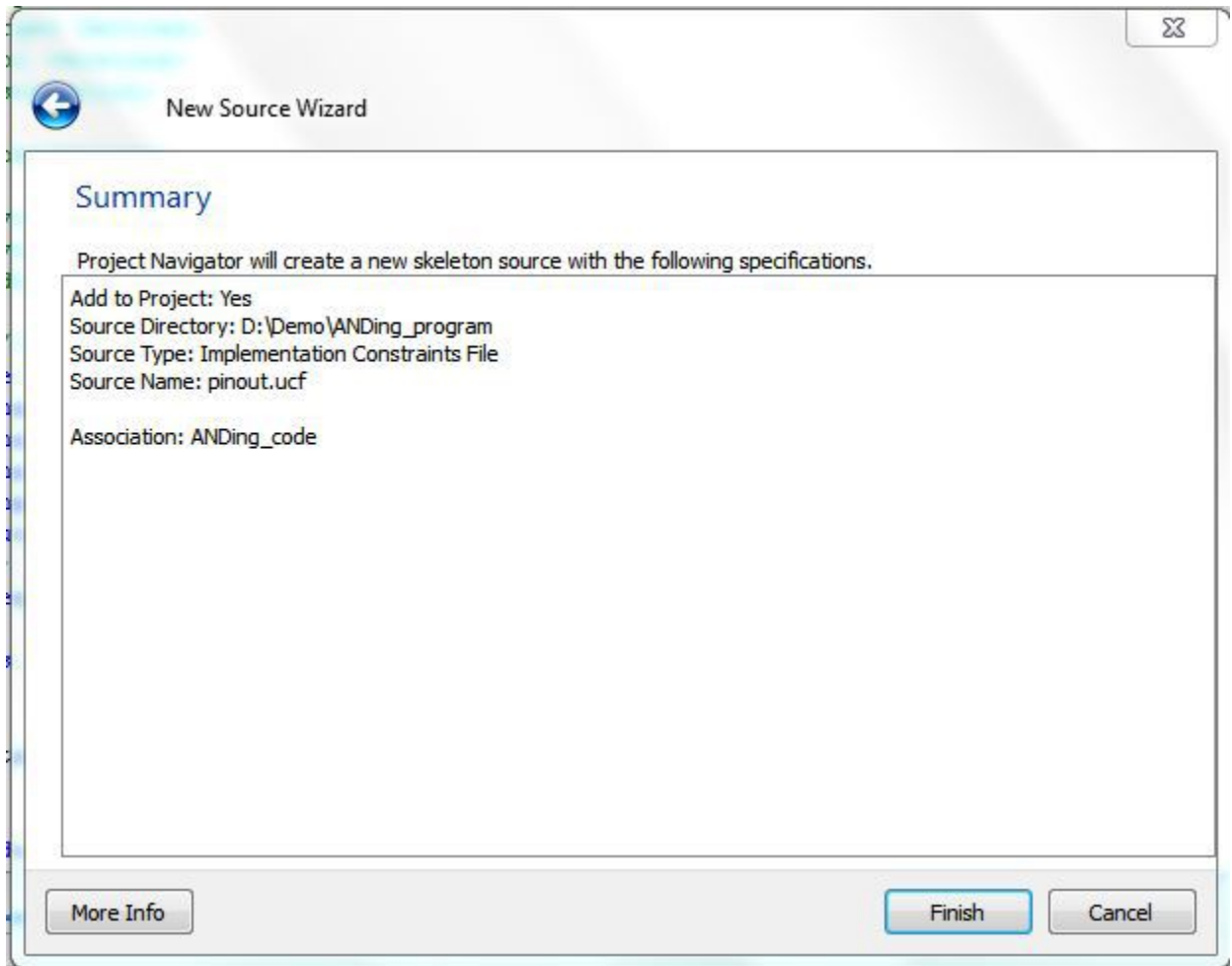
Step 8: Write a program for ANDing operator in module present in project navigator.



Step 9: Click on Project > New Source. Select Implementation Constraints file type and enter the file name (e.g. pinout).

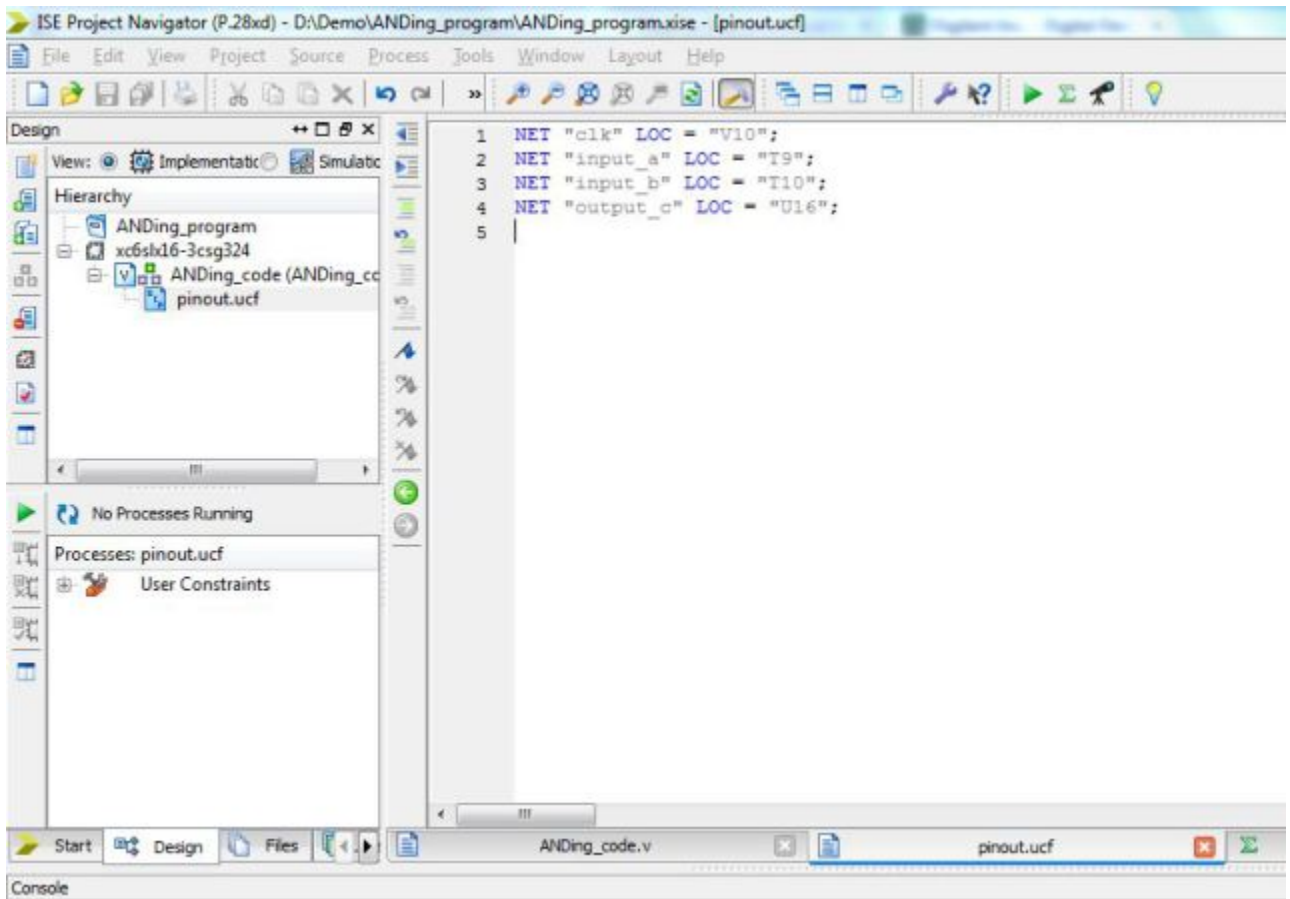


Click on Next.



Click on Finish.

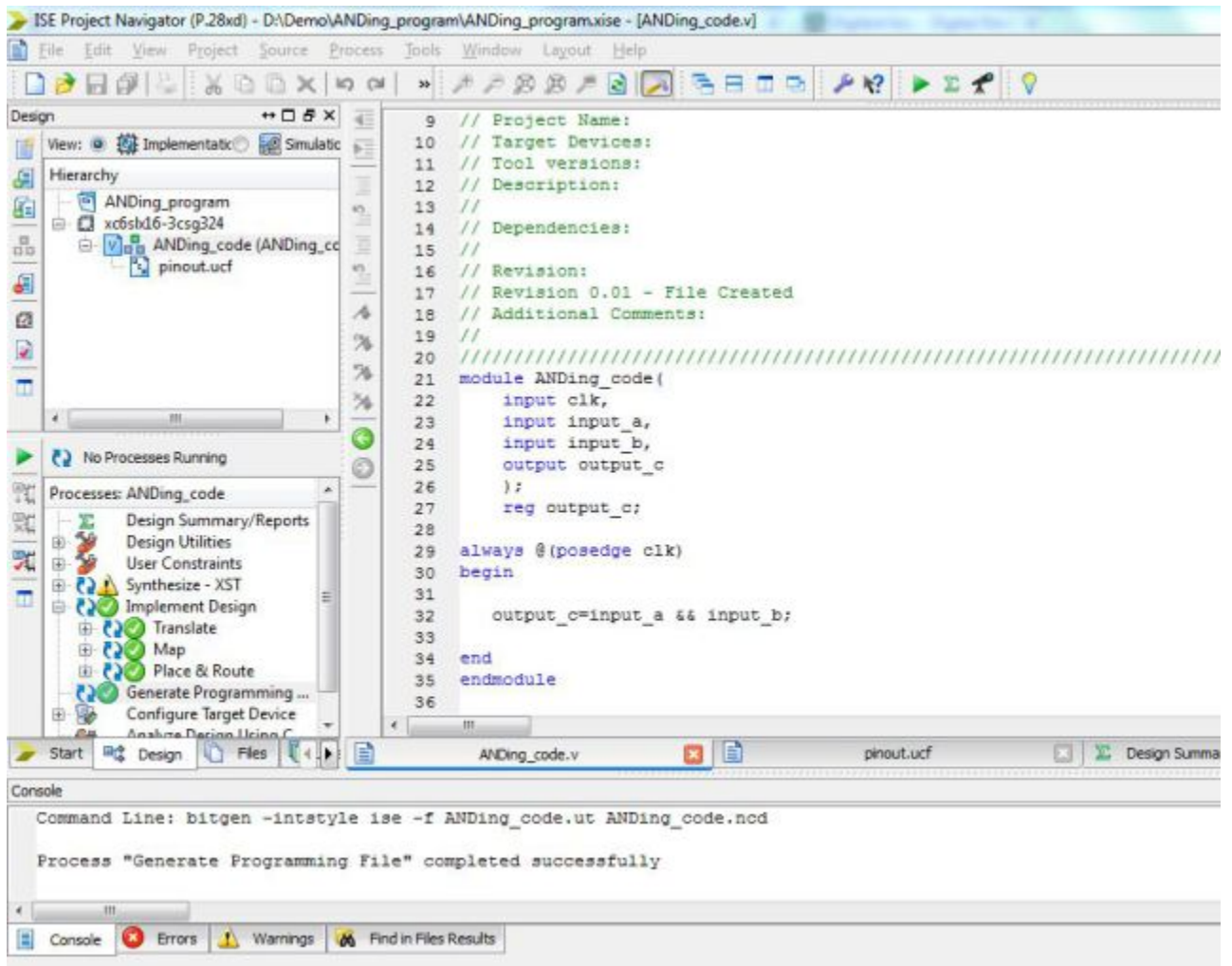
Step 10: Write the inputs, outputs and its pin location in proper format of **.ucf** file. (use datasheet of Xilinx board for pin location). Here two switches SW0 and SW1 are used for input and one led LD0 is used for output.



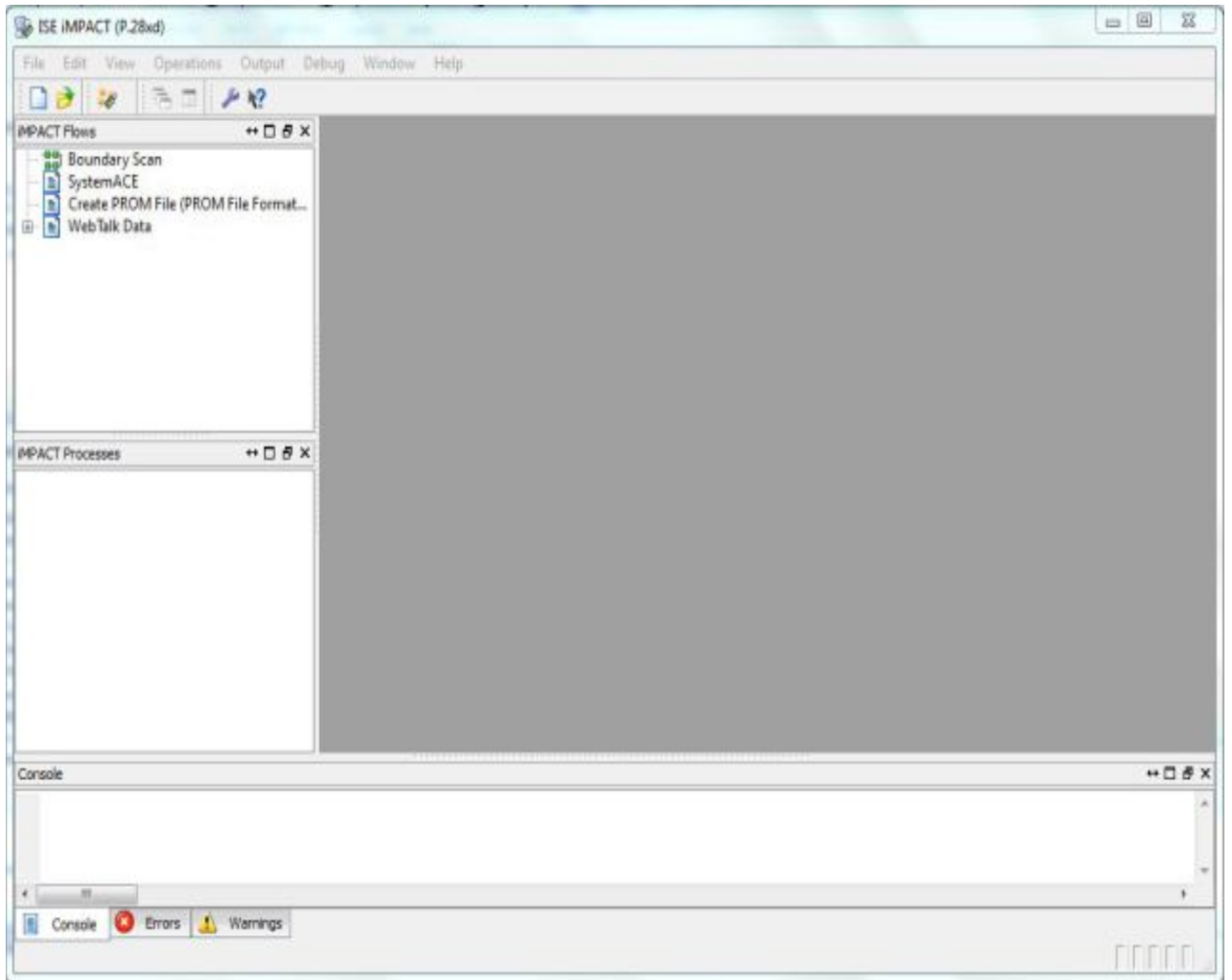
Step 11: Open main ANDing program and double click on Synthesize – XST. After successful completion of Synthesis, double click on Implement Design. Implement design consists of three parts-

- Translate
- Map
- Place and Route

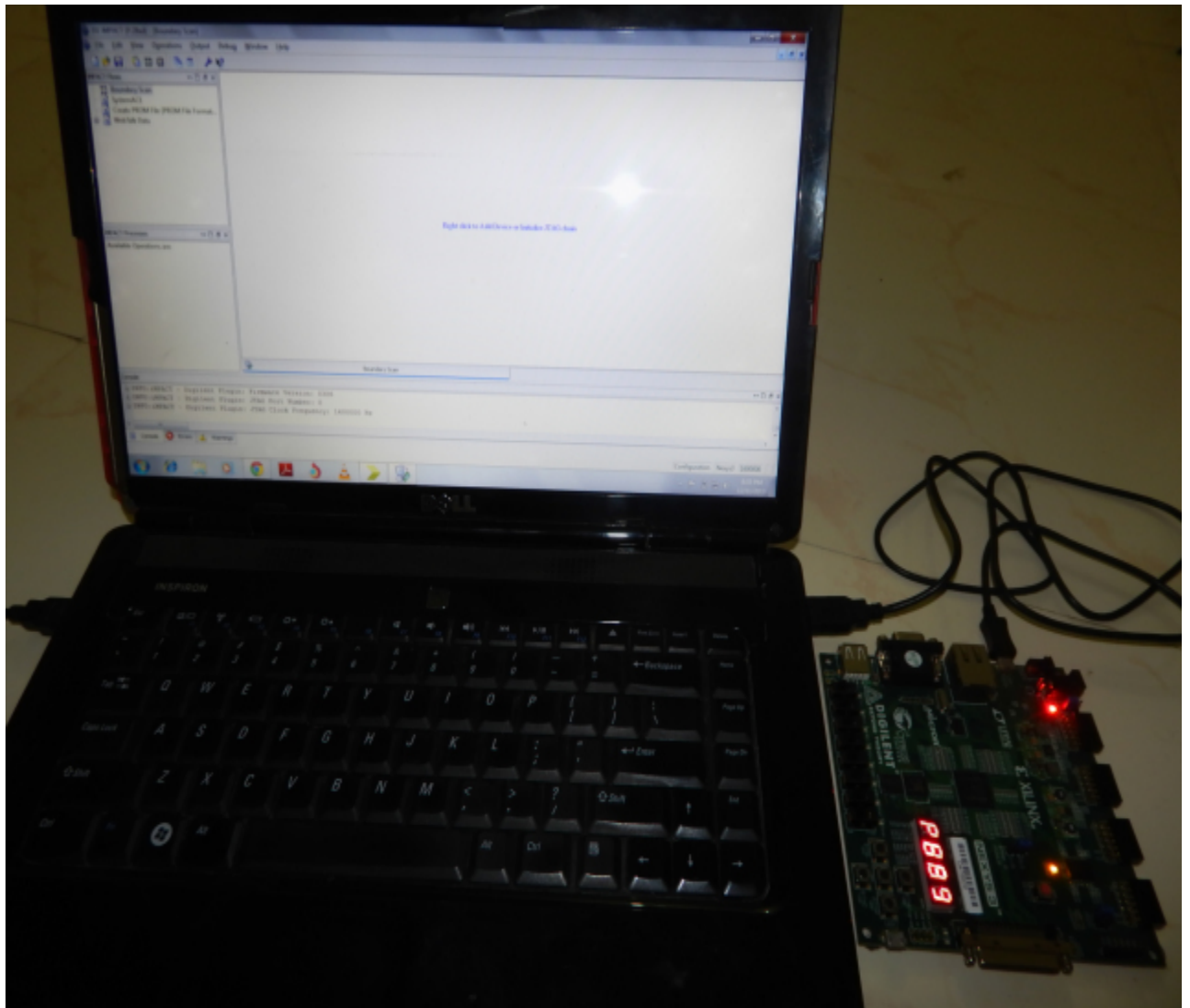
For detail information of Implement design [Click Here](#). After successful completion of implement design double click on Programming File Generation. Programming File Generation produces a bitstream for Xilinx device configuration. Successful completion of all these process the window looks like.



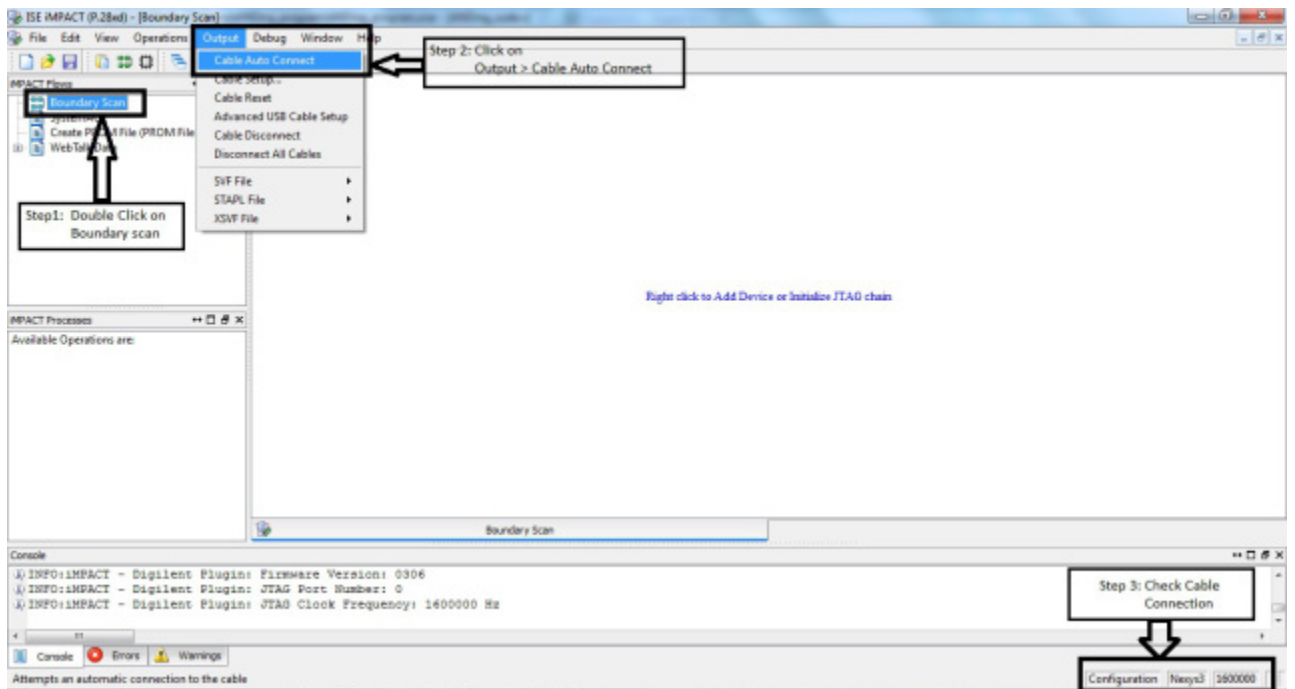
Step 12: Double click on **Configure Target Device** and a new **ISE iMPACT** window open.



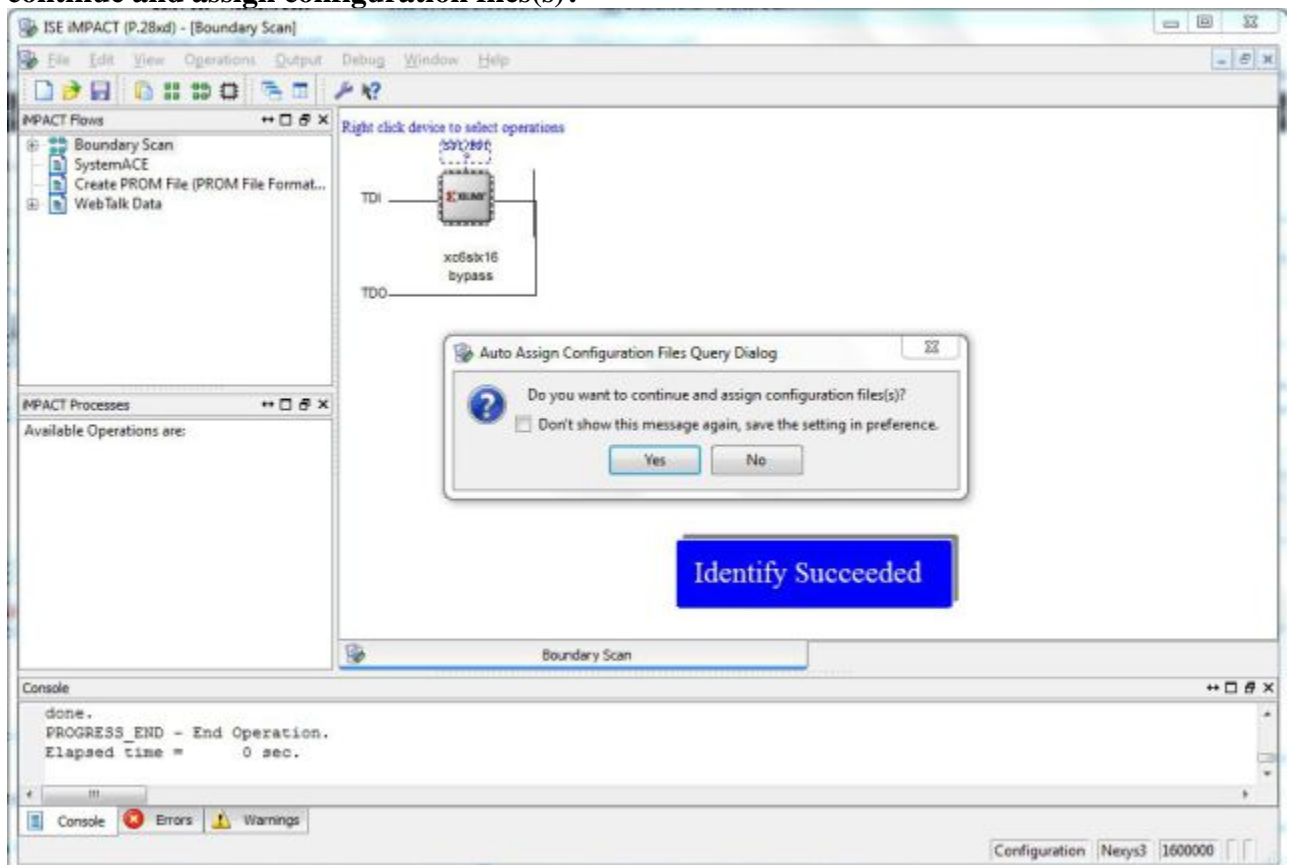
Step 13: Connect the Xilinx board to your PC/Laptop using USB cable.



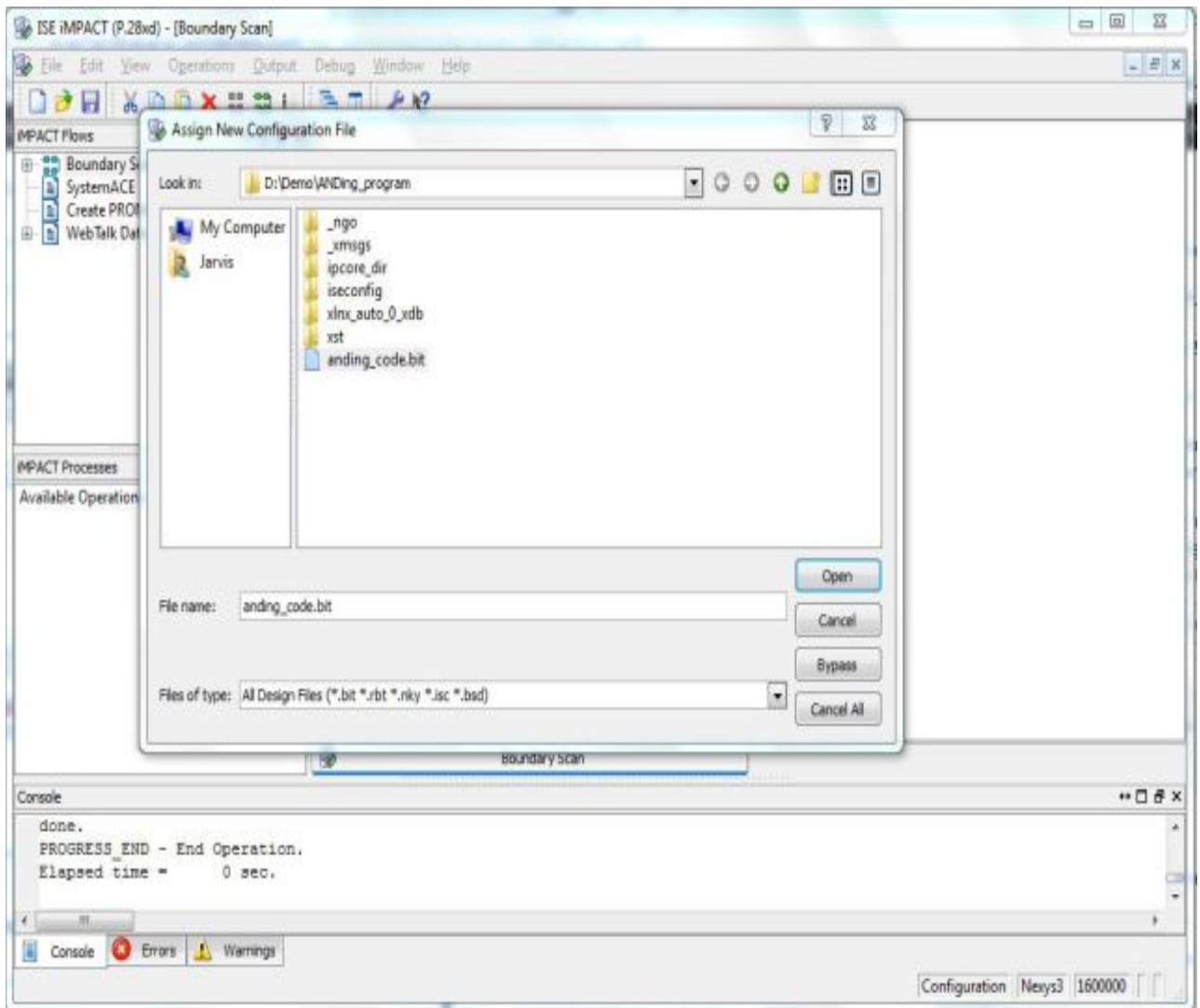
Step 14: Double click on Boundary scan. Check auto cable connection **Output > Cable Auto Connect** and if cable is connected then Window bottom part looks like step 3 shown in below.



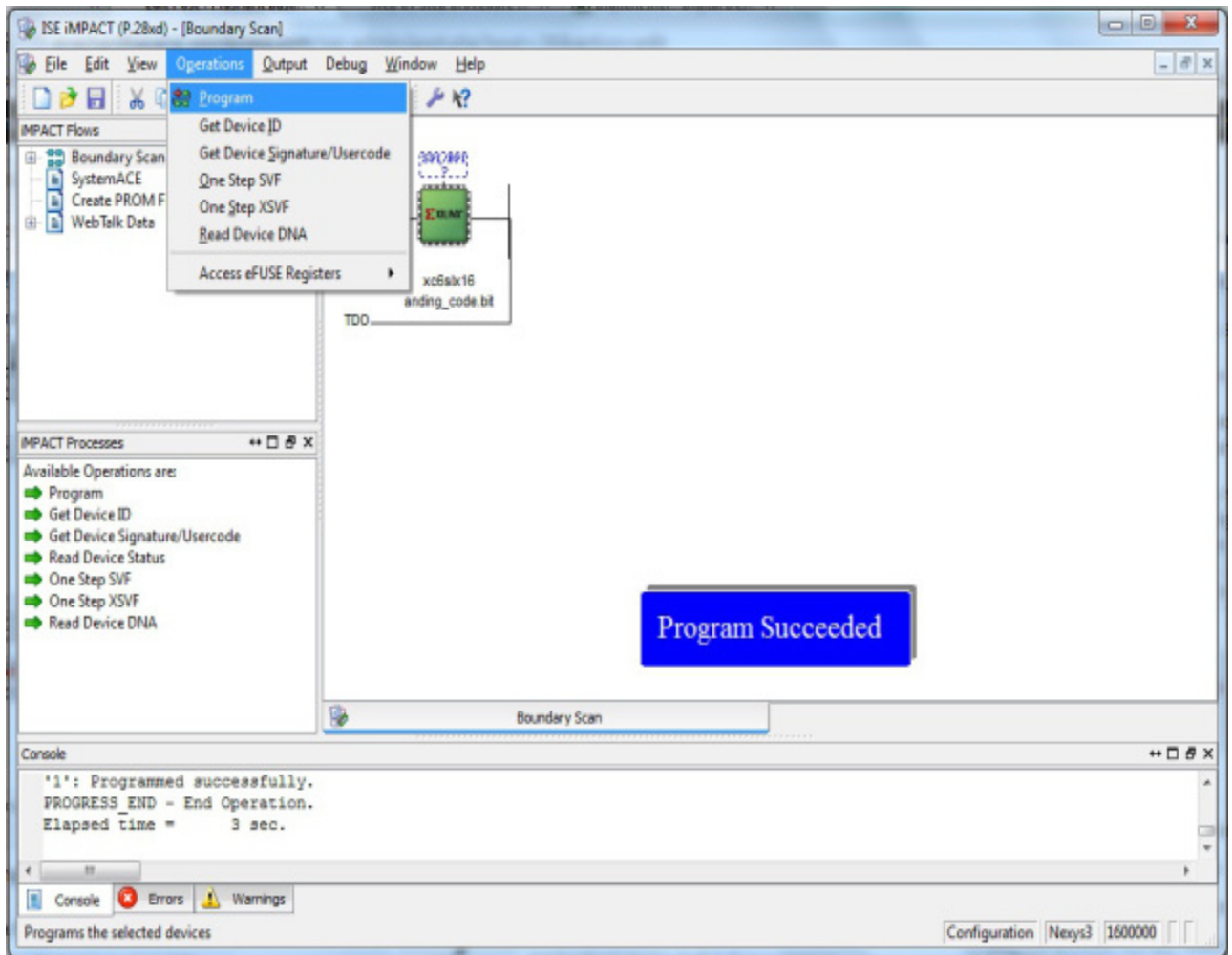
Step 15: Click on File > Initialize Chain. After that they ask for “Do you want to continue and assign configuration files(s)?”



Click on **Yes** and select the generated bit-stream file.



Step 16: Click on Open. After that they ask **“Do you want to attach an SPI or BPI PROM to this device?”** click on No tab. Click on **Operations > Program**. If Programming successful then they shows **Program Succeeded**.



Step 17: Check the output on hardware(Board). Here I am giving input through switches and output shows on LED. Output:

1. Switch1(OFF) AND Switch2(OFF) = LED(OFF)
2. Switch1(ON) AND Switch2(OFF) = LED(OFF)
3. Switch1(OFF) AND Switch2(ON) = LED(OFF)
4. Switch1(ON) AND Switch2(ON) = LED(ON)