

CPE 151
Digital IC Design

Project No.1

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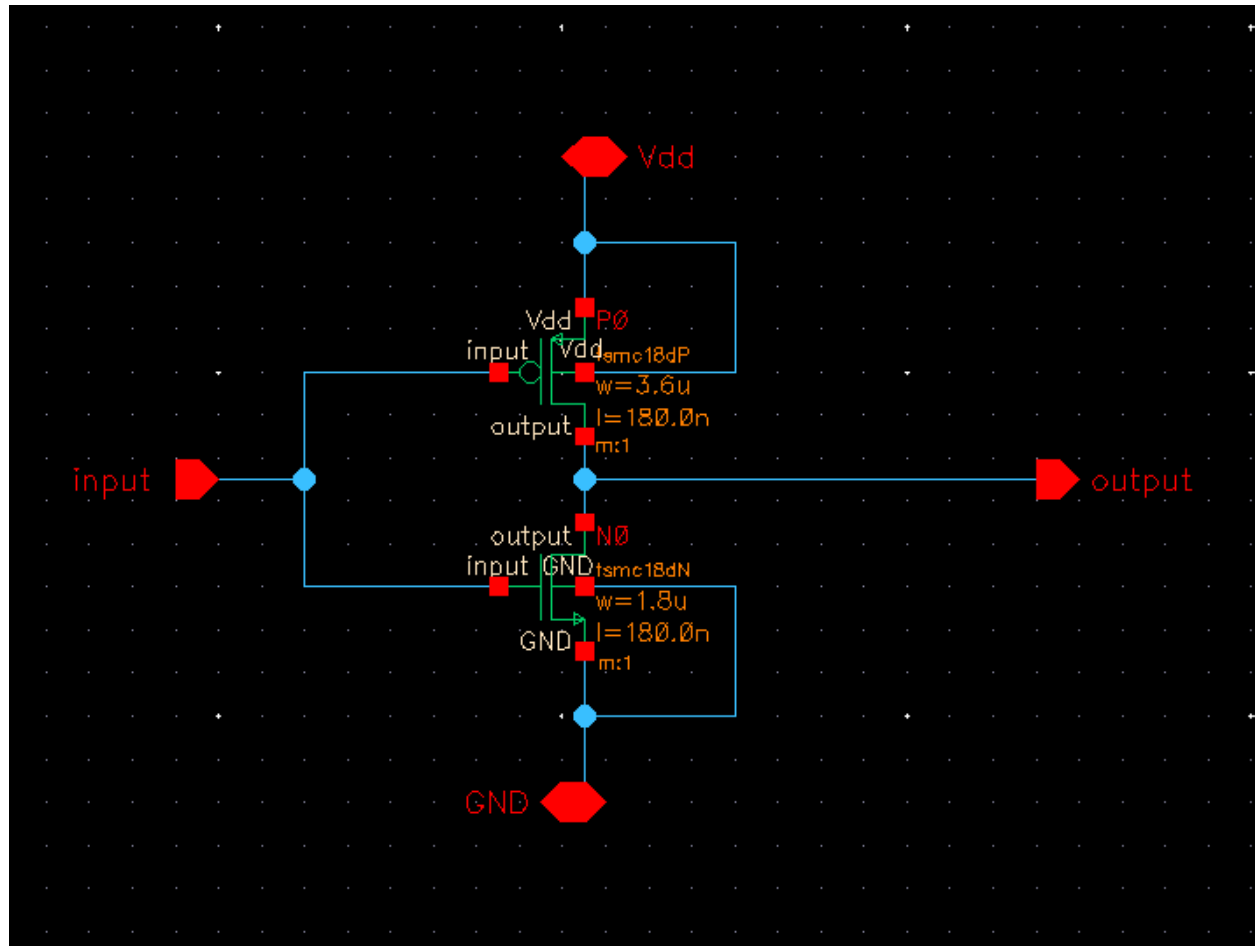
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Inverter

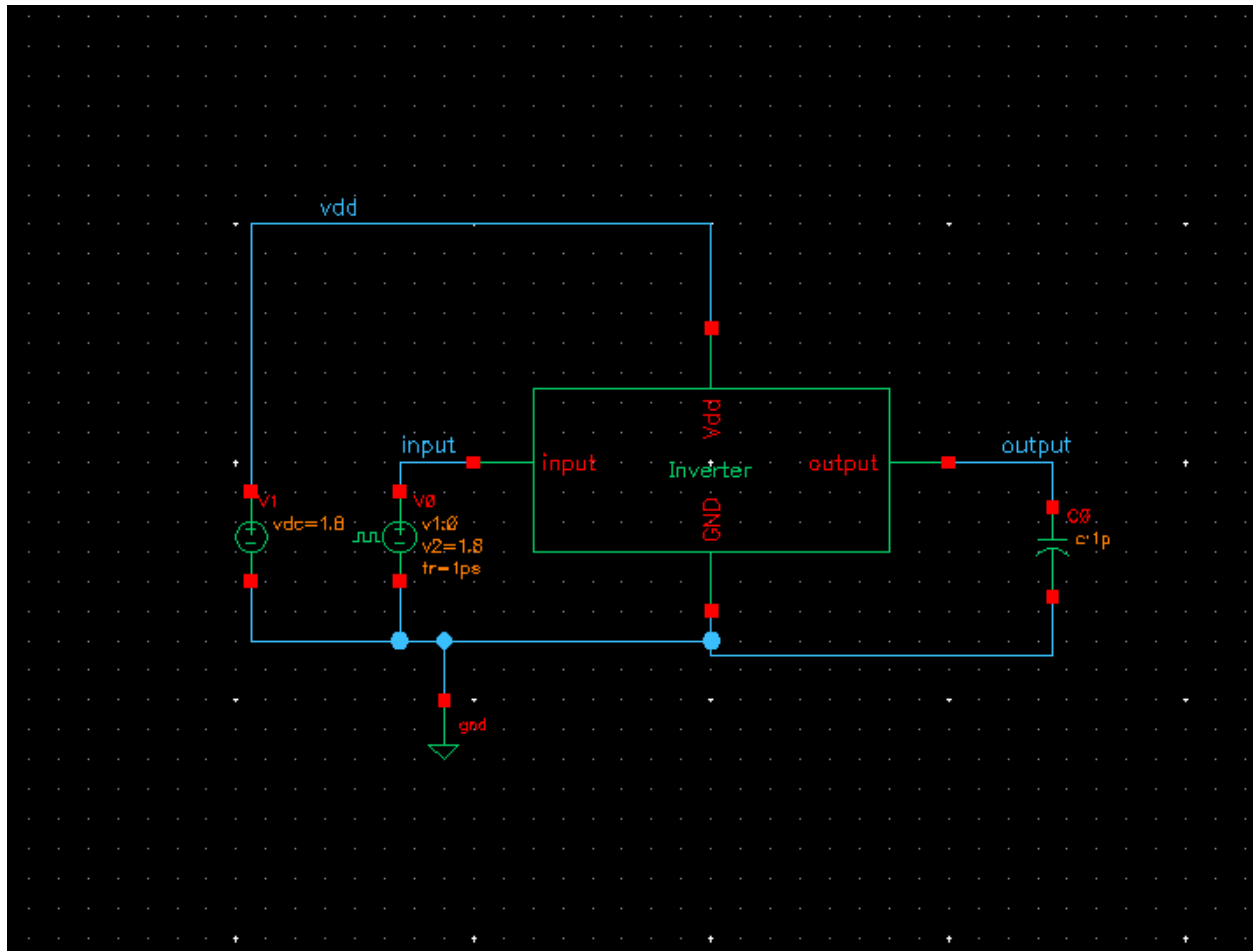
$$(W/L)_n = 1.8/.18$$

$$(W/L)_p = 3.6/.18$$

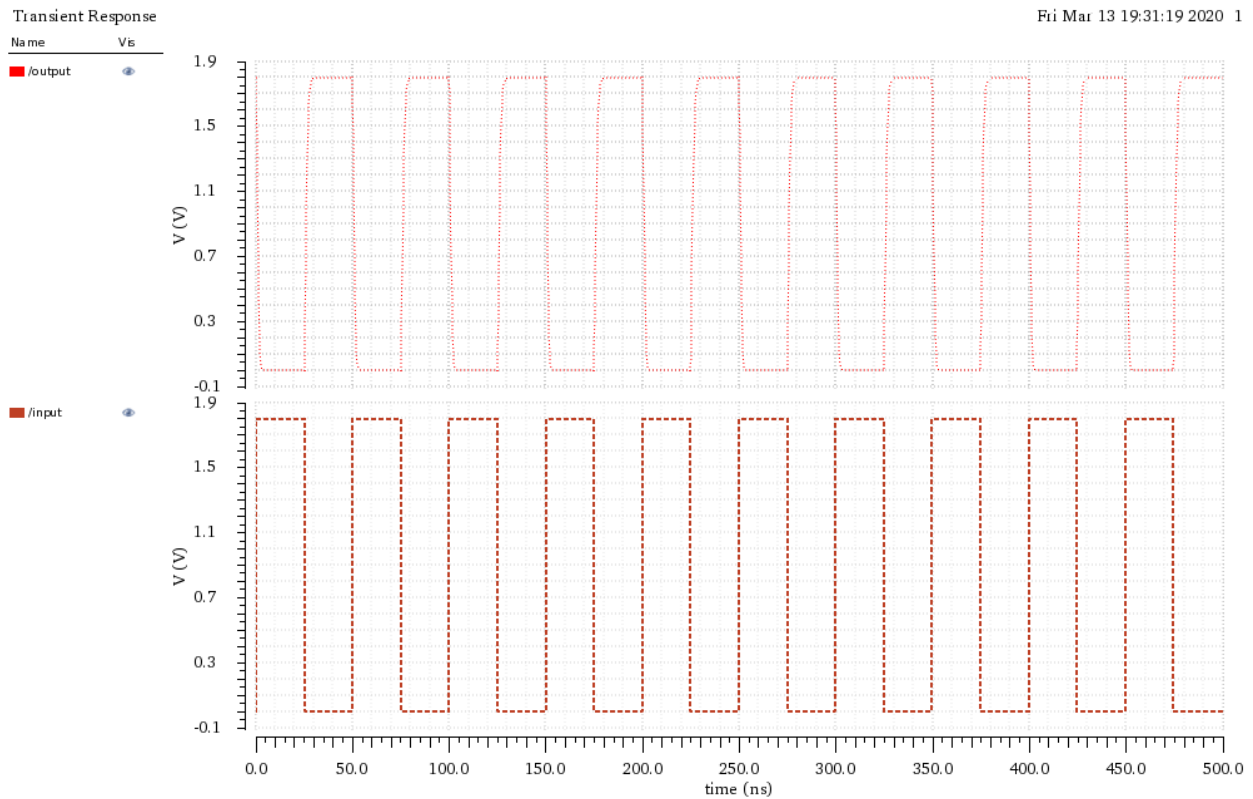
Schematic(Inverter):



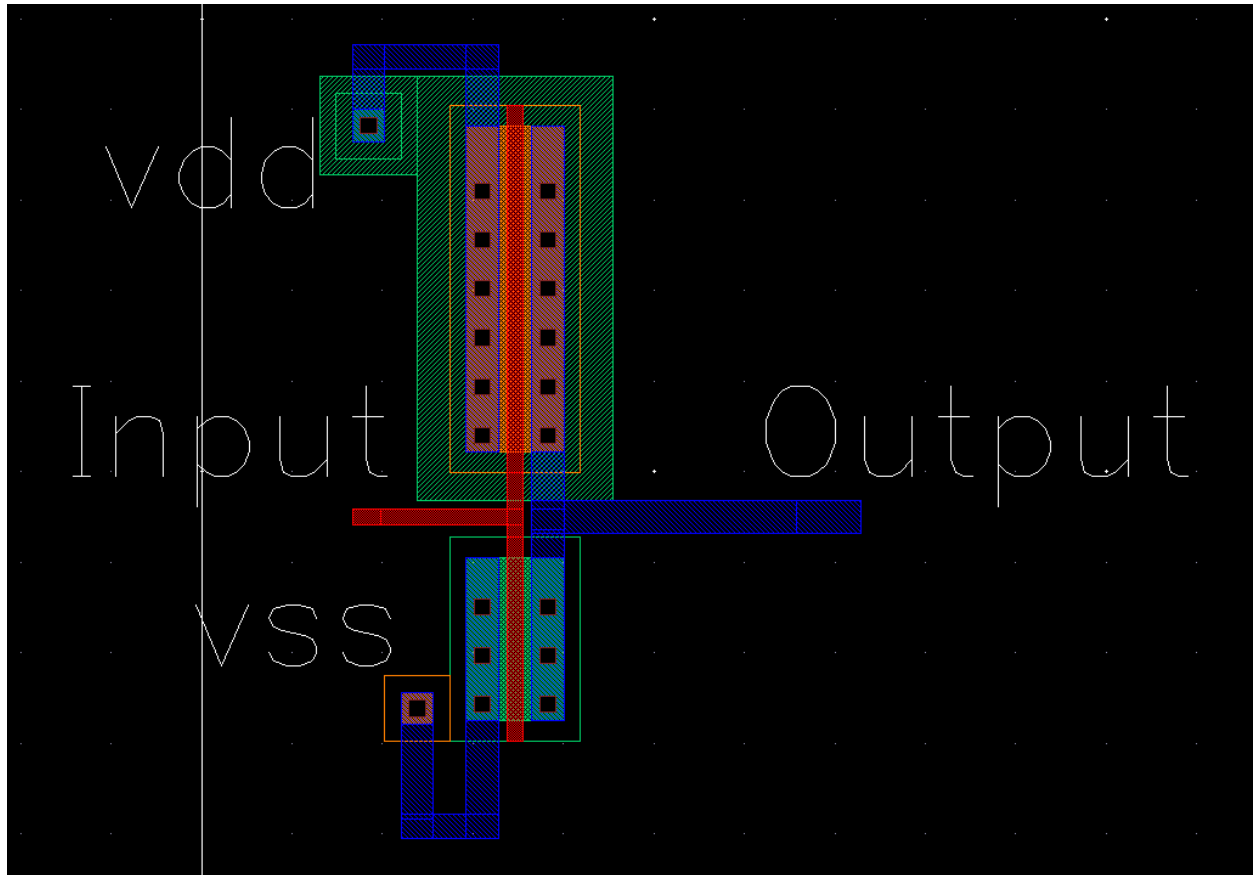
Test Bench(Inverter):



Test Bench Waveform(Inverter):



Layout (Inverter):



LVS(Inverter):

@(#)CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/installs/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/komacd/CadDemo/LVS -l -s -t /gaia/class/student/komacd/CadDemo/LVS/layout
/gaia/class/student/komacd/CadDemo/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/komacd/CadDemo/LVS/layout/netlist

count

4	nets
4	terminals
1	pmos
1	nmos

Net-list summary for /gaia/class/student/komacd/CadDemo/LVS/schematic/netlist

count

4	nets
4	terminals
1	pmos
1	nmos

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists failed to match.

layout schematic

instances

un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

nets

un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4

terminals

un-matched	4	4
matched but		
different type	0	0
total	4	4

Probe files from /gaia/class/student/komacd/CadDemo/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

T -1 GND /GND

? Terminal GND in the schematic is not present in the layout.

T -1 Vdd /Vdd

? Terminal Vdd in the schematic is not present in the layout.

T -1 input /input

? Terminal input in the schematic is not present in the layout.

T -1 output /output

? Terminal output in the schematic is not present in the layout.

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/komacd/CadDemo/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

T -1 Input /Input

? Terminal Input in the layout is not present in the schematic.

T -1 Output /Output

? Terminal Output in the layout is not present in the schematic.

T -1 vdd /vdd

? Terminal vdd in the layout is not present in the schematic.

T -1 vss /vss

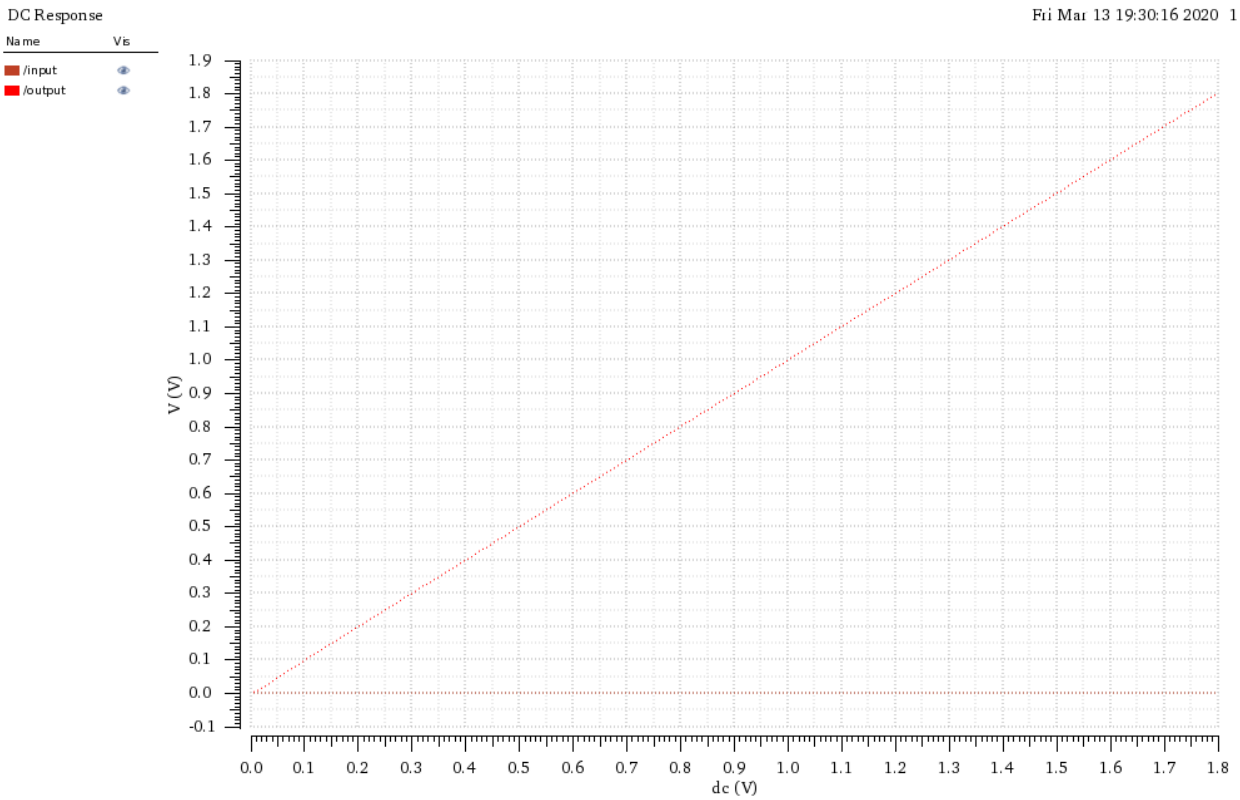
? Terminal vss in the layout is not present in the schematic.

prunenet.out:

prunedev.out:

audit.out:

Post Layout-Simulation(Inverter):



Conclusion:

S. No.	Description	Rise Time(us)	Fall Time(us)	Delay Time(us)
1.	Inverter	0us	0.001us	0us