CPE 151

Digital IC Design

Project No.2

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3input NAND

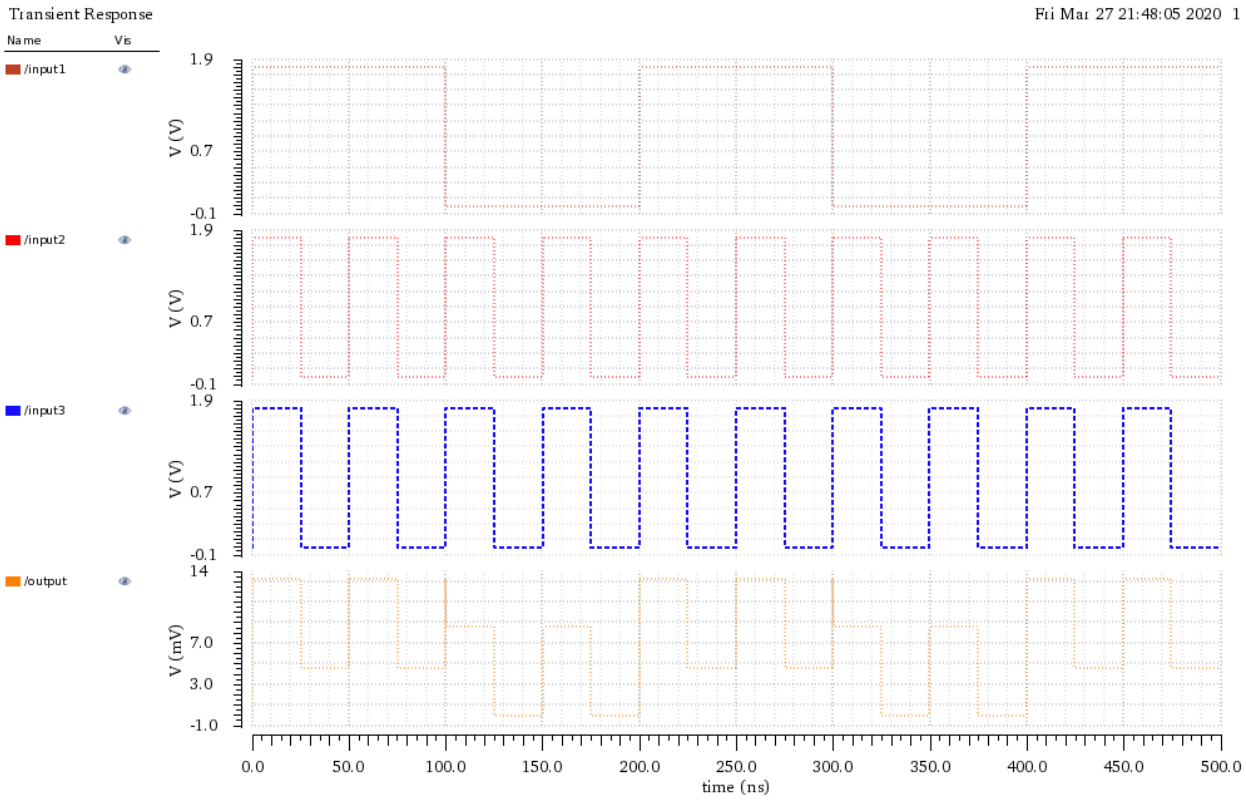
(W/L)_n = 1.8/.18

(W/L)_p=3.6/0.18

Schematic(3input NAND):

Test Bench(3input NAND):

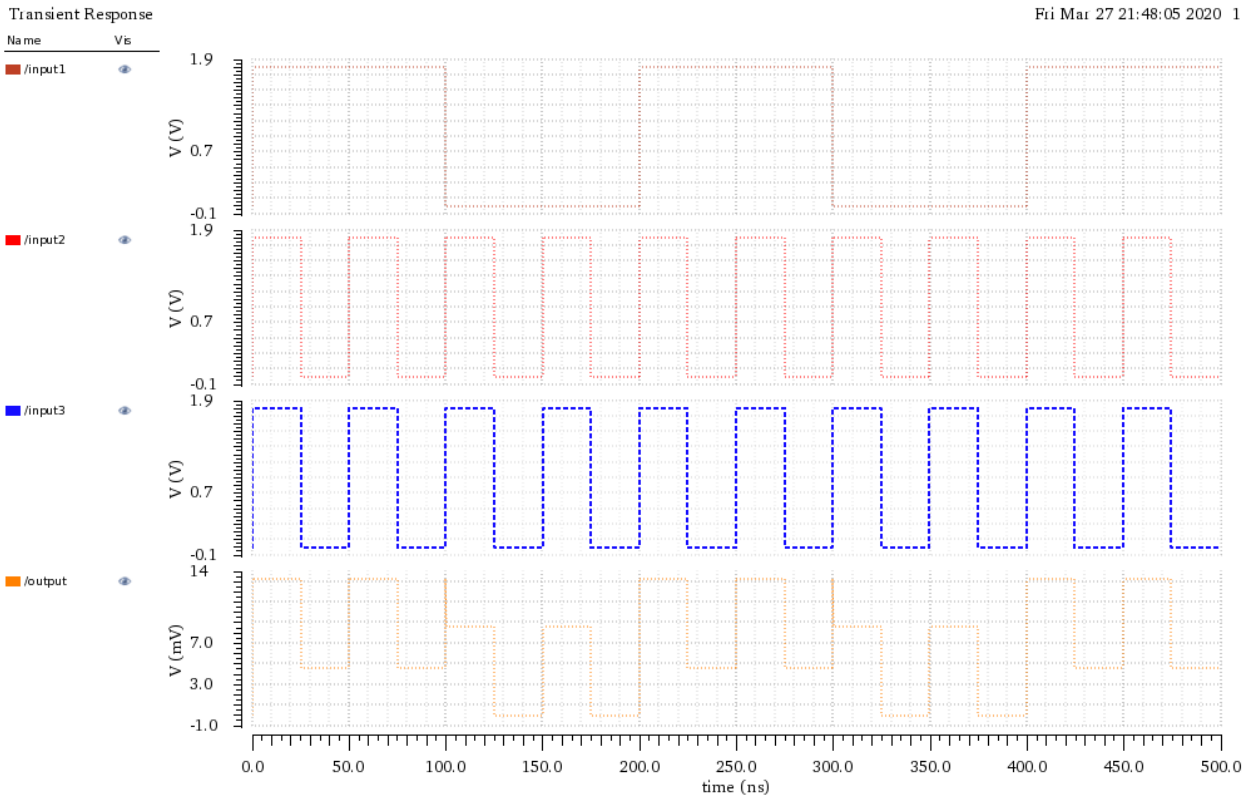
Test Bench Waveform(3input NAND):



Layout (3input NAND):

LVS(3input NAND):

Post Layout-Simulation(3input NAND):



Conclusion:

S. No.	Description	Rise Time(us)	Fall Time(us)	Delay Time(us)
1.	3input NAND	.001us	0us	0us