

CPE 151
Digital IC Design

Project No.3

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4/2/2020

Contents

S. No	Section	Page No.
1.	Ring Oscillator Schematic	5
2.	Ring Oscillator Test bench	6
3.	Ring Oscillator Test bench Waveform	7
4.	Ring Oscillator Layout	8
5.	Ring Oscillator DRC	9
6.	Ring Oscillator LVS	10
7.	Ring Oscillator Post-layout	12

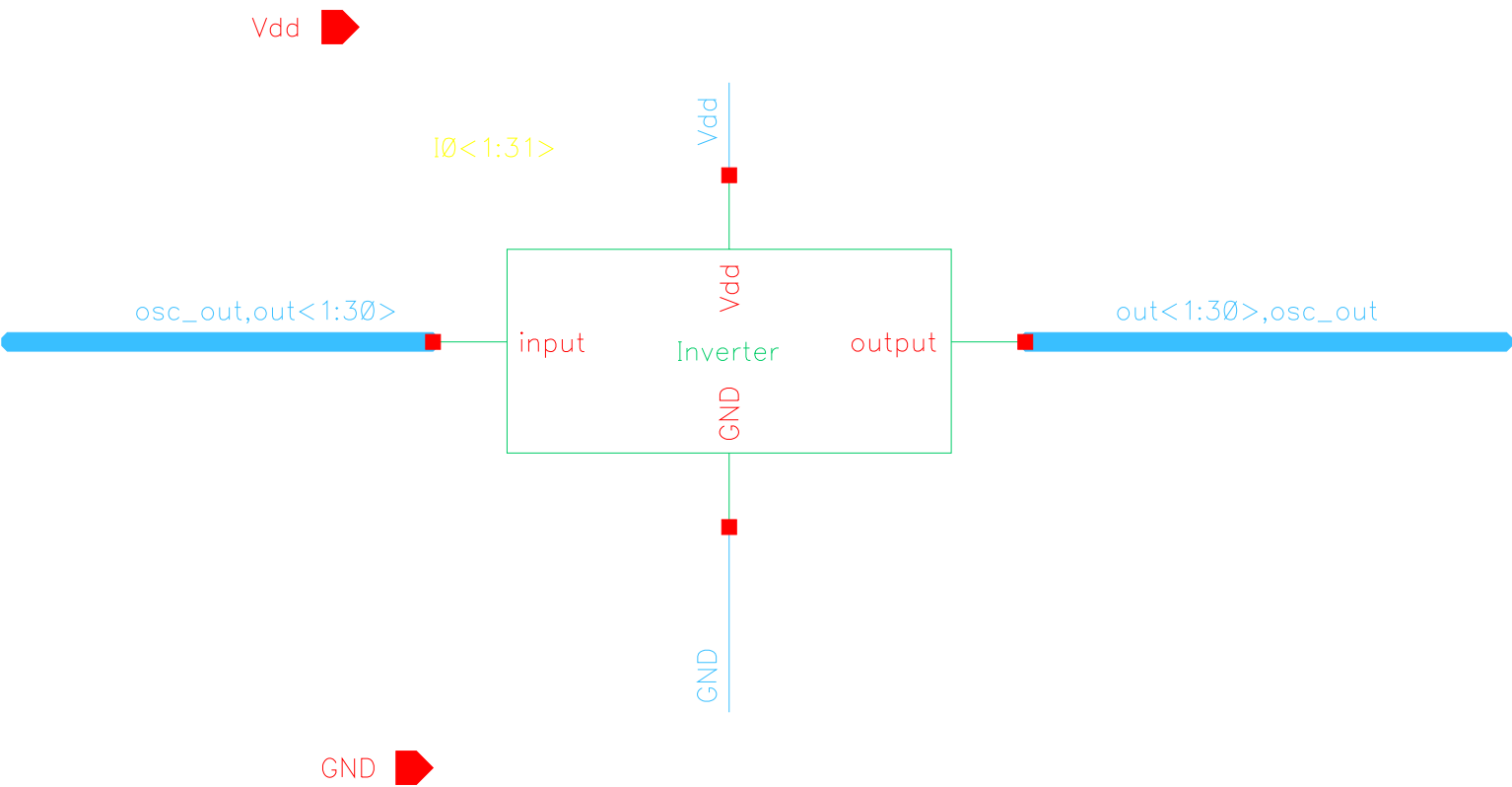
Ring Oscillator

$(W/L)_n = 1.8/.18$

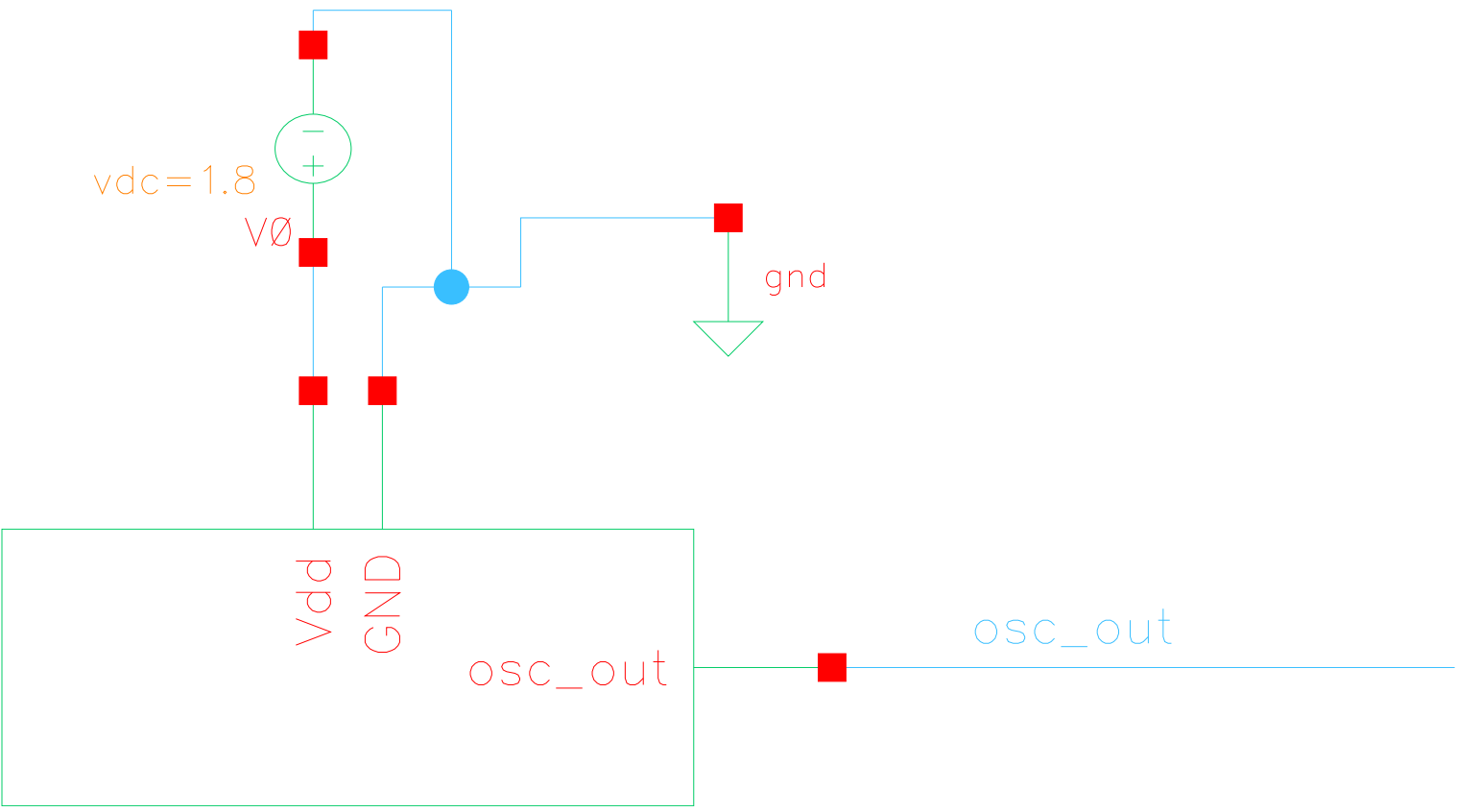
$(W/L)_p = 3.6/0.18$

Using 180 nm Technology

Schematic (Ring Oscillator):




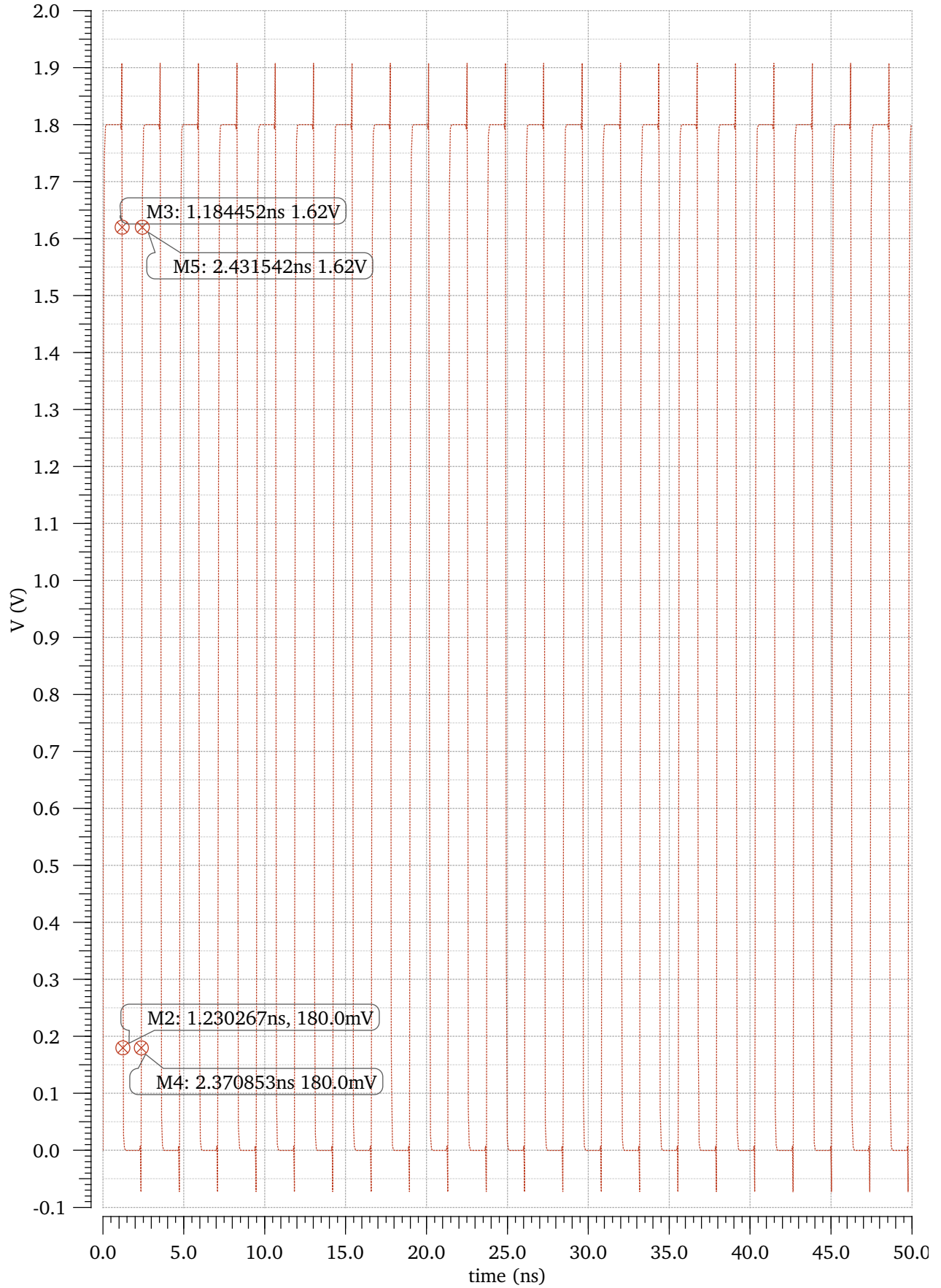
Test Bench (Ring Oscillator):



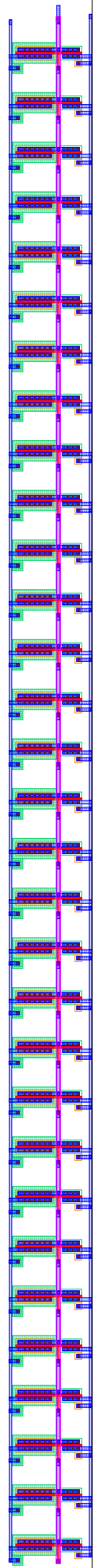
Test Bench Waveform (Ring Oscillator):

Transient Response**Thu Apr 2 14:14:29 2020**

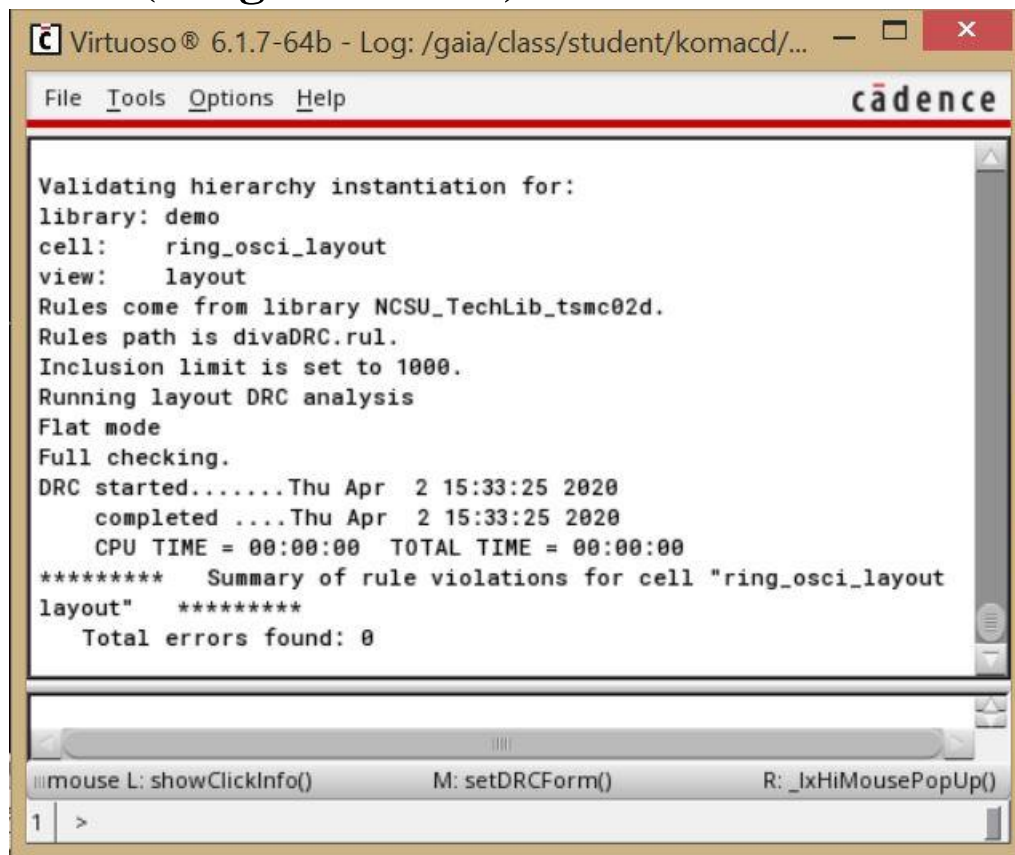
Name	Vis
/osc_out	



Layout (Ring Oscillator):



DRC (Ring Oscillator):



LVS (Ring Oscillator):

```

1: @(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
2:
3: Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/komacd/CadDemo/LVS -l -s -t /
  aia/class/student/komacd/CadDemo/LVS/layout /gaia/class/student/komacd/CadDemo/LVS/schematic
4: Like matching is enabled.
5: Net swapping is enabled.
6: Using terminal names as correspondence points.
7: Compiling Diva LVS rules...
8:
9:     Net-list summary for /gaia/class/student/komacd/CadDemo/LVS/layout/netlist
10:         count
11:         64          nets
12:         3           terminals
13:         31          pmos
14:         31          nmos
15:
16:     Net-list summary for /gaia/class/student/komacd/CadDemo/LVS/schematic/netlist
17:         count
18:         33          nets
19:         3           terminals
20:         31          pmos
21:         31          nmos
22:
23:
24:     Terminal correspondence points
25:     N61      N31      GND
26:     N63      N32      Vdd
27:     N62      N30      osc_out
28:
29: Devices in the rules but not in the netlist:
30:     cap nfet pfet nmos4 pmos4
31:
32:     Ill-defined correspondence points.
33:
34:     N62 N30  Accepted because one is a subset of the other
35:     N62 N30  Accepted because one is a subset of the other
36:
37:
38:     Device summary for layout
39:             bad  total
40:     nmos      1    31
41:
42:
43:     Device summary for schematic
44:             bad  total
45:     nmos      1    31
46:
47: 60 net-list ambiguities were resolved by random selection.
48:
49: The net-lists failed to match.
50:
51:             layout  schematic

```

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52:                                     instances
53:      un-matched                      1      1
54:      rewired                        30      0
55:      size errors                     0      0
56:      pruned                         0      0
57:      active                         62     62
58:      total                          62     62
59:
60:                                     nets
61:      un-matched                      32     16
62:      merged                         15      0
63:      pruned                         0      0
64:      active                         64     33
65:      total                          64     33
66:
67:                                     terminals
68:      un-matched                      1      1
69:      matched but
70:      different type                  0      0
71:      total                          3      3
72:
73:
74: Probe files from /gaia/class/student/komacd/CadDemo/LVS/schematic
75:
76: devbad.out:
77: I /I0<1>/N0
78: ? Device does not cross-match.
79:
80: netbad.out:
81: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
82: To see the complete information please see the file:
83: /gaia/class/student/komacd/CadDemo/LVS/schematic/netbad.out
84:
85: mergenet.out:
86:
87: termbad.out:
88: T -1  osc_out /osc_out
89: ? Terminal osc_out in the schematic failed to match any terminal in the layout.
90:
91: prunenet.out:
92:
93: prunedev.out:
94:
95: audit.out:
96:
97:
98: Probe files from /gaia/class/student/komacd/CadDemo/LVS/layout
99:
100: devbad.out:
101: I /+29
102: ? Device does not cross-match.
103:

```

\\gaia\Komacd\CadDemo\LVS\si.out

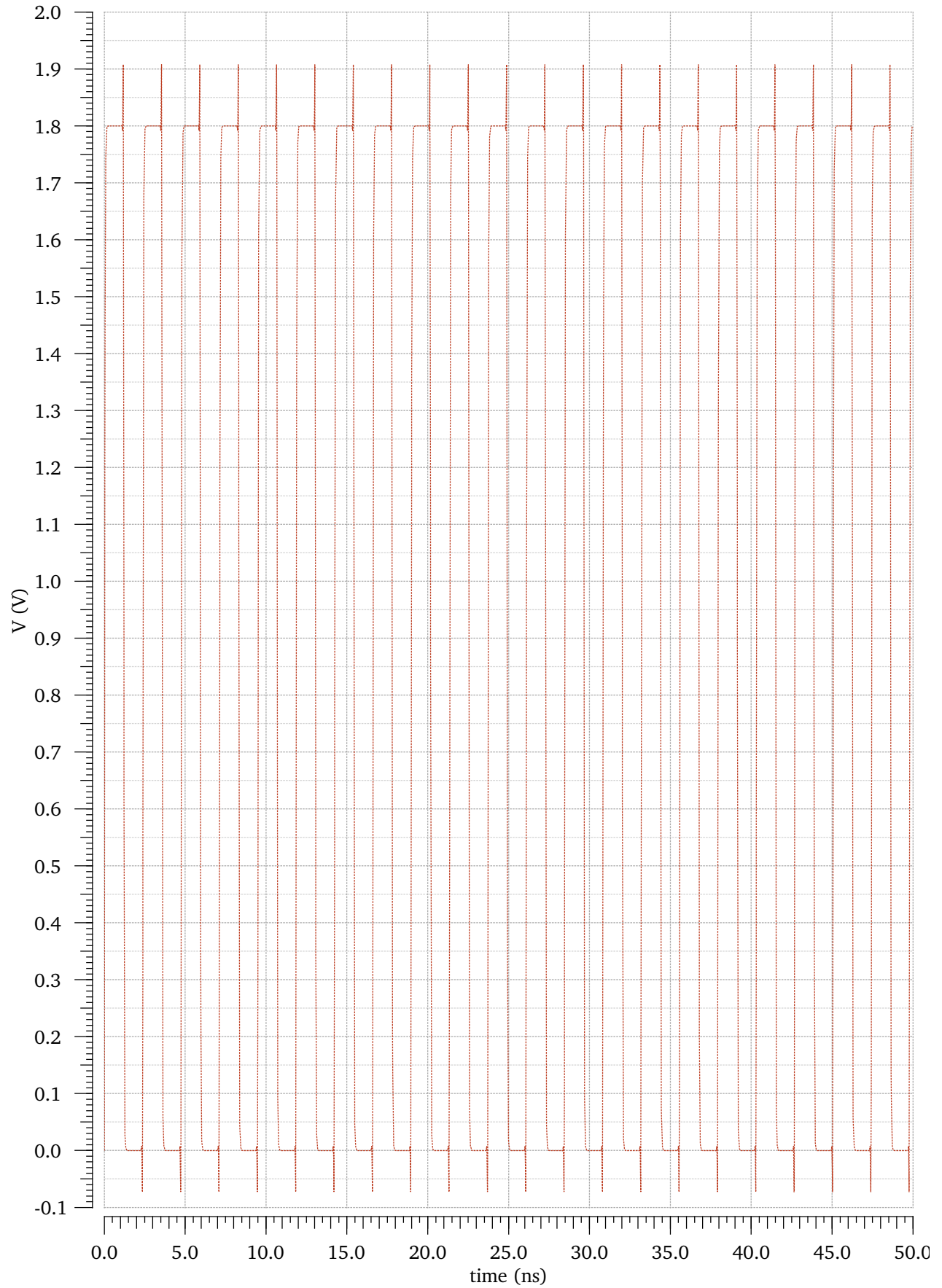
104: netbad.out:
105: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
106: To see the complete information please see the file:
107: /gaia/class/student/komacd/CadDemo/LVS/layout/netbad.out
108:
109: mergenet.out:
110: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
111: To see the complete information please see the file:
112: /gaia/class/student/komacd/CadDemo/LVS/layout/mergenet.out
113:
114: termbad.out:
115: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFile.
116: To see the complete information please see the file:
117: /gaia/class/student/komacd/CadDemo/LVS/layout/termbad.out
118:
119: prunenet.out:
120:
121: prunedev.out:
122:
123: audit.out:
124:

Post Layout-Simulation (Ring Oscillator):

Transient Response**Thu Apr 2 15:28:29 2020**

Name Vis

/osc_out



Conclusion:

S. No.	Description	Rise Time(us)	Fall Time(us)	Delay Time(us)
1.	Ring Oscillator	0.006us	0.005us	0us