TFH-Berlin

Mikrocomputer-Technik

MCT 49

Teil4: Parallel-I/O-Baustein 82C55A

Studiengang Technische Informatik (BA)
Prof. Dr.-Ing. Alfred Rożek

82C55A
Blockdiagramm

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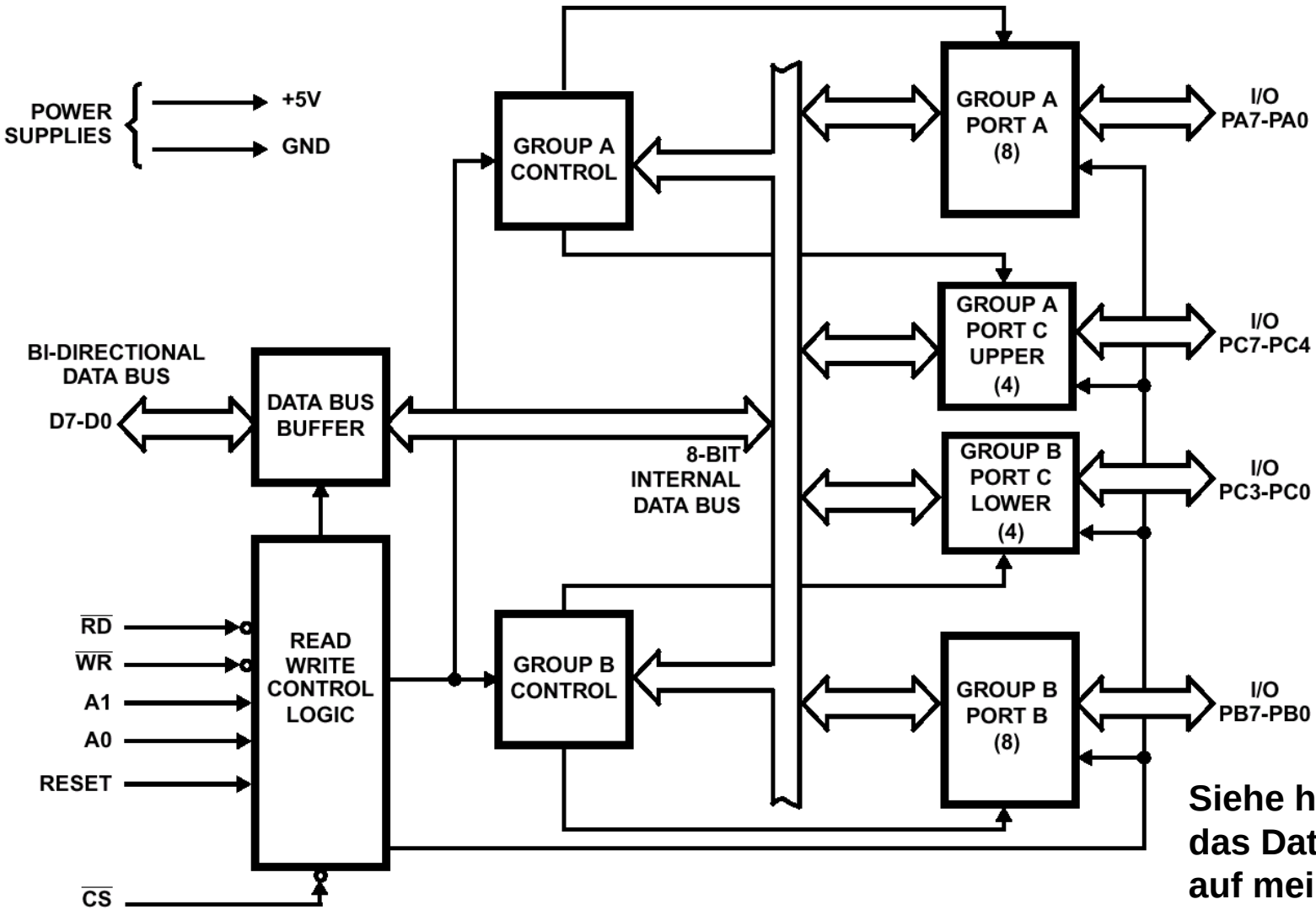

Siehe hierzu auch das Datenblatt zum 82C55A auf meiner Homepage

82C55A
Pinouts

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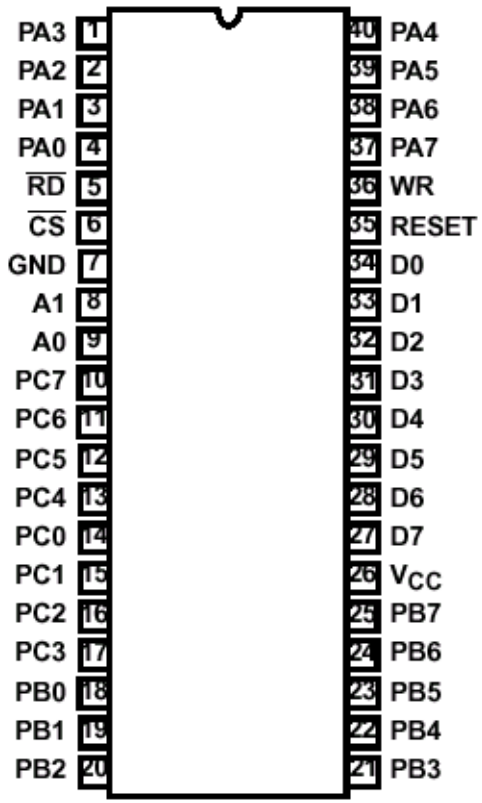
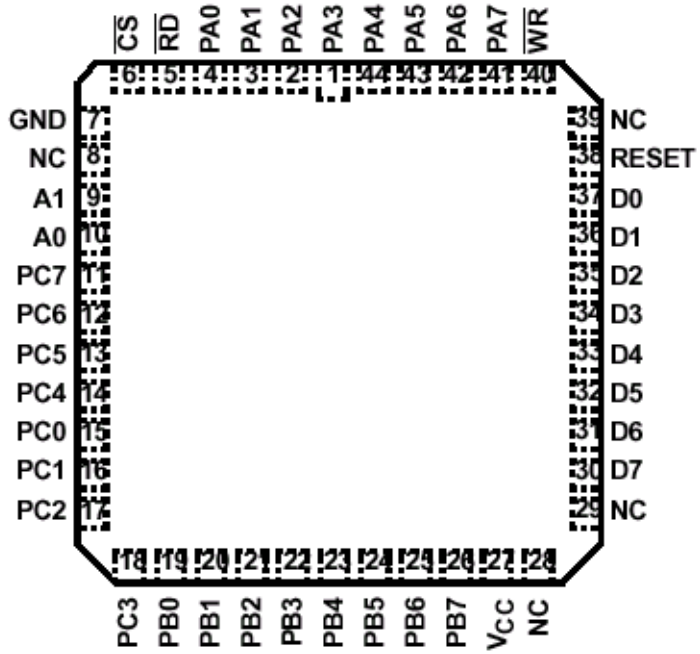
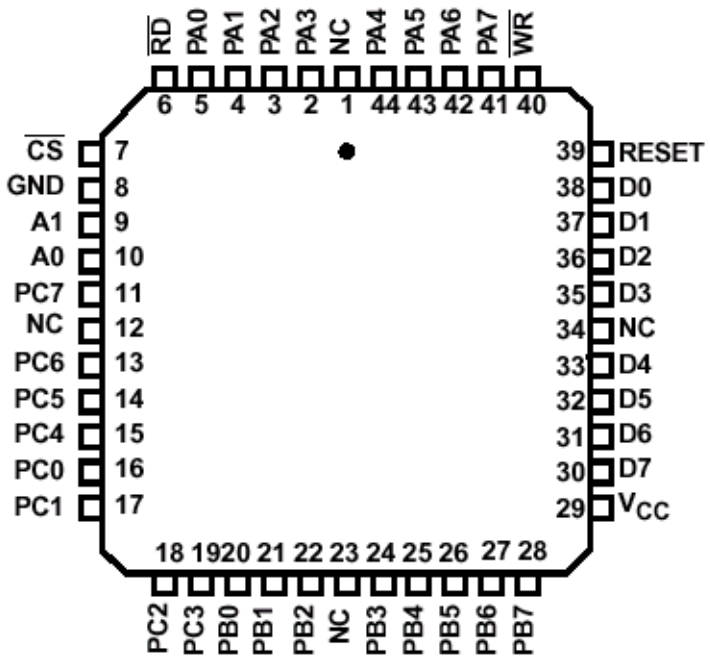
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW



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A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

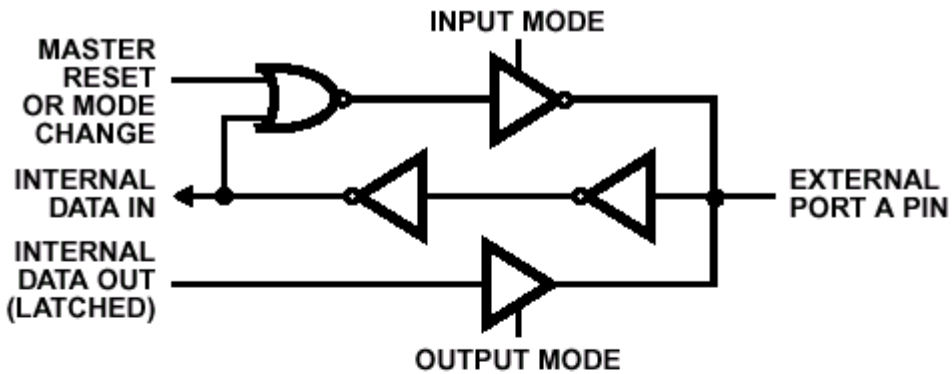

FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

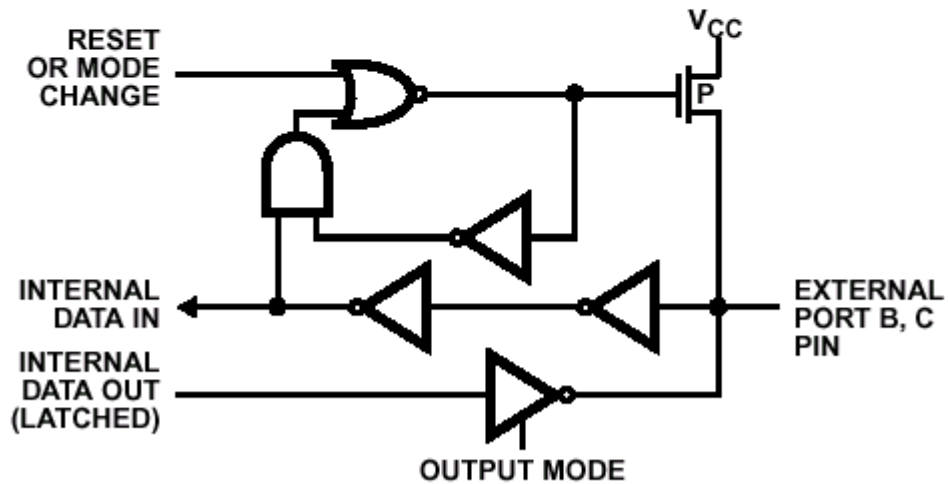

FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

82C55A
Mode-Definitionen

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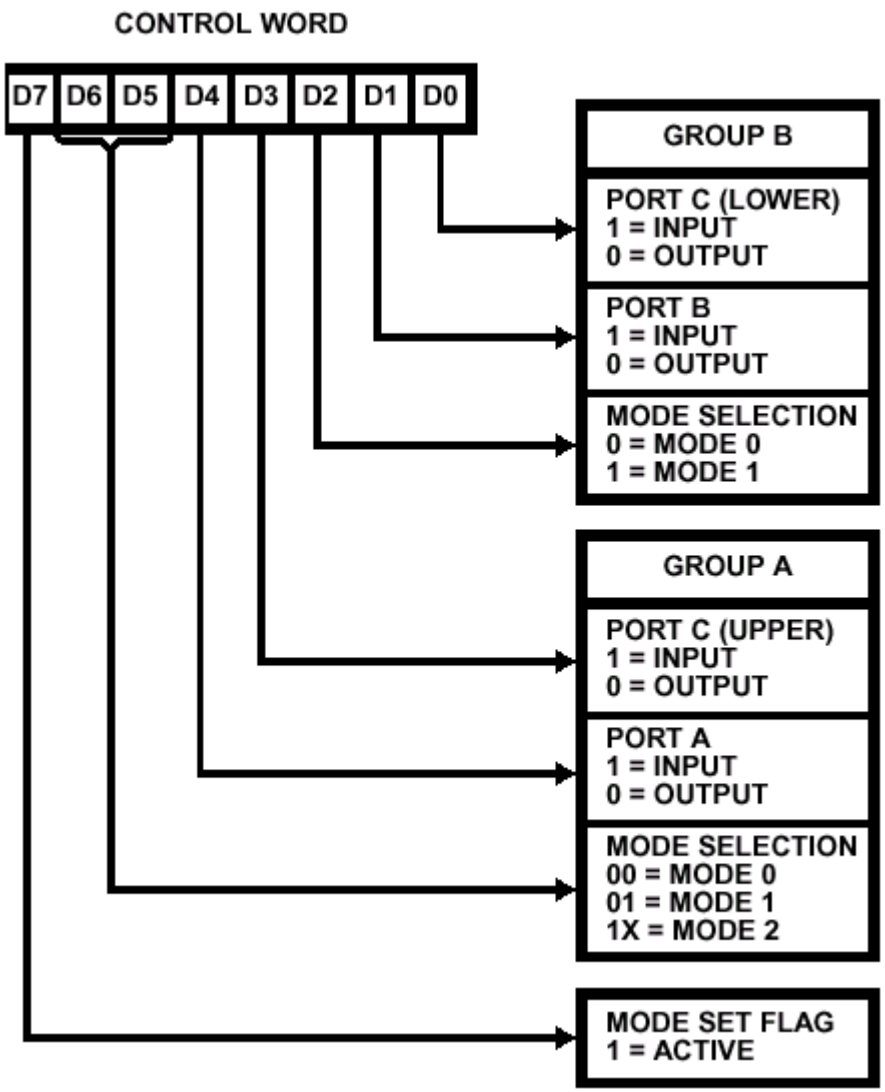
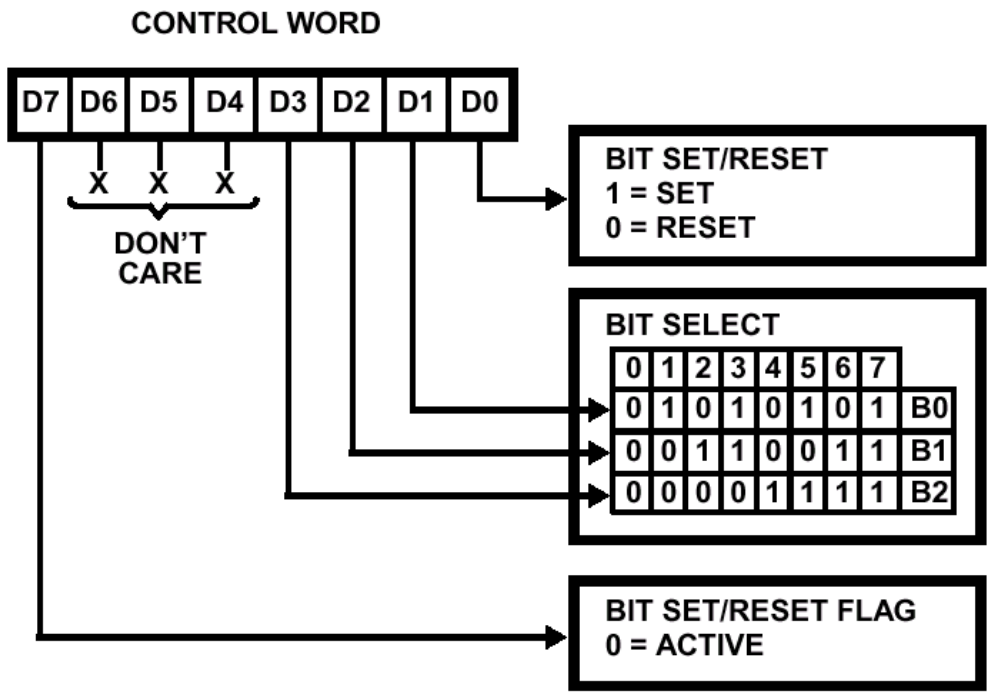


Mode-Format Definition



Bit Set/Reset Format

82C55A
Mode 0 Port Definition

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A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

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Mode 0: Basic Input und Basic Output

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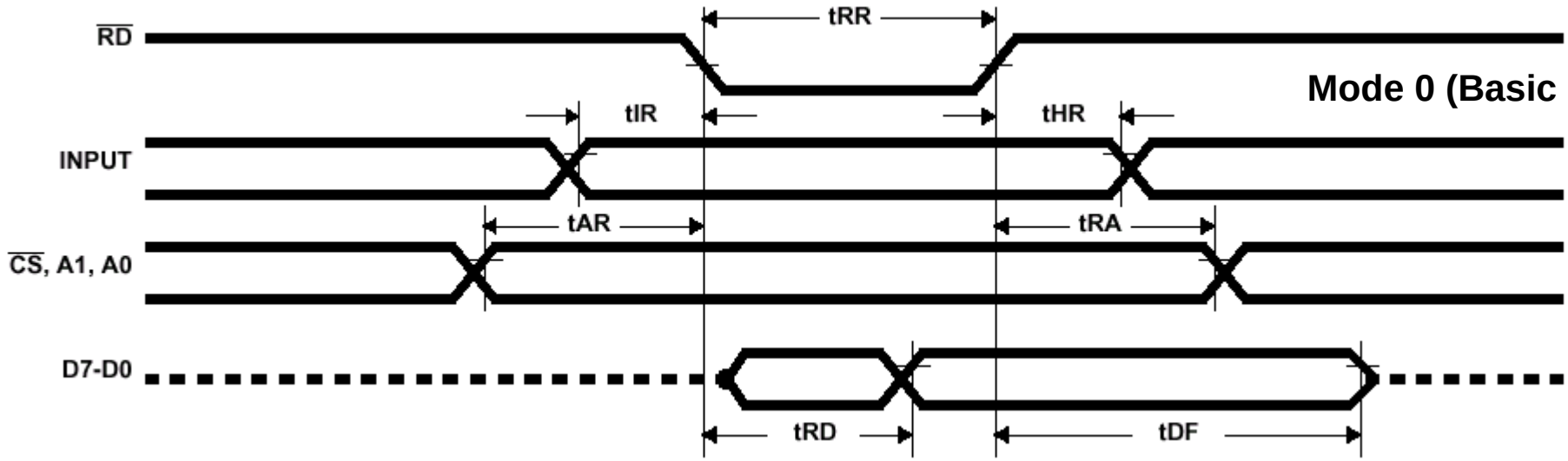

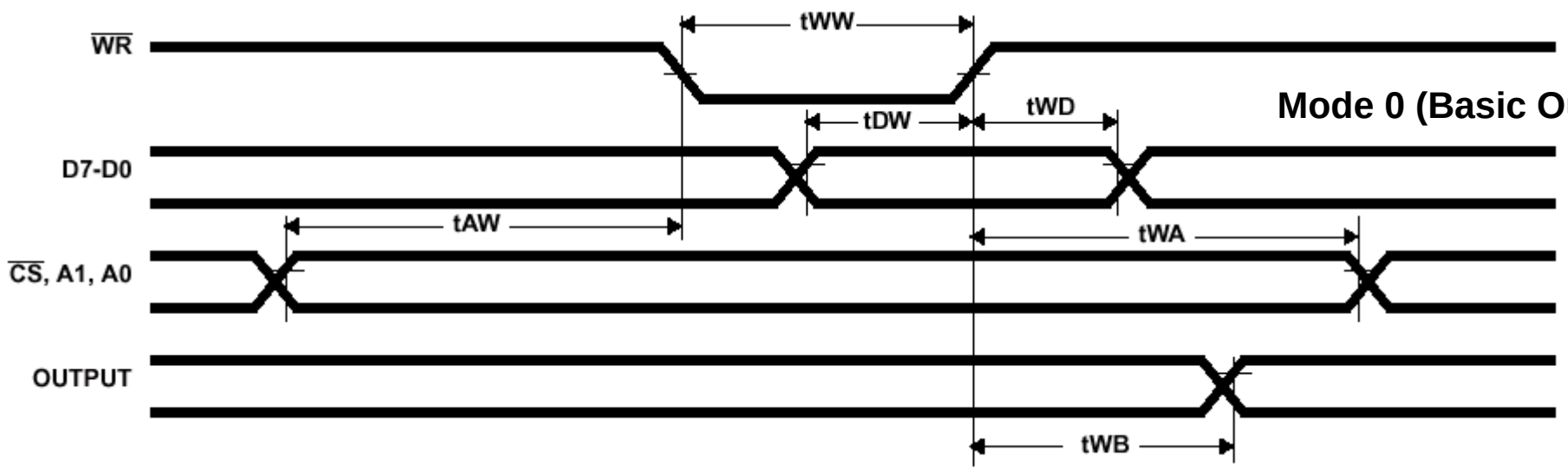

82C55A
Mode 0: Konfigurationen$_1$

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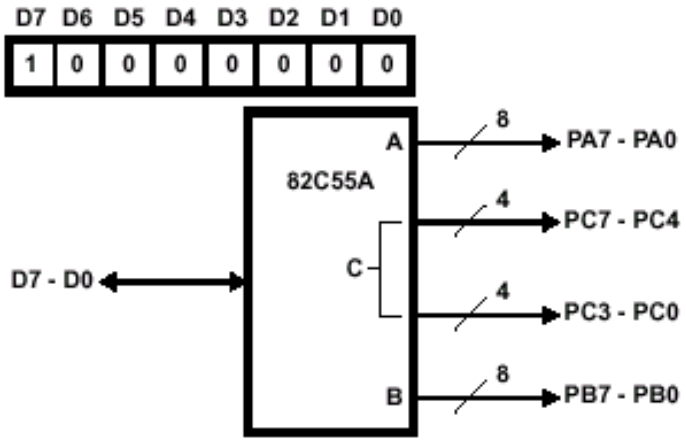
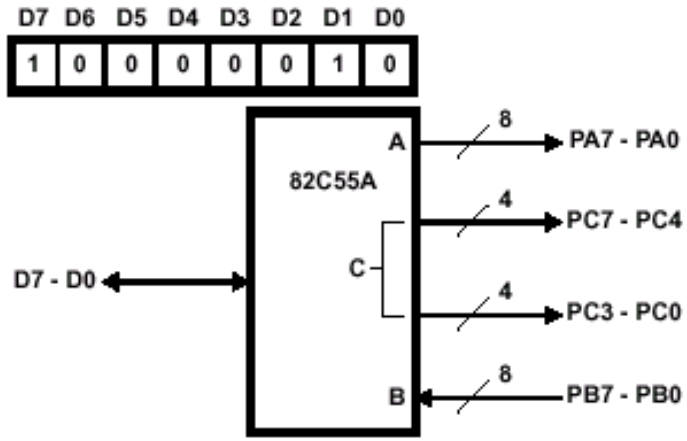
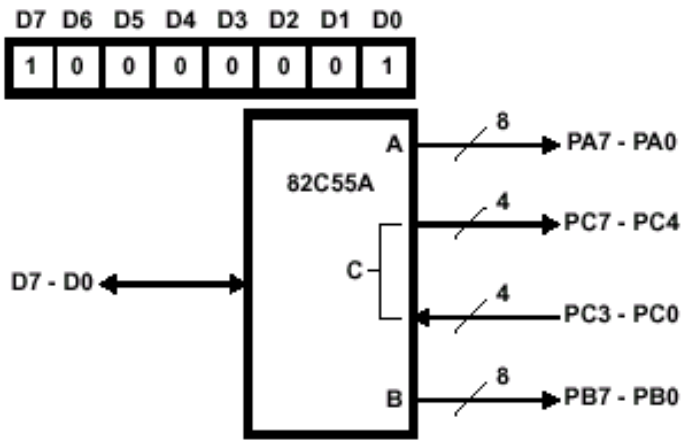
CONTROL WORD #0



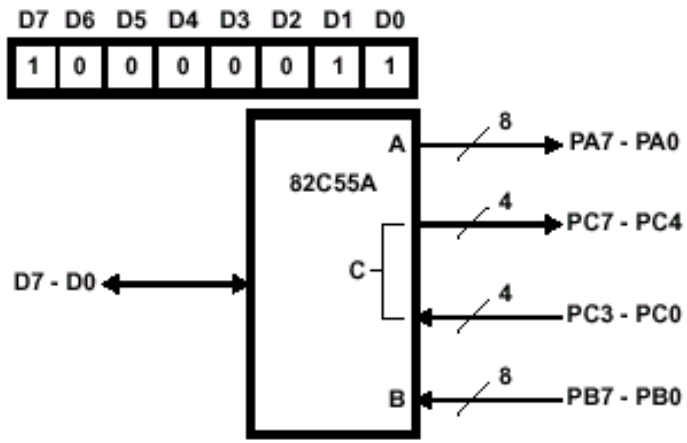
CONTROL WORD #2



CONTROL WORD #1



CONTROL WORD #3



82C55A
Mode 0: Konfigurationen$_2$

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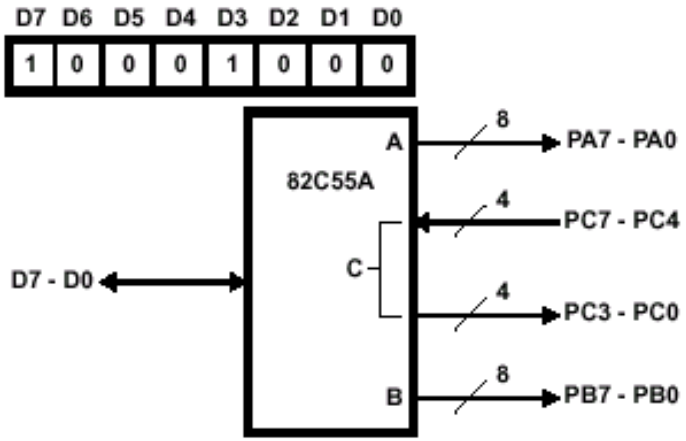
CONTROL WORD #4



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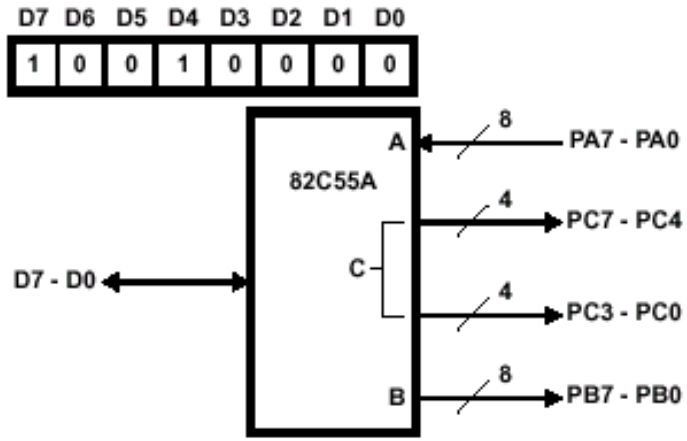

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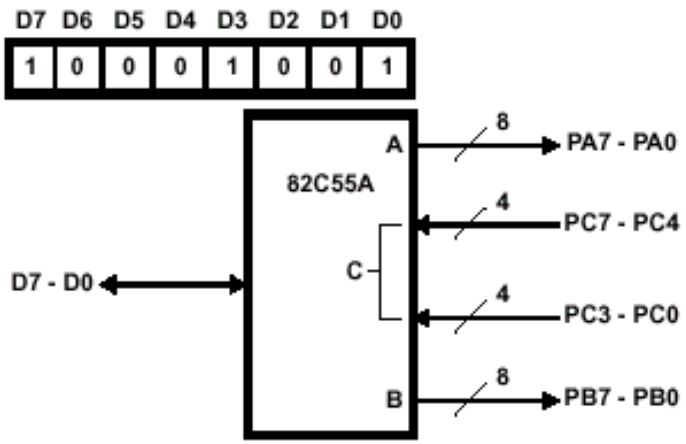

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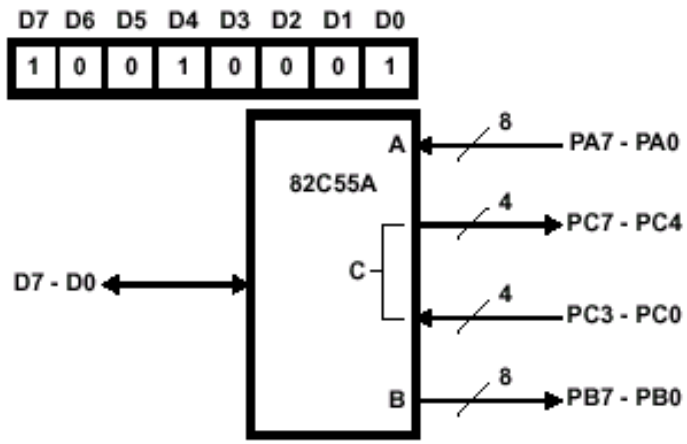

82C55A
Mode 0: Konfigurationen$_3$

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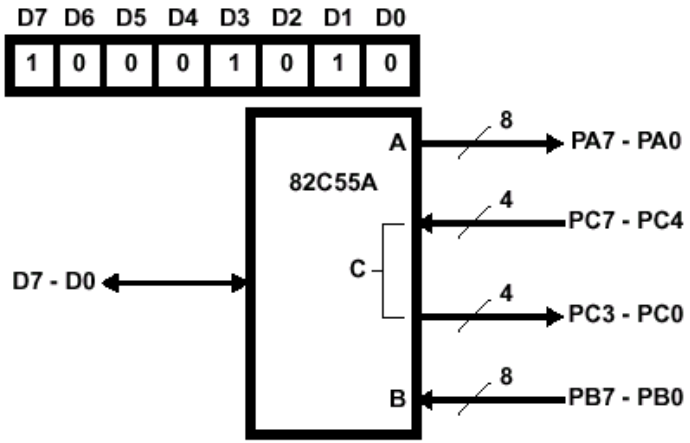
CONTROL WORD #6



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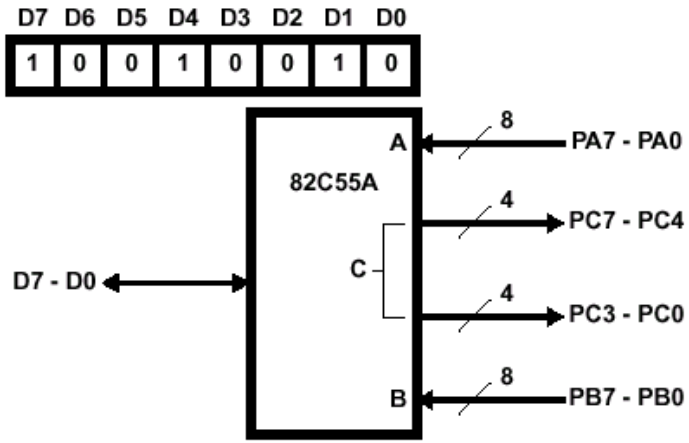
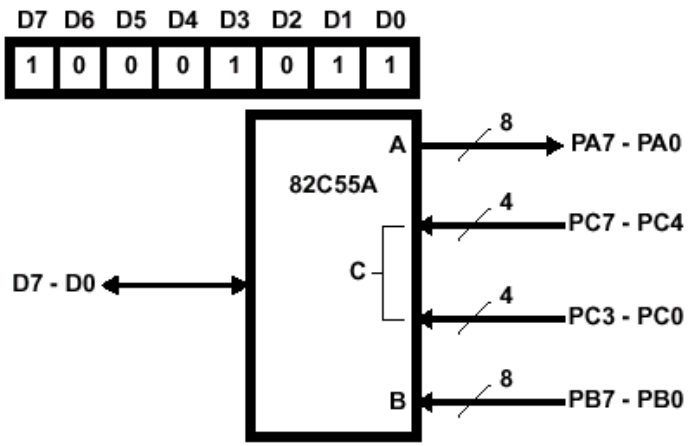
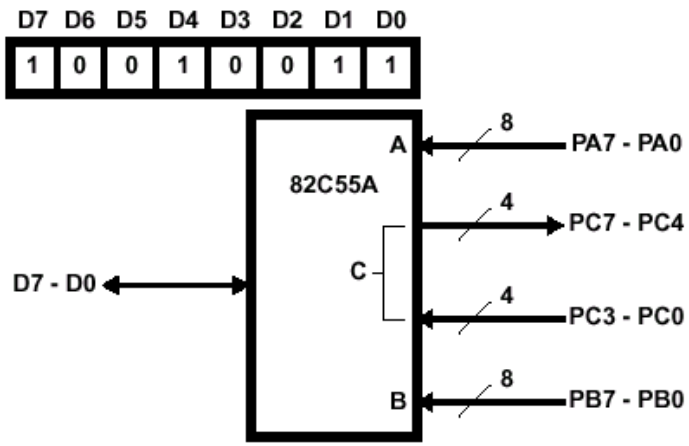


CONTROL WORD #7



CONTROL WORD #11



82C55A
Mode 0: Konfigurationen$_4$

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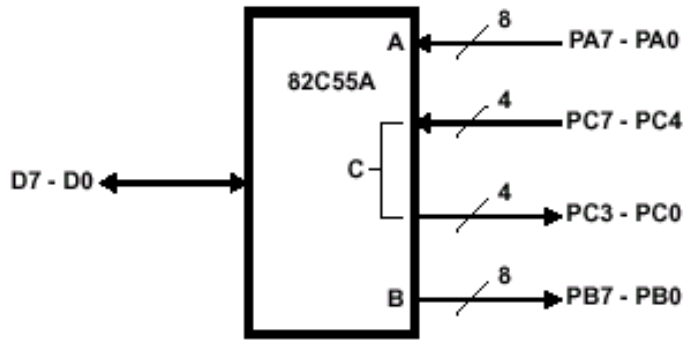
CONTROL WORD #12

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	0



CONTROL WORD #14

D7	D6	D5	D4	D3	D2	D1	D0
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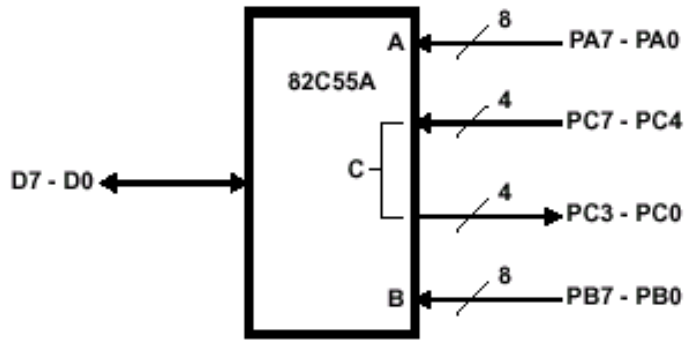
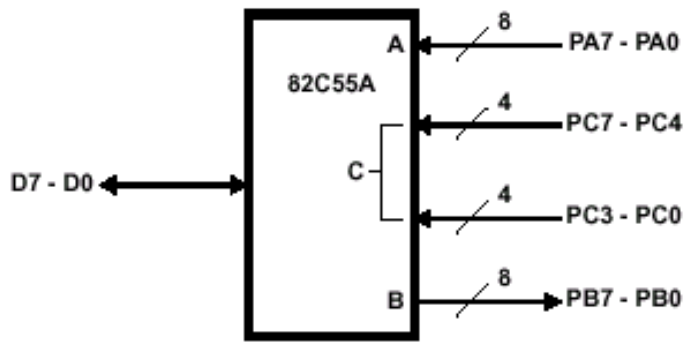


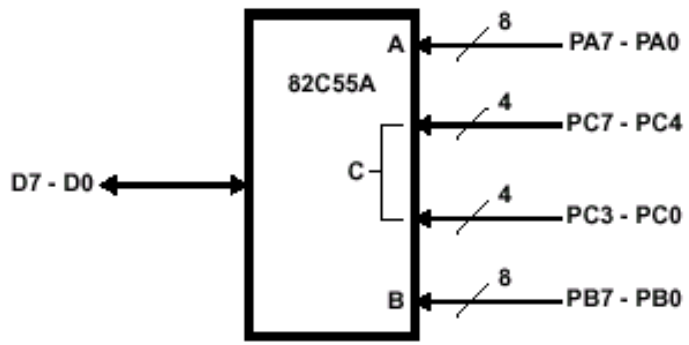
CONTROL WORD #13

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1

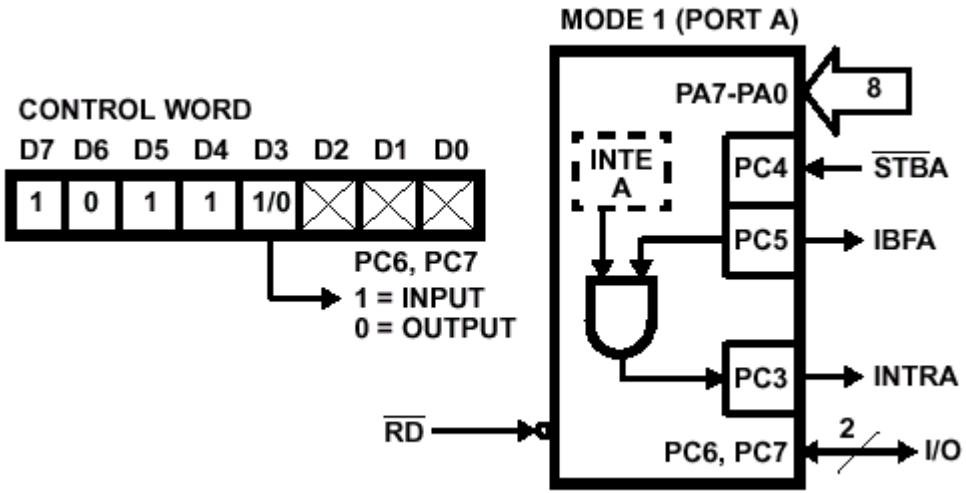


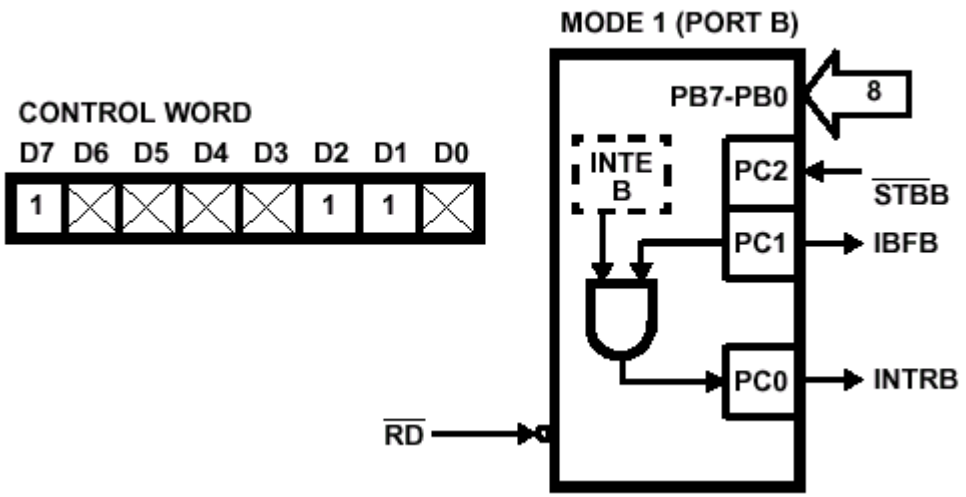
CONTROL WORD #15

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	1	1



Mode 1: Operating Modes$_1$





Input

Mode 1: Operating Modes$_2$

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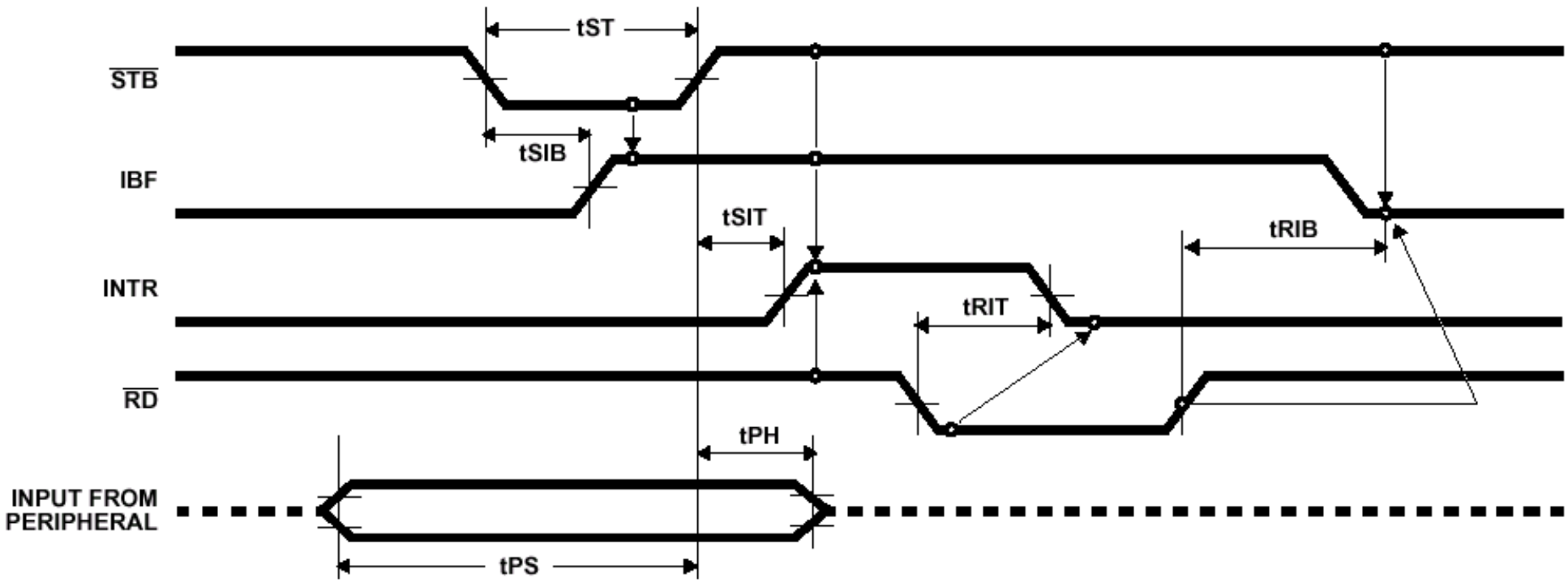
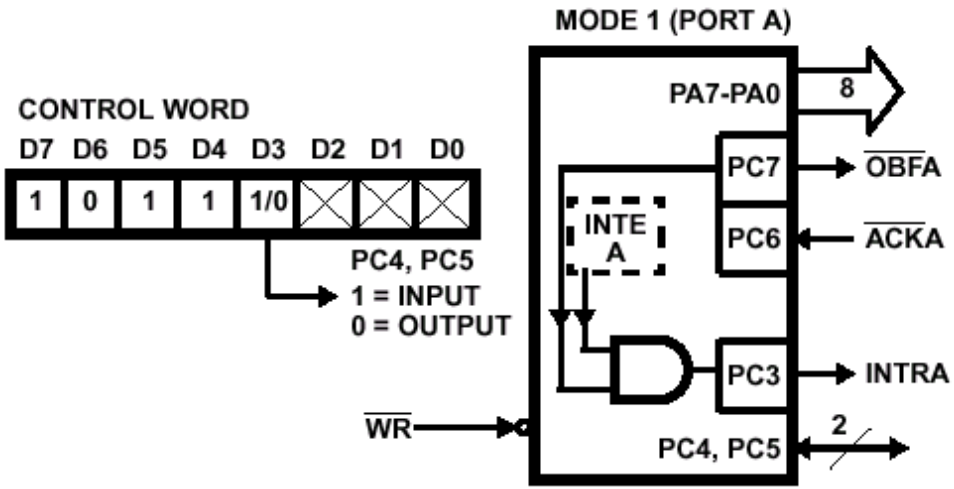
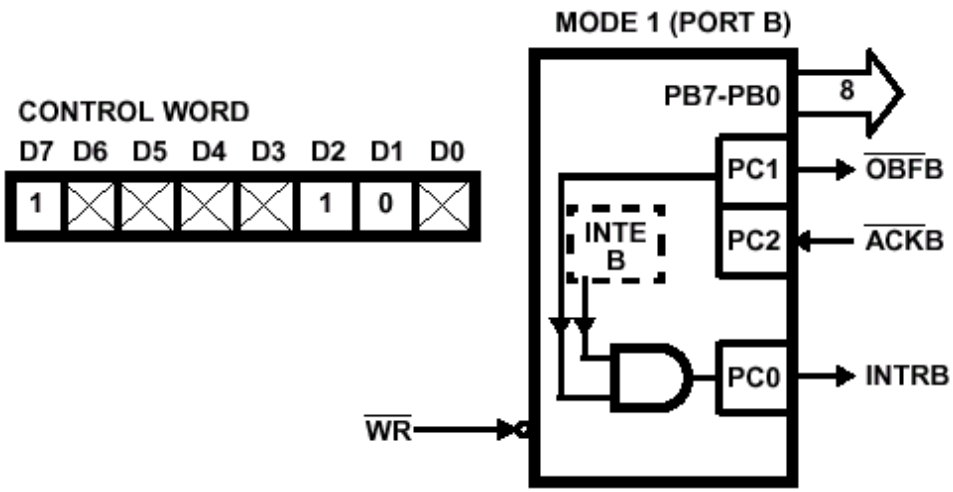


Mode 1: Operating Modes$_3$

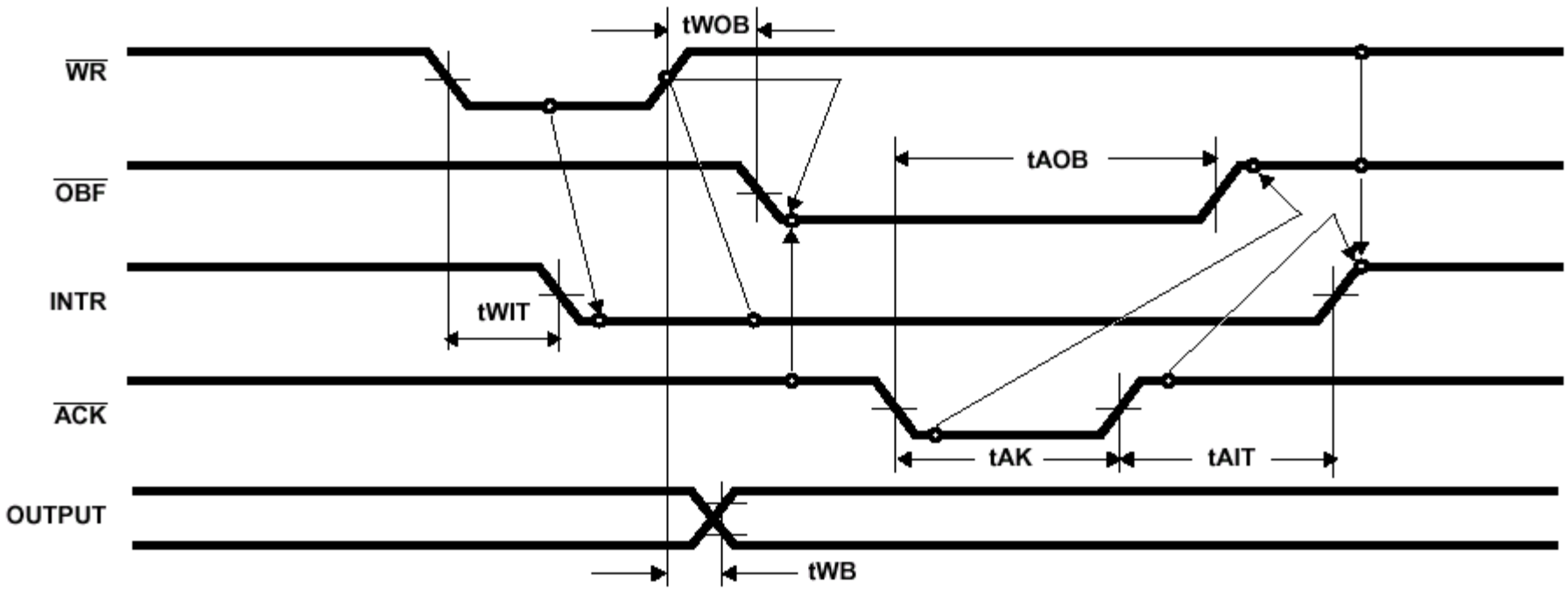




Output

Mode 1: Operating Modes$_4$

TFH-Berlin



Strobed Output

Mode 1: Operating Modes$_5$

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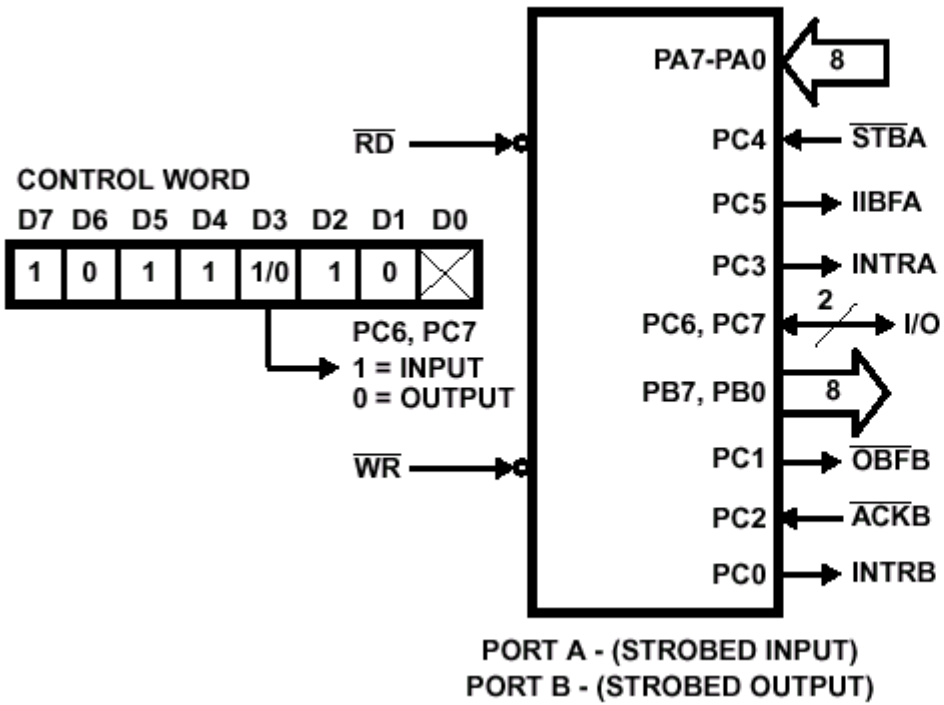
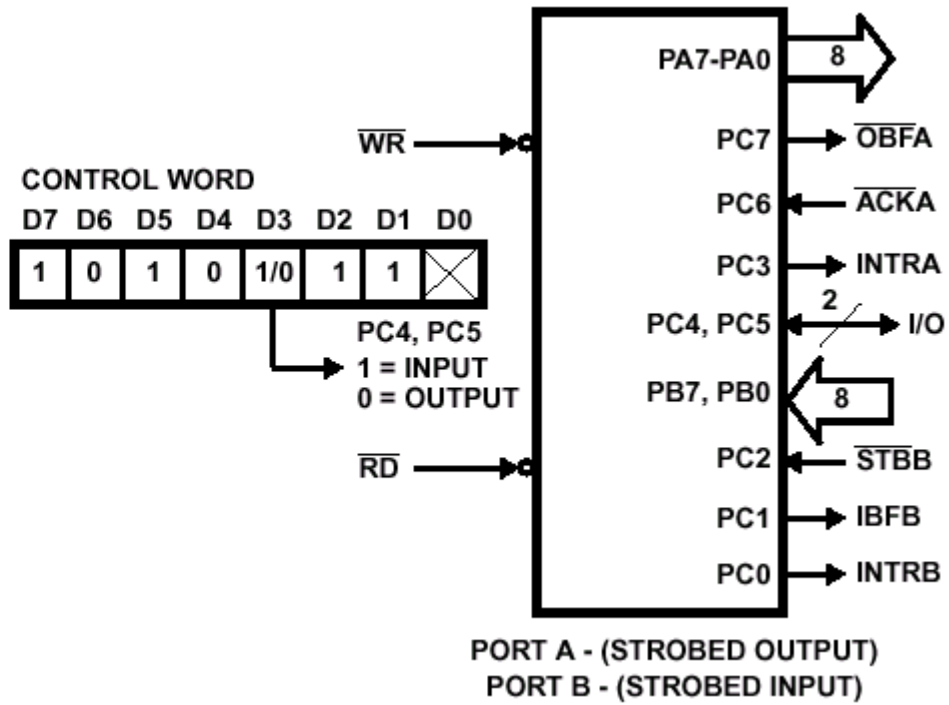
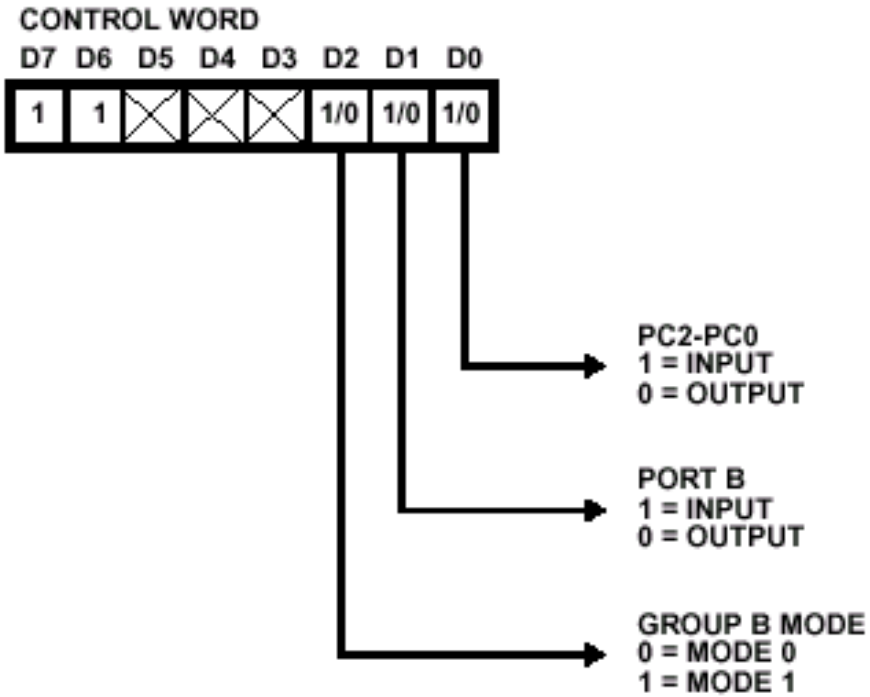
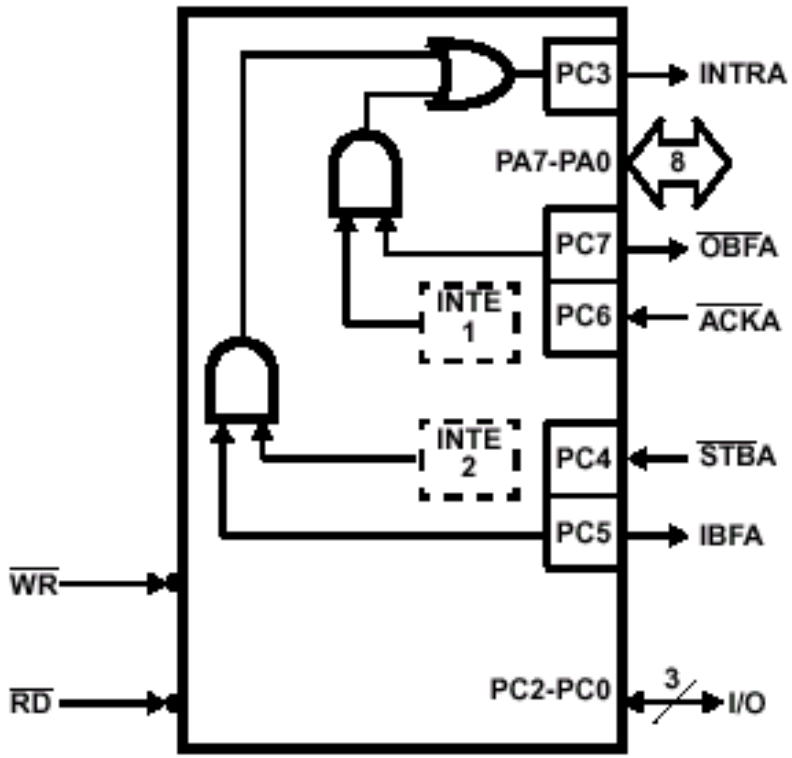




Kombinationen

Mode 2: Operating Modes$_1$





82C55A
Mode 2: Operating Modes$_2$ Bidirektional

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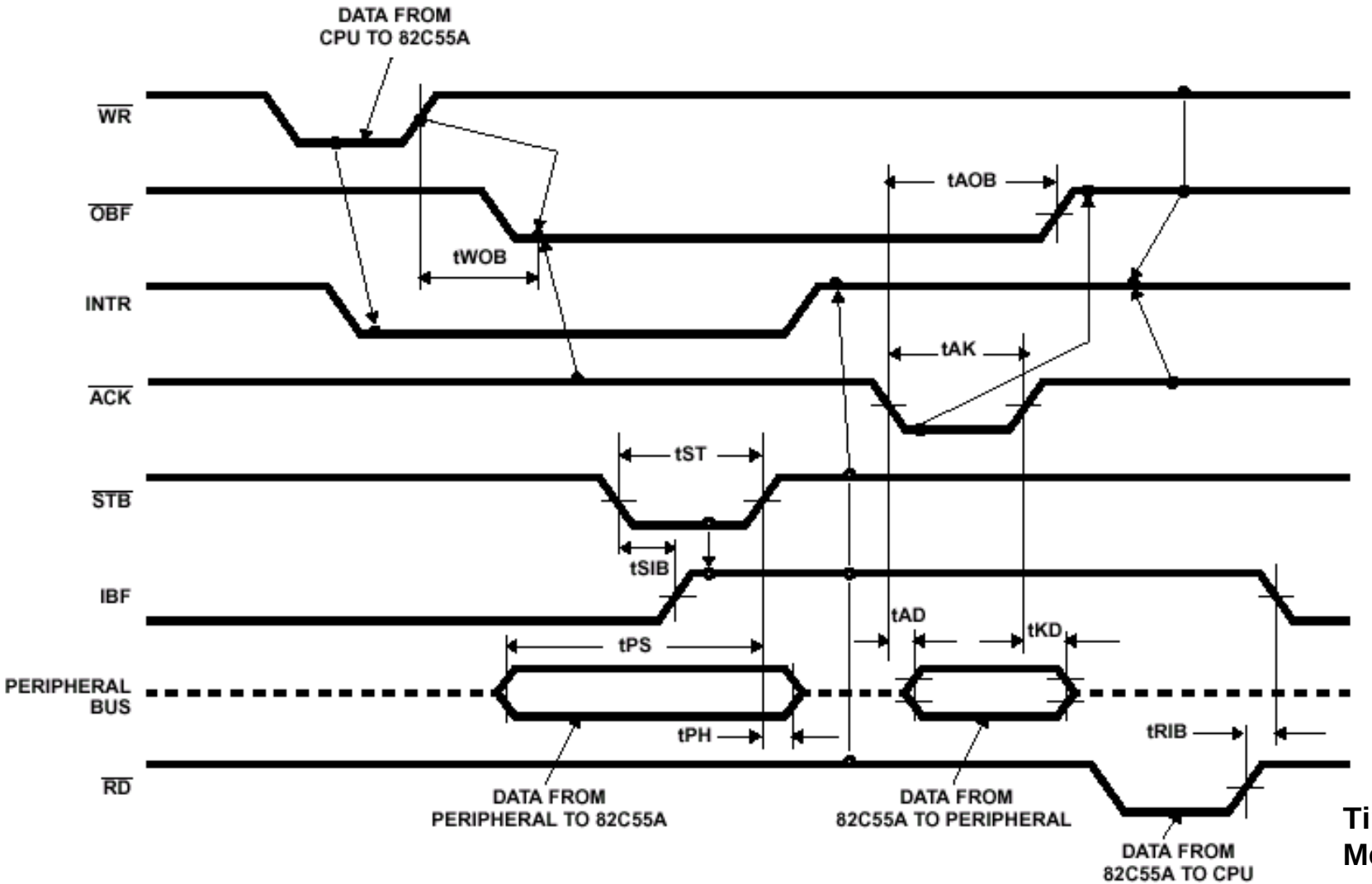

Timing Diagramm Mode 2

82C55A
Mode 2: Operating Modes$_3$

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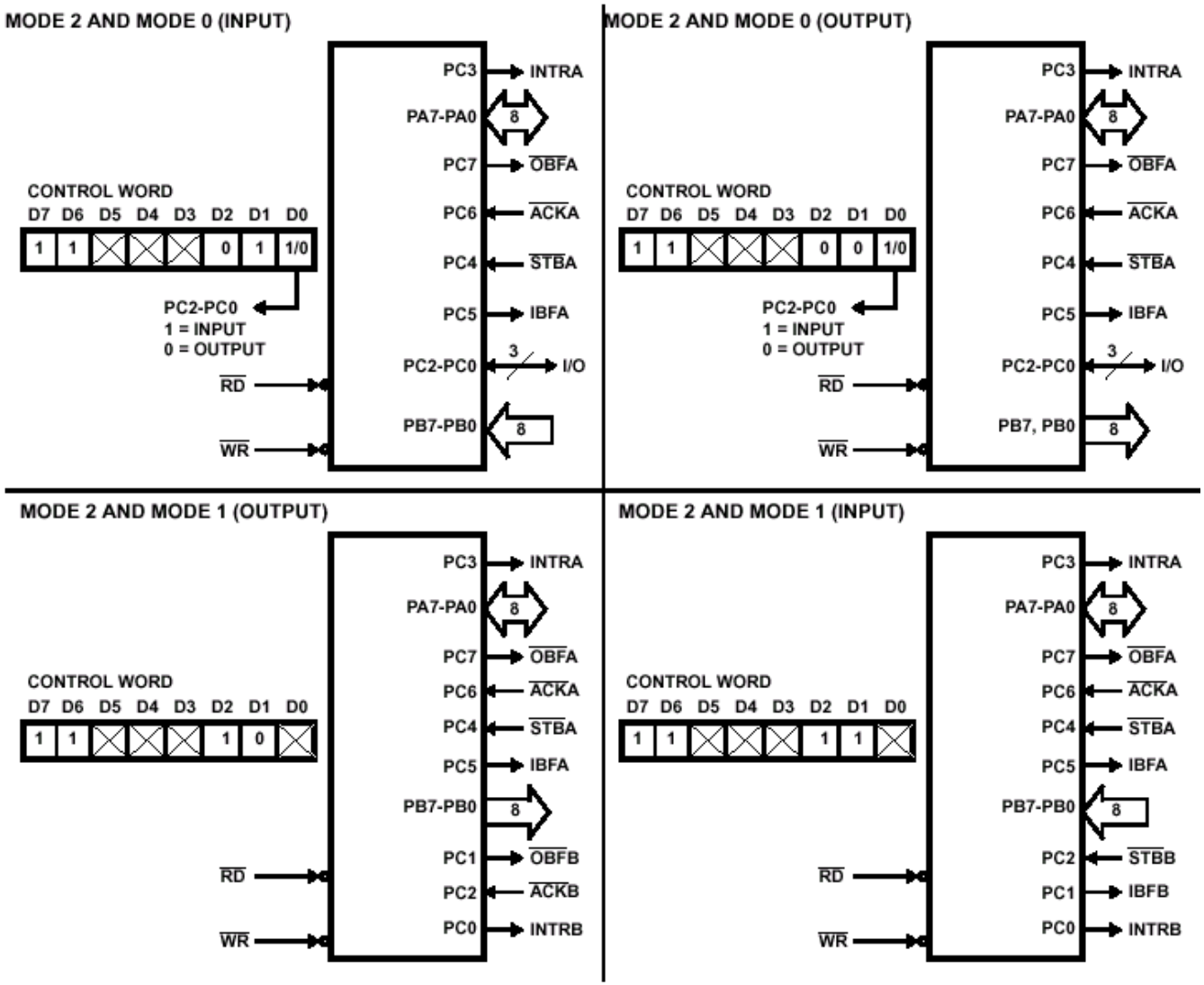

Kombinationen

82C55A
Übersichtstabelle der Betriebsartendefinition

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	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	↔	
PA1	In	Out	In	Out	↔	
PA2	In	Out	In	Out	↔	
PA3	In	Out	In	Out	↔	
PA4	In	Out	In	Out	↔	
PA5	In	Out	In	Out	↔	
PA6	In	Out	In	Out	↔	
PA7	In	Out	In	Out	↔	
PB0	In	Out	In	Out		Mode 0 or Mode 1 Only
PB1	In	Out	In	Out		
PB2	In	Out	In	Out		
PB3	In	Out	In	Out		
PB4	In	Out	In	Out		
PB5	In	Out	In	Out		
PB6	In	Out	In	Out		
PB7	In	Out	In	Out		
PC0	In	Out	INTRB	INTRB	I/O	
PC1	In	Out	IBFB	$\overline{OBF}$B	I/O	
PC2	In	Out	$\overline{STB}$B	$\overline{ACK}$B	I/O	
PC3	In	Out	INTRA	INTRA	INTRA	
PC4	In	Out	$\overline{STB}$A	I/O	$\overline{STB}$A	
PC5	In	Out	IBFA	I/O	IBFA	
PC6	In	Out	I/O	$\overline{ACK}$A	$\overline{ACK}$A	
PC7	In	Out	I/O	$\overline{OBF}$A	$\overline{OBF}$A	

Zusammenfassung: Mode 1 und Mode 2

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INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
		GROUP A			GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTEA	I/O	I/O	INTRA	INTEB	OBFB	INTRB
		GROUP A			GROUP B		

FIGURE 15. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
OBFA	INTE1	IBFA	INTE2	INTRA	X	X	X
		GROUP A			GROUP B		

(Defined by Mode 0 or Mode 1 Selection)

Status Wort Format Mode 2

INTERRUPT ENABLE FLAG	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or $\overline{STB}$B (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

Interrupt Enable Flags in Mode 1 und Mode 2

Beispiel: Interface für die Druckerschnittstelle

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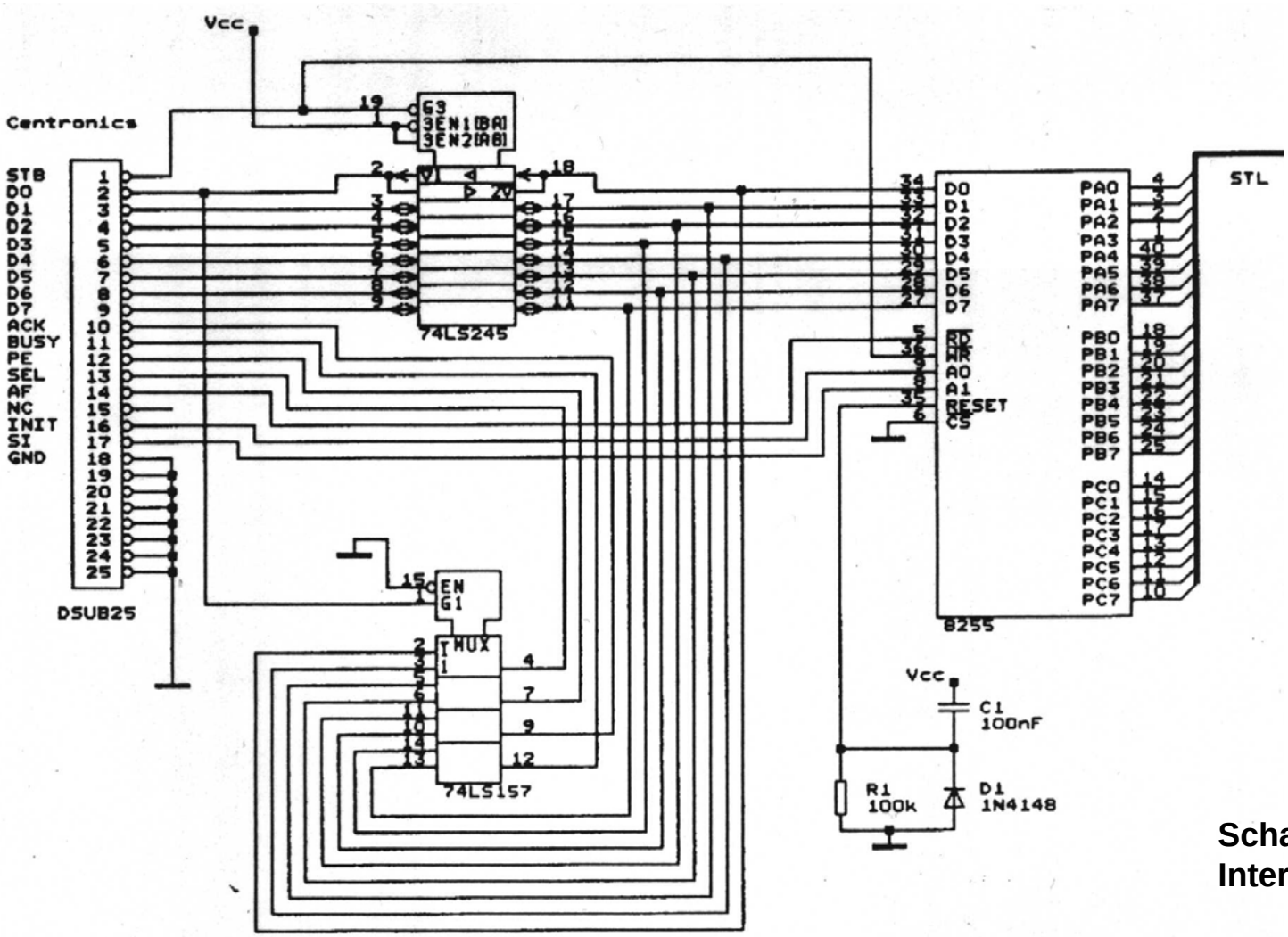

Schaltplan der Interfaceschaltung

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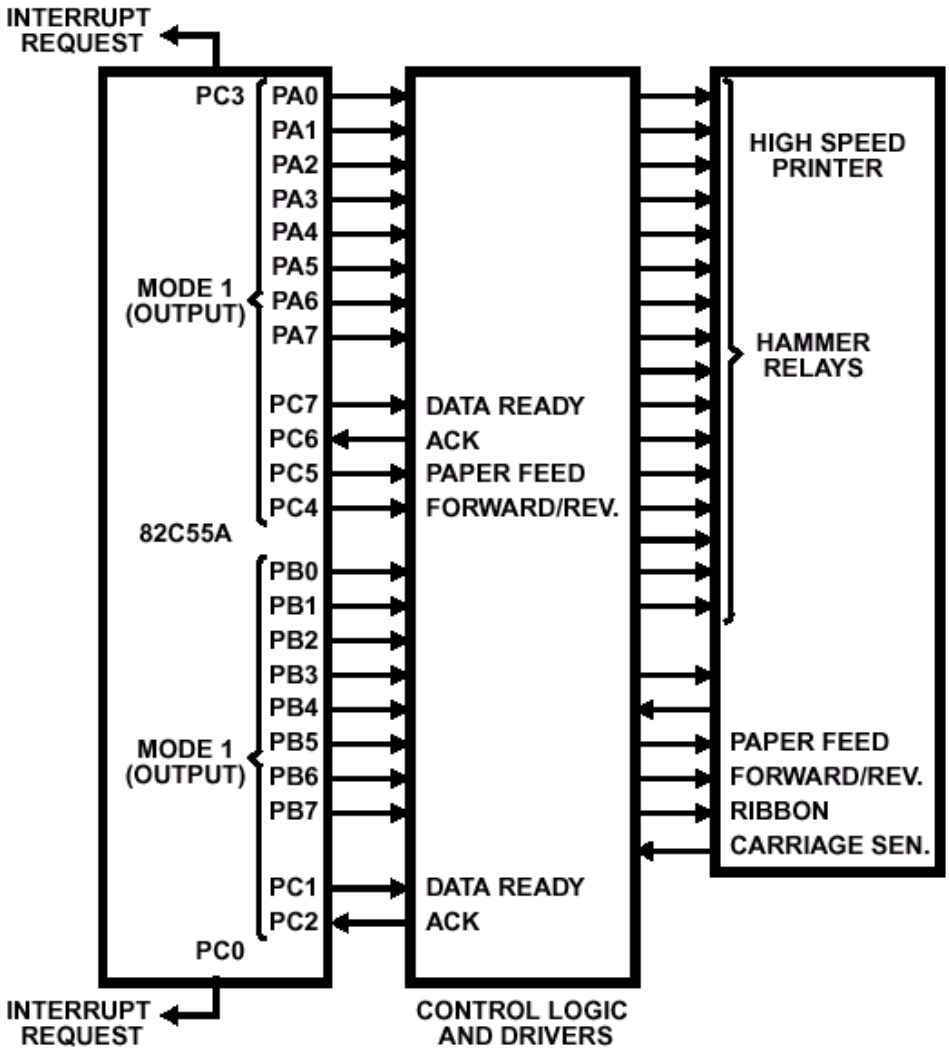
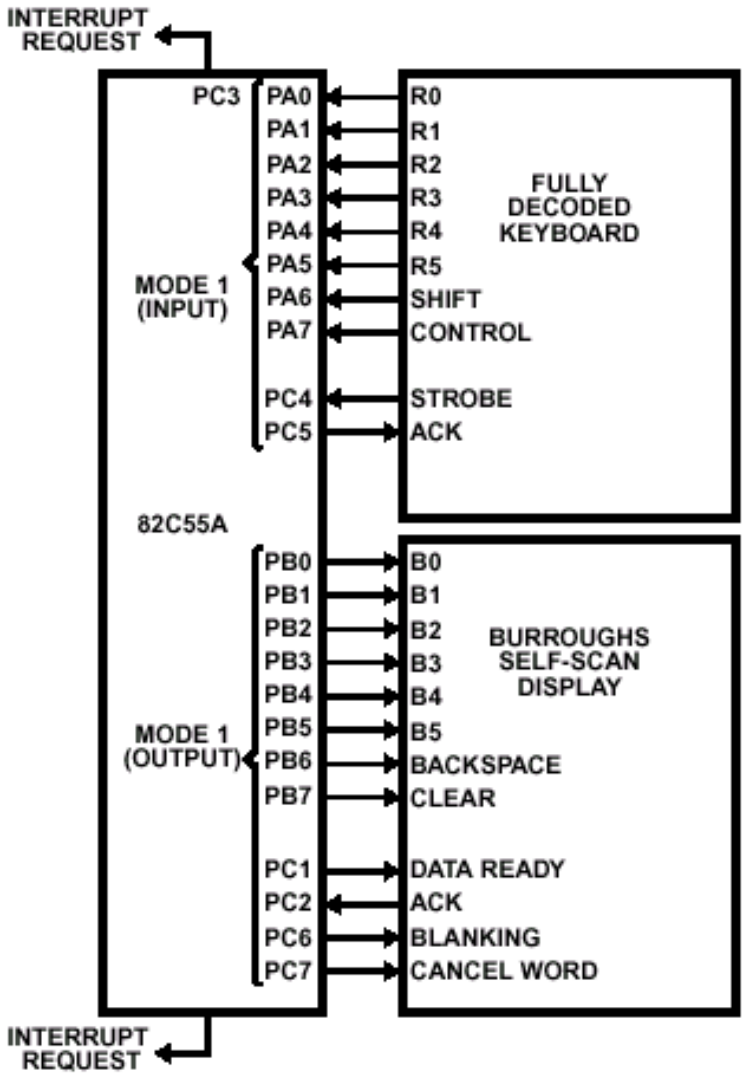
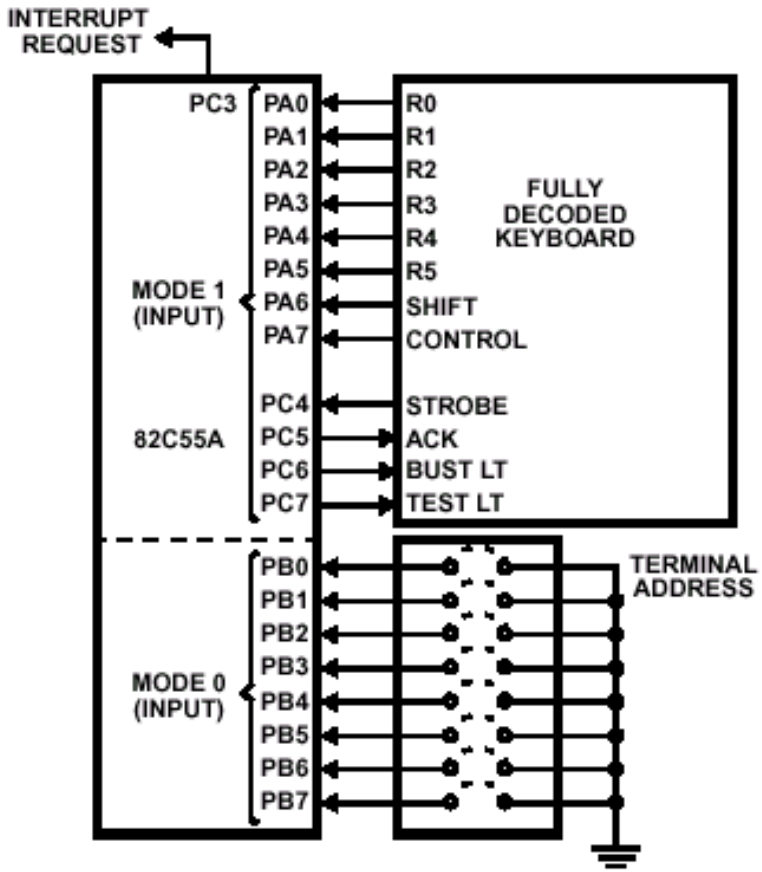


Printer Interface

Keyboard und Display Interface

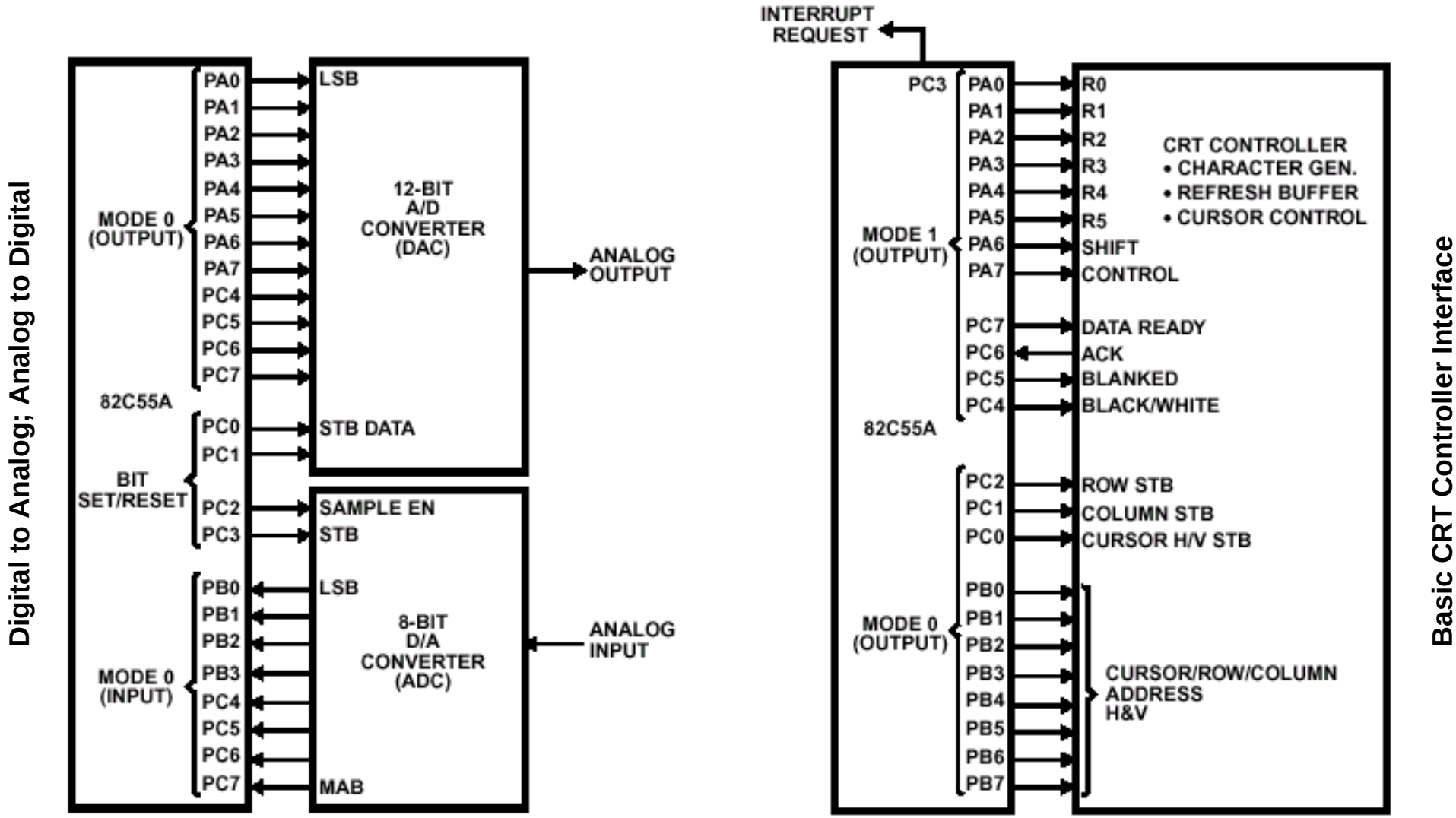




Keyboard und Terminal Adress Interface

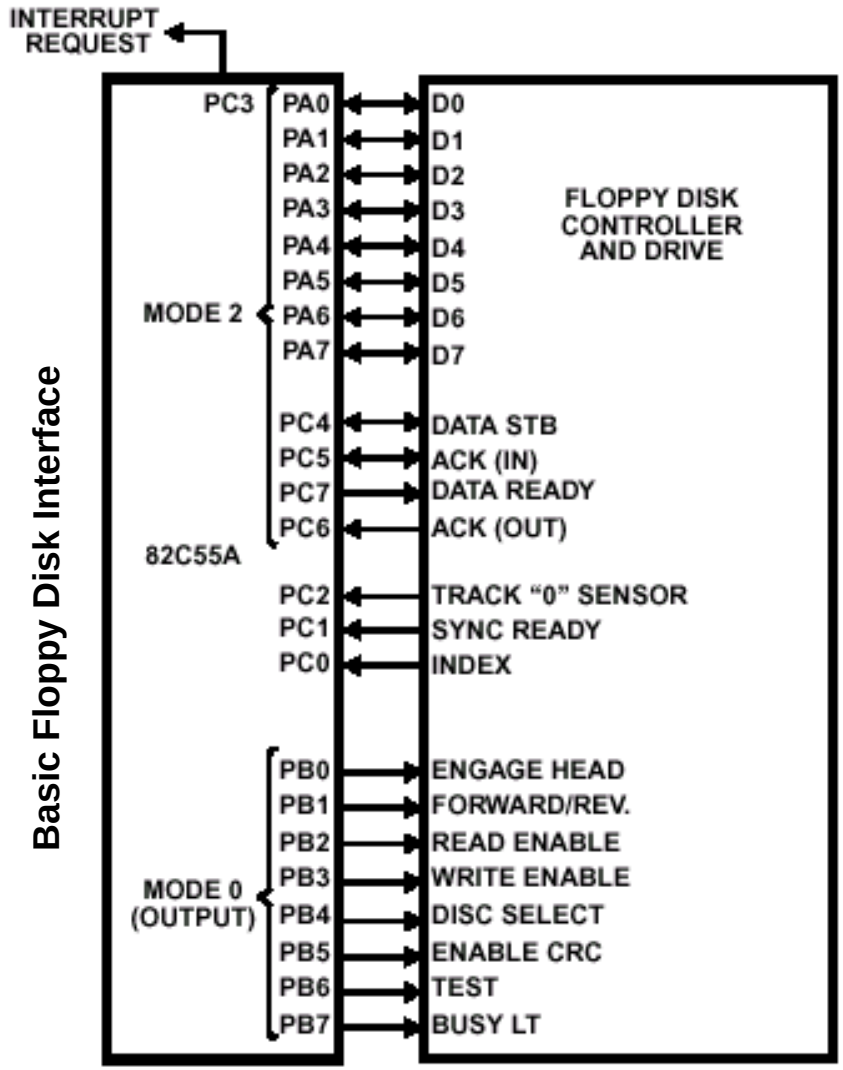
82C55A
Applikationsbeispiele$_3$

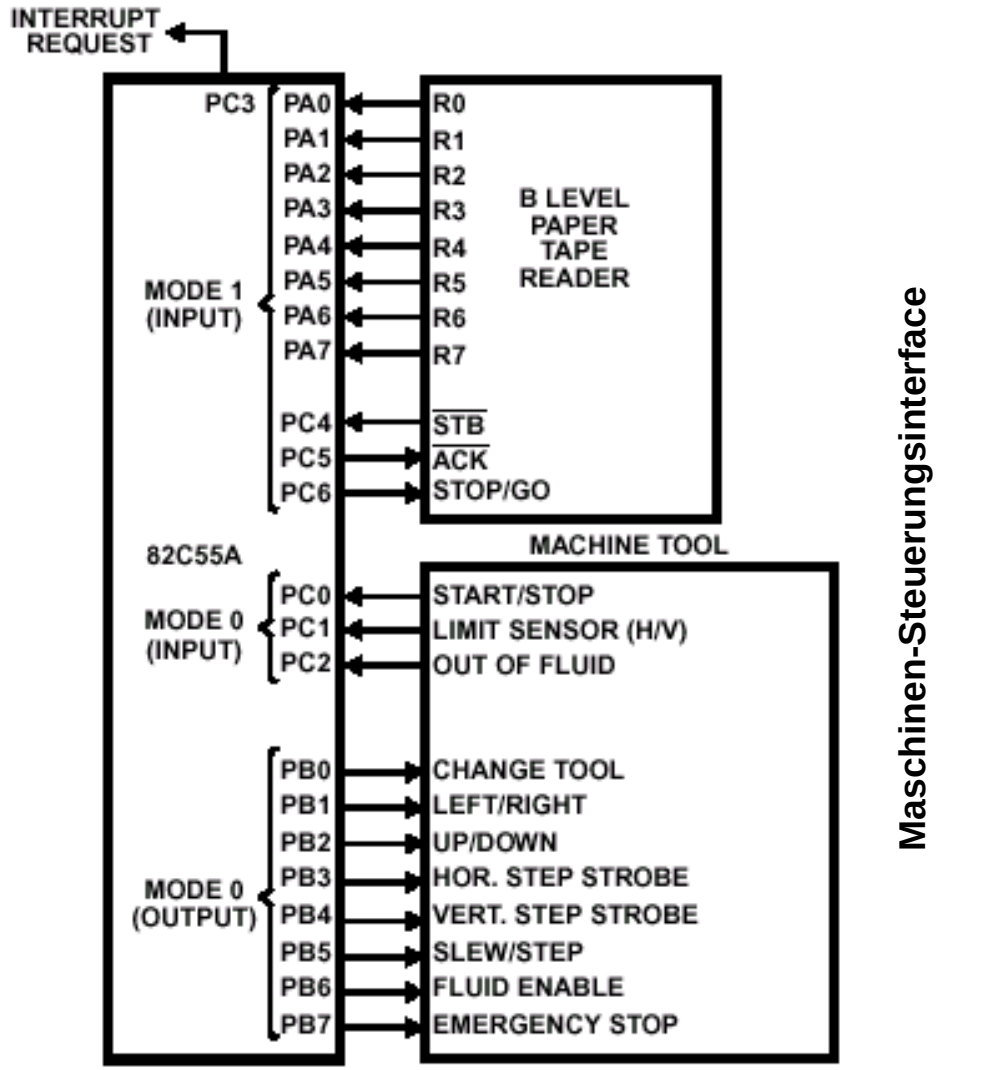
TFH-Berlin



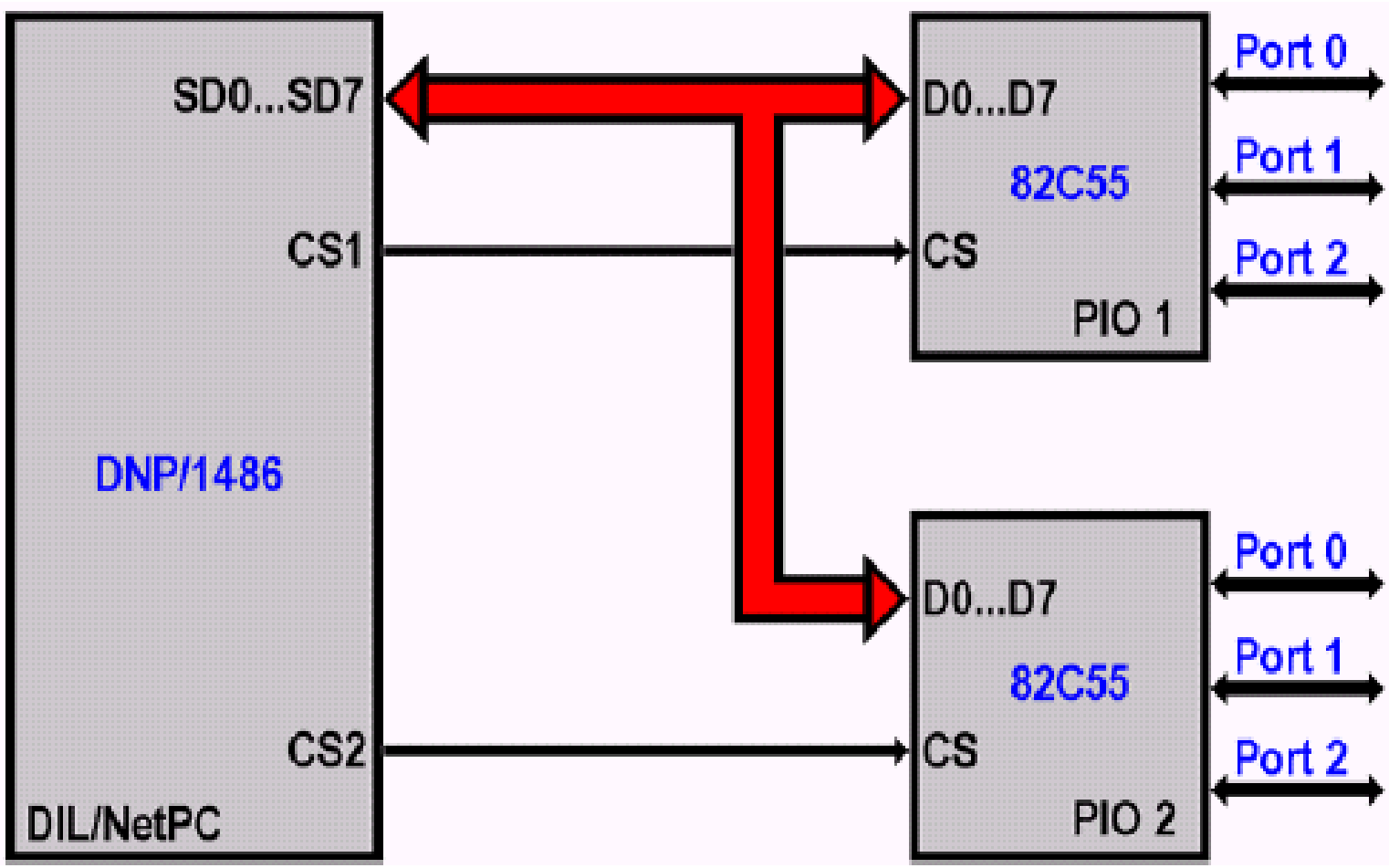
82C55A
Applikationsbeispiele$_4$

TFH-Berlin





TFH-Berlin



Parallel-I/O-Erweiterung für den DIL/NetPC

Anwendungsbeispiel 8255 Betriebsart 0

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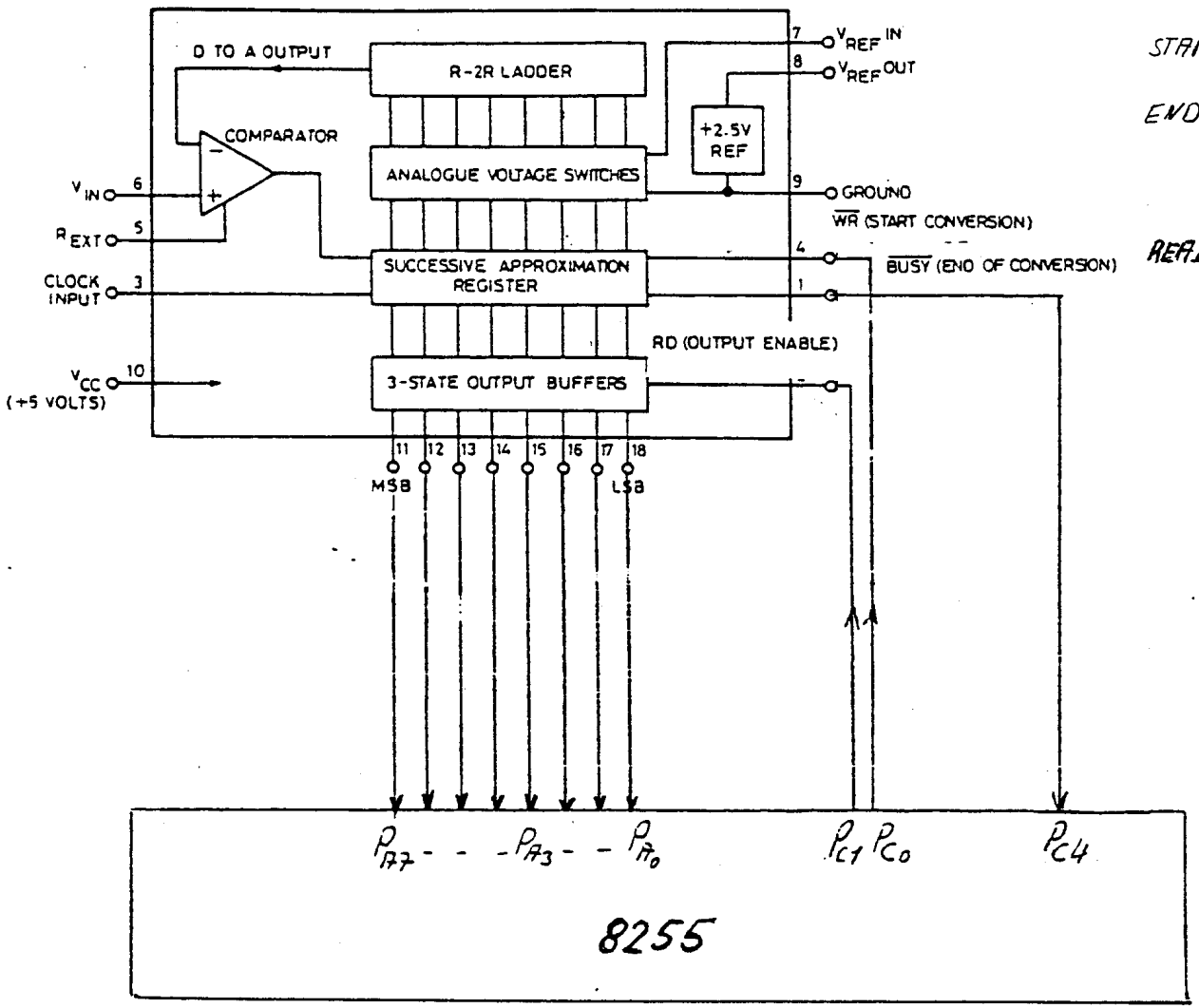

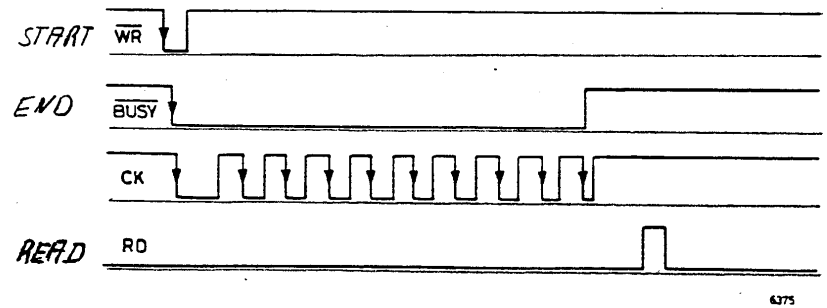

Timing Diagramm

8-Bit A/D-Wandler
(Sukzessive Approximation)

Isolierte Ein-/Ausgabe (isolated I/O)

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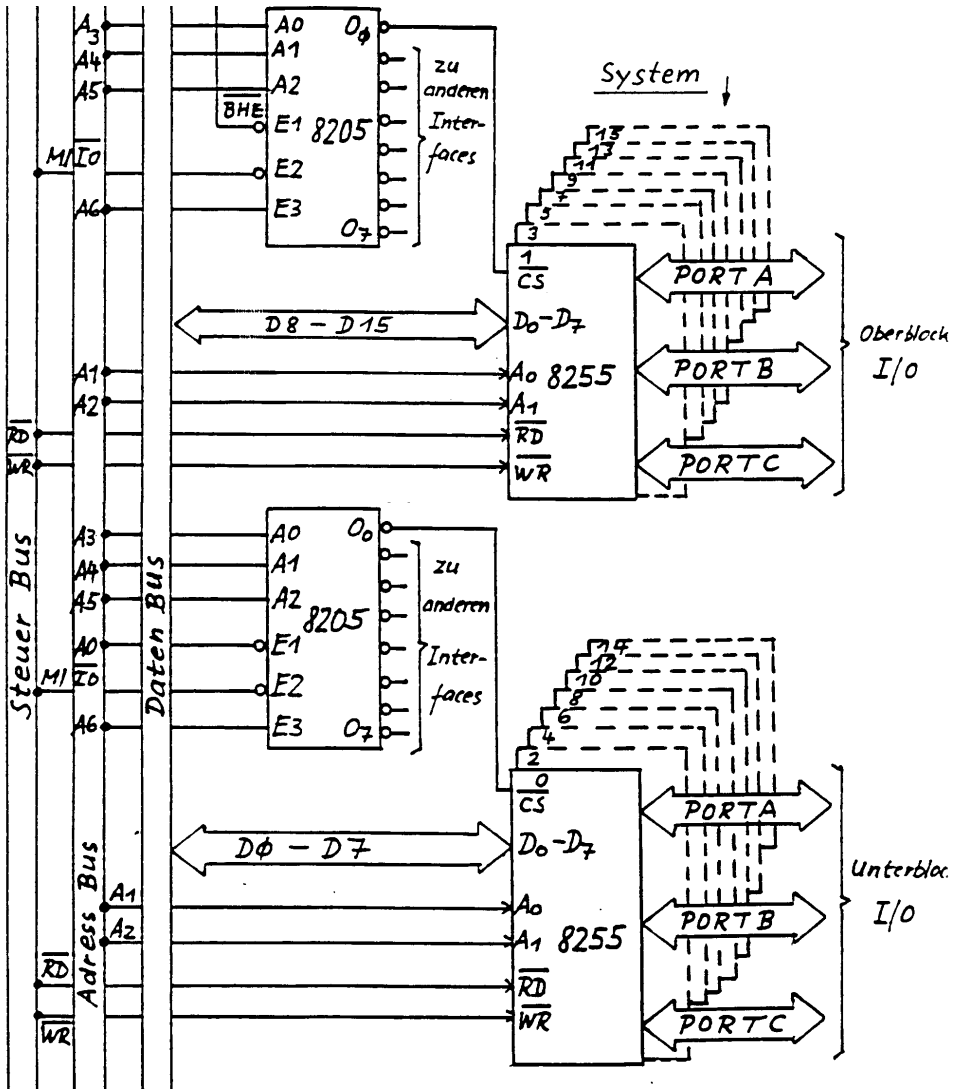


In der angegebenen Systemkonfiguration können Word- und Bytetransfers unter gerader und Bytetransfers unter ungerader Adresse durchgeführt werden.

Beispiele:

1) Word-Transfer mit gerader Adresse:
M/IO=L, A0=L, A6=H, /BHE=L
IN AX,40H oder: IN AX,DX mit [DX]=0040H

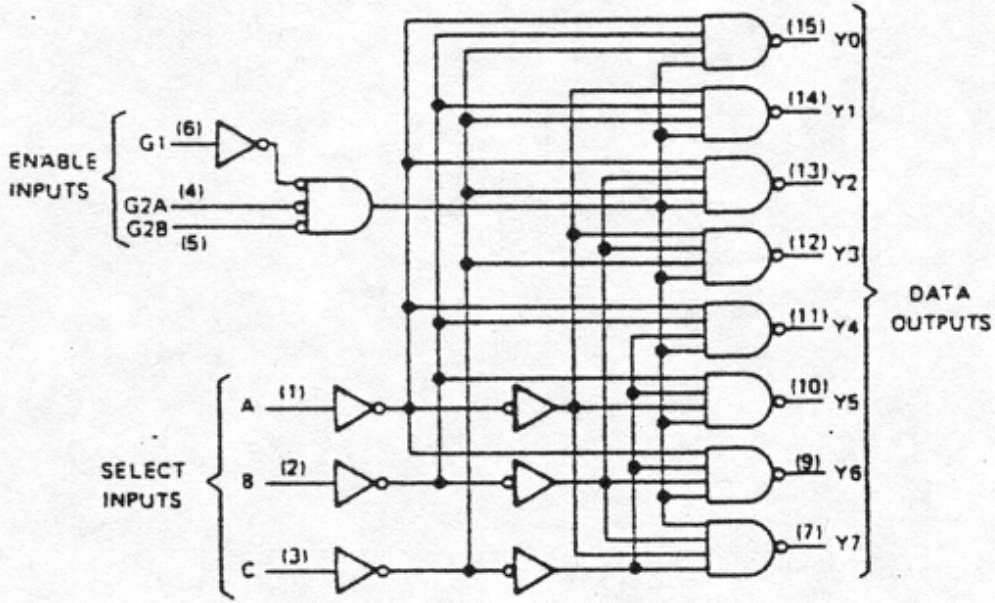
2) Byte-Transfer mit gerader Adresse:
M/IO=L, A0=L, A6=H, /BHE=H
OUT 40H,AL oder: OUT DX,AL mit [DX]=0040H

3) Byte-Transfer mit ungerader Adresse:
M/IO=L, A0=H, A6=H, /BHE=L
IN AL,41H oder: IN AL,DX mit [DX]=0041H

zu 1)

A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0

'LS138, 'S138



'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

Functional Block- Diagrams and Logic

Function Table

Quelle: Texas Instruments

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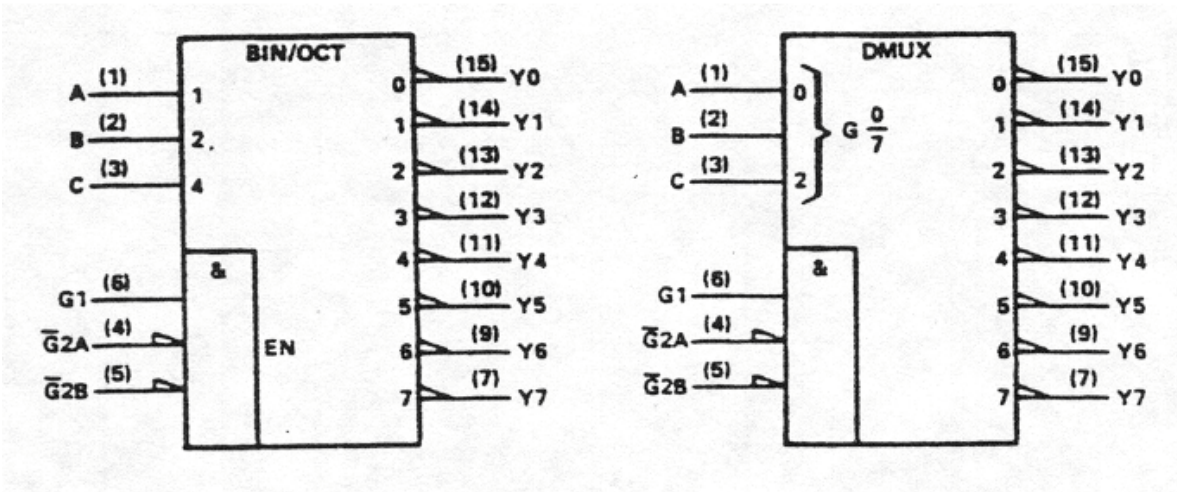
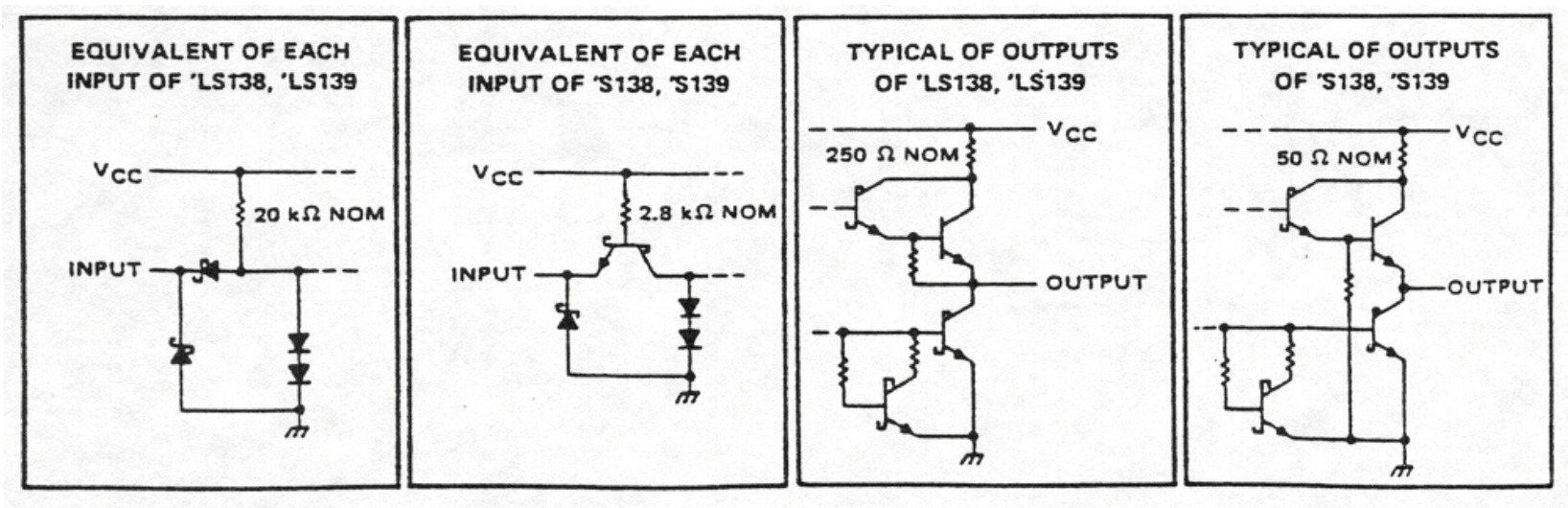


Symbole (alternative Darstellungen)



Schematics der Inputs und Outputs

Quelle: Texas Instruments

TFH-Berlin

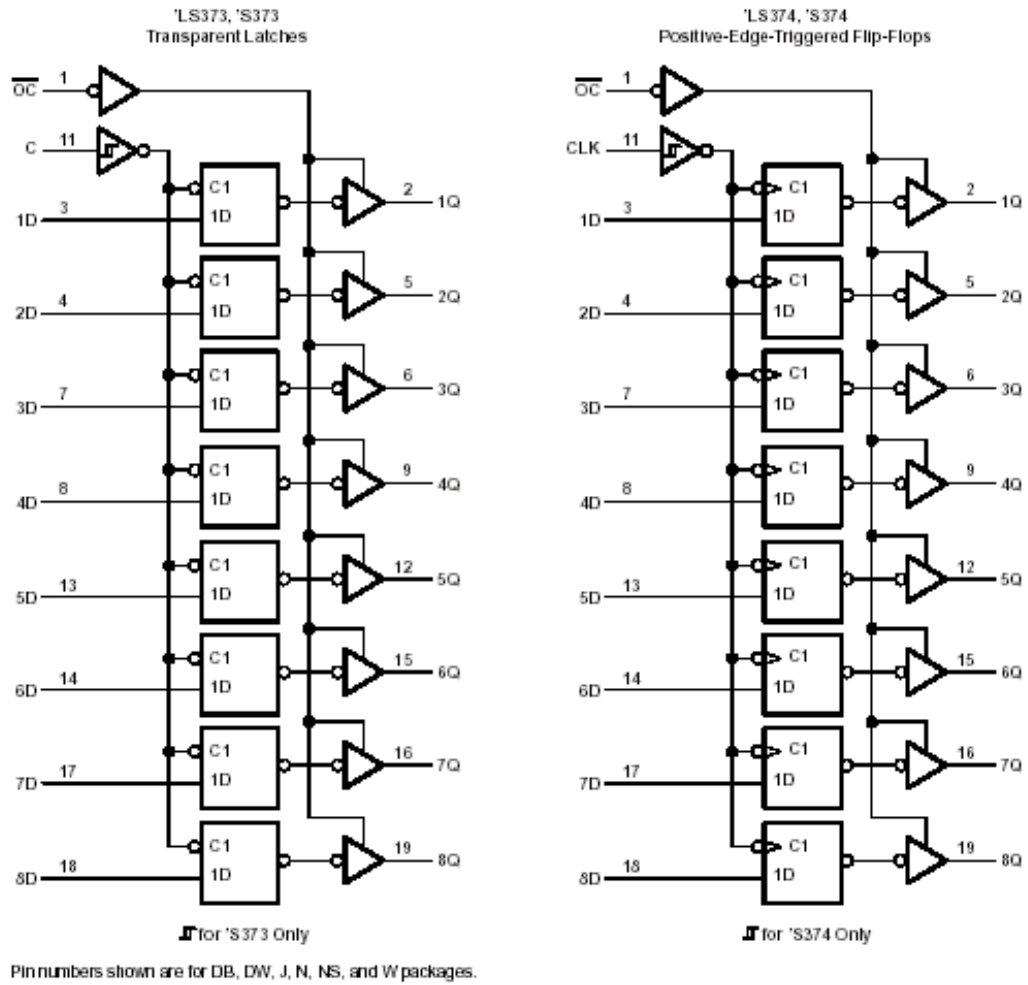
'LS373, 'S373 (each latch)

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'LS374, 'S374 (each latch)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Function Tables



Logic Diagrams (positive logic)

Quelle: Texas Instruments