CSE 6230

Homework 1(b): Cache Basics

Due 11:59PM, Friday, 1/17/2020 (Check Canvas for updates to due date)

Submit pdf document on Carmen (can be image of handwritten solution) and also bring along a hardcopy to class - no late submissions).

All work must be performed individually

1. See in HW1 (a) on canvas
2. (10 points) Suppose a computer's address size is k bits (using byte addressing), cache capacity is C bytes, block size is $B = 2^b$ bytes, and it is E-way set-associative. Including the storage for the valid bit, tag, and data, what is the total number of bits of storage needed to implement the cache?
3. See in HW1 (a) on canvas
4. (40 points) Consider the following loop:

```
float s, A[size]; int i, it;
s = 0.0;
for (it=0; it < 10; it++)
  for (i=0; i<size; i++)
    s +=A[i];
```

Consider the execution of the code on a system containing a direct-mapped L1 cache with block-size 16 words and capacity 8K words, and a 2-way set-associative L2 cache with block size B2 = 32 words and capacity C2 = 64K words. Assume L1 hit time to be a t_1, L2 hit time to be t_2, and t_m to be the access time for memory (i.e., miss penalty for the L2 cache). Provide analysis of the average memory access time for each of the following three cases (assume s, i, and it, and size are held in registers):

(a) size ≤ 8K
(b) 8K < size ≤ 64K
(c) size > 64K