2023 Digital IC Design Homework 5

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| **Simulation Result** | | | | |
| Functional simulation | | Completed | Gate-level simulation | Completed |
|  | | |  | |
| **Evaluation Results** | | | | |
| test1.png | | 25.32 | test2.png | 24.82 |
| test3.png | | 29.12 | test4.png | 20.95 |
| test5.png | | 21.94 | test6.png | 25.21 |
| **Description of your design** | | | | |
| 因為這次作業不看cycle跟元件數，所以我把state拆得很細，方便我debug  ，我一開始先把所有資料接進來，屬於綠的放進G的MEM，同理R跟B，在計算上，因為有四種不同的區塊，但分類方式跟前面放資料一樣，所以分4種state(S2\_x, S3\_x, S4\_x, S5\_x)，x又分為三個階段，決定要取哪個值、取值、計算後放回去，S6更新位置，S7判斷結束了沒，因為我是最一開始就做了的，所以我得作法會得到126\*126的圖 | | | | |

*Scoring = average PSNR of the six test images*

**\* PSNR of all interpolation results should meet at least the baseline.**