

ATHENS UNIVERSITY OF ECONOMICS AND BUSINESS

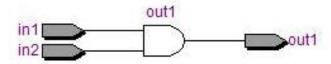
Αρχιτεμτονική Υπολογιστών

ΠΡΩΤΗ ΕΡΓΑΣΙΑ

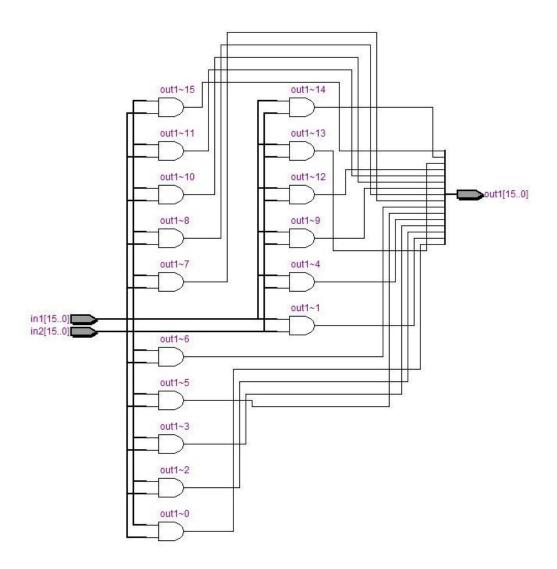
Στεφάνου Δημήτριος 3160245 Σωτηροπούλου Δικαία 3160172 Ομάδα 15

RTLs

AND Gate



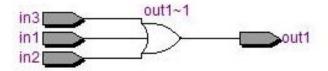
AND Gate (16 bits)



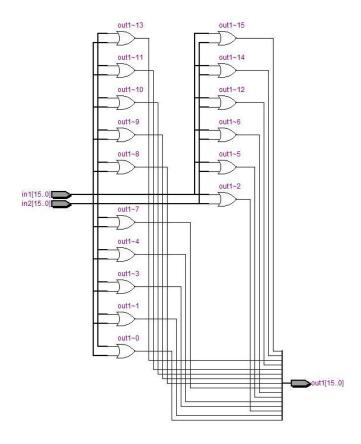
NOT Gate (16bits)



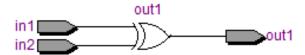
OR Gate (3 inputs)



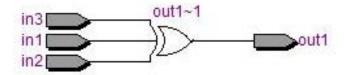
OR Gate (16 bits)



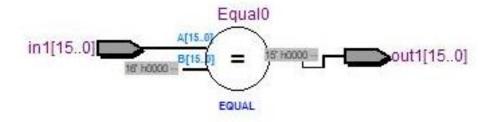
XOR Gate



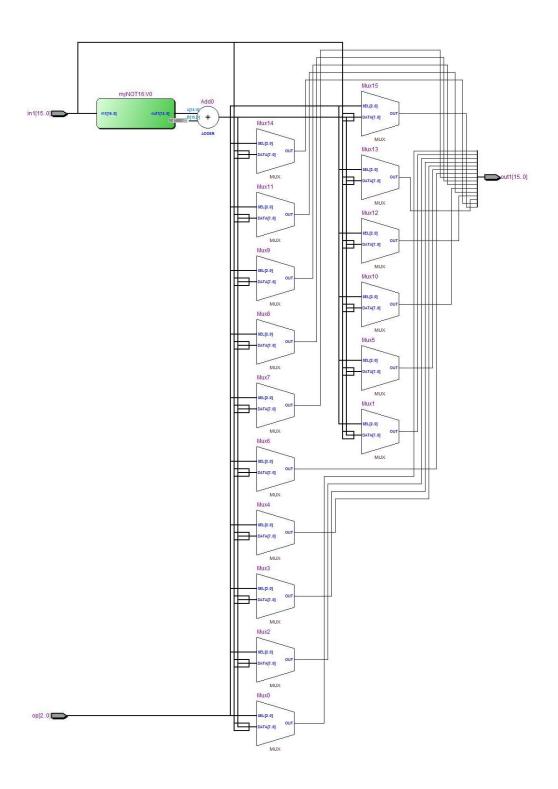
XOR Gate (3 inputs)



NOT (ALU implementation)

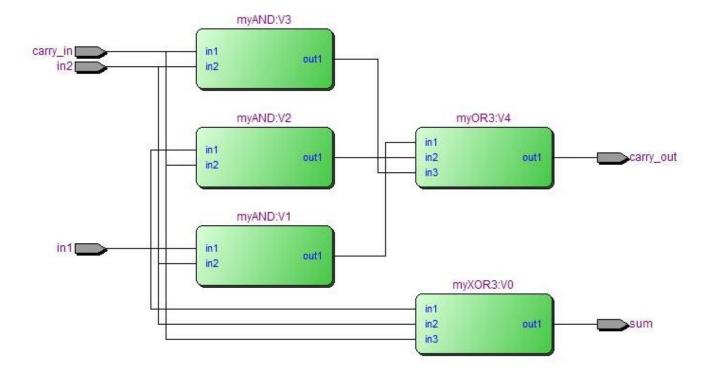


Two's Complement

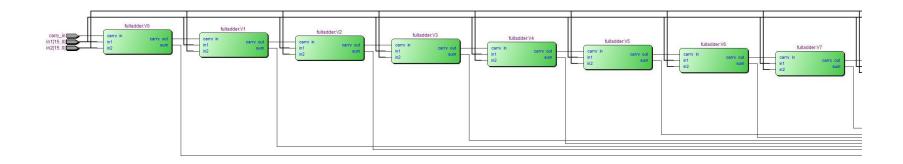


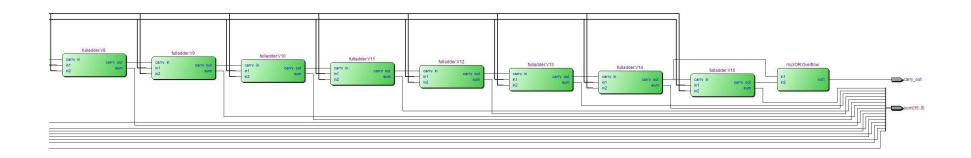


Full Adder (1 bit)



Full Adder (16 bits)

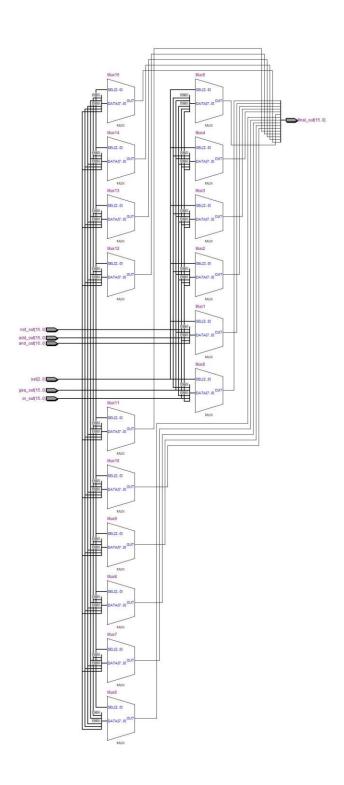




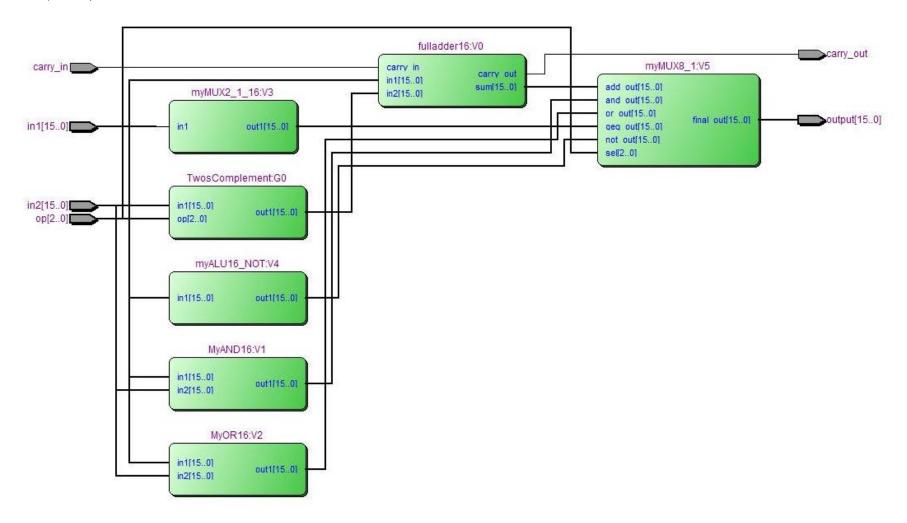
Multiplexer 2 to 1 (16 bits)



Multiplexer 8 to 1



ALU (16 bits)

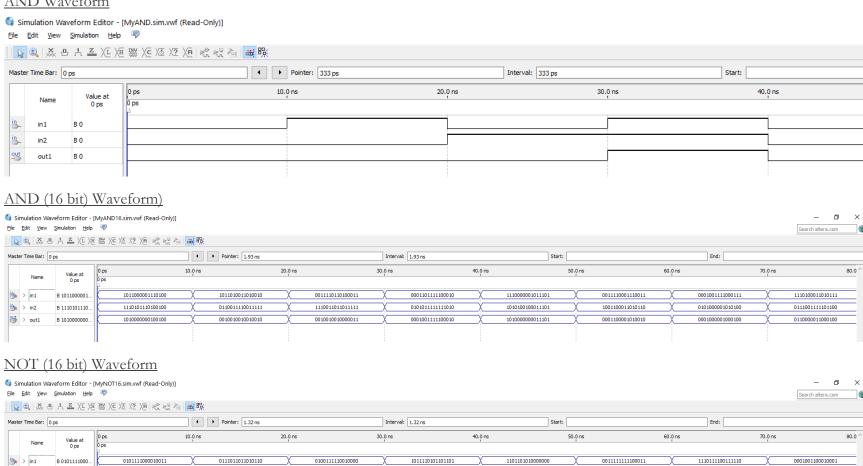


Waveforms

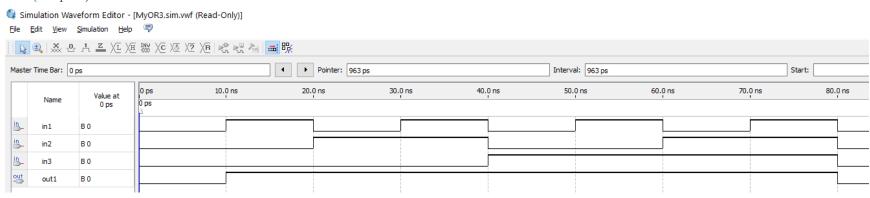
AND Waveform

out1 > out1

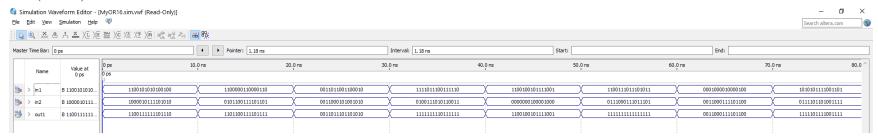
B 1010000111.



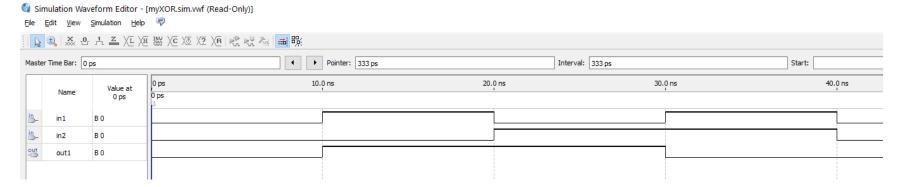
OR (3 inputs) Waveform



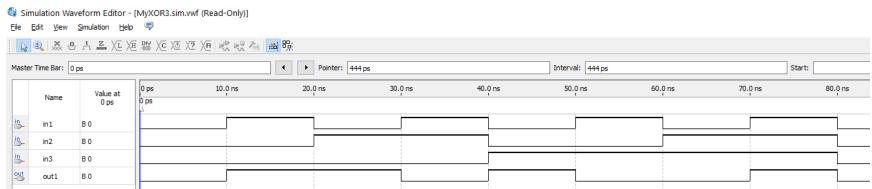
OR (16 bits) Waveform



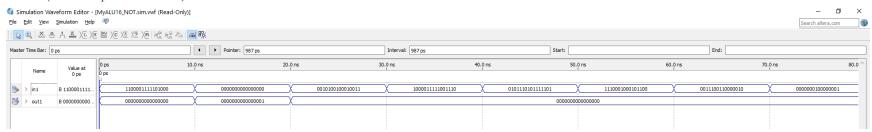
XOR Waveform



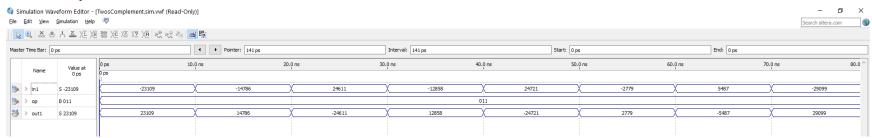
XOR (3 inputs) Waveform



NOT (ALU implementation) Waveform



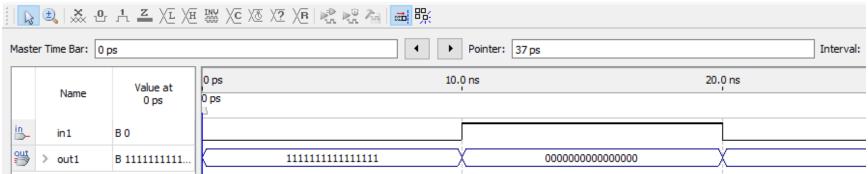
Two's Complement



Multiplexer 2 to 1 (16 bit)

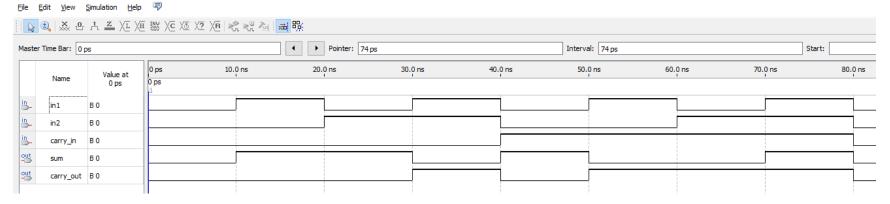
Simulation Waveform Editor - [MyMUX2_1_16.sim.vwf (Read-Only)]

File Edit View Simulation Help

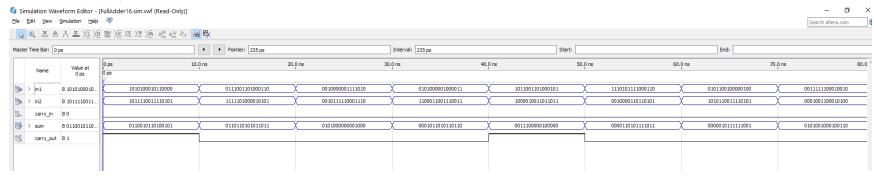


Full Adder (1 bit) Waveform

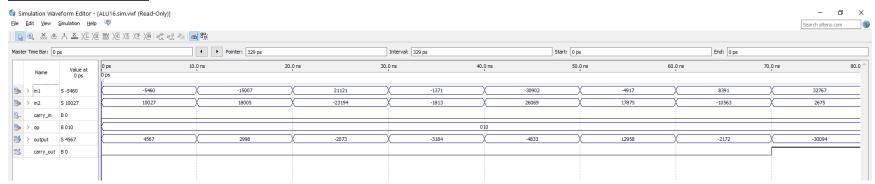
🥞 Simulation Waveform Editor - [FullAdder.sim.vwf (Read-Only)]



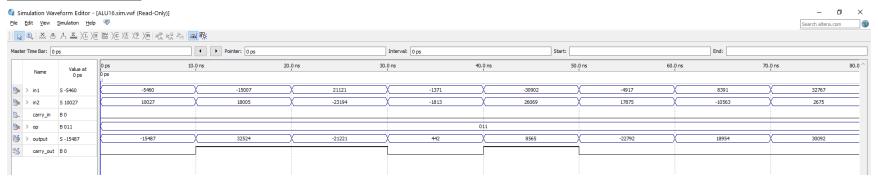
Full Adder (16 bit) Waveform



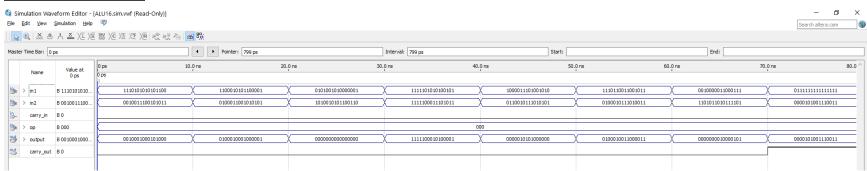
ALU ADD Waveform



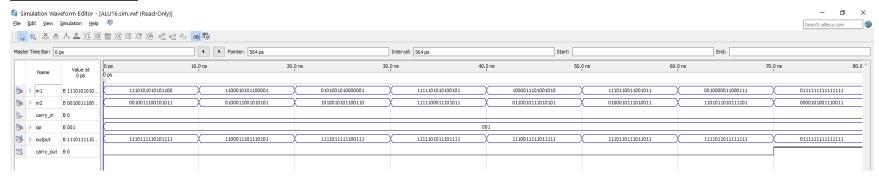
ALU SUB Waveform



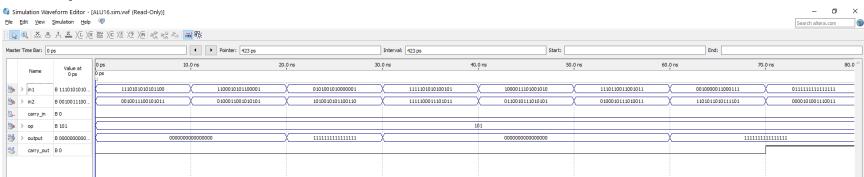
ALU AND Waveform



ALU OR Waveform



ALU GEQ Waveform



ALU NOT Waveform

