ATHENS UNIVERSITY
OF ECONOMICS
AND BUSINESS

Αρχιτεκτονική Υπολογιστών

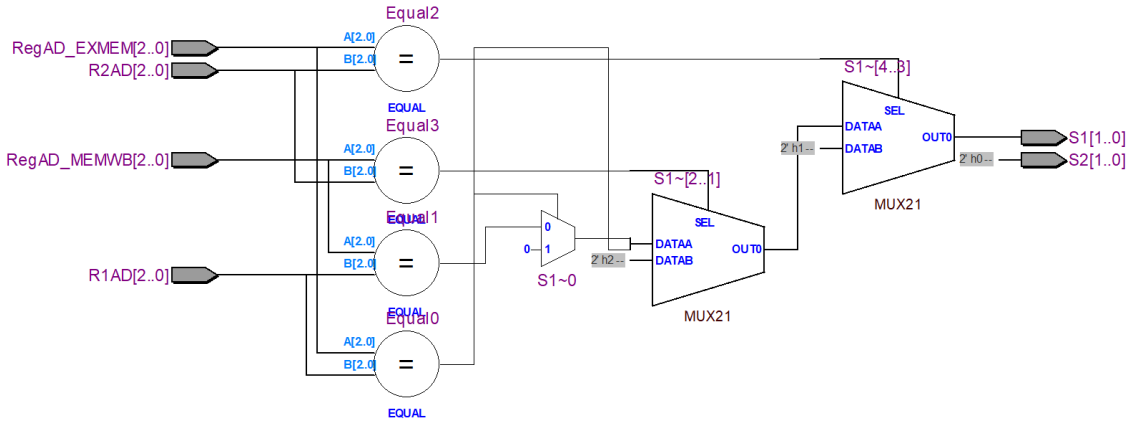
ΤΡΙΤΗ ΕΡΓΑΣΙΑ

Στεφάνου Δημήτριος 3160245
Σωτηροπούλου Δικαία 3160172

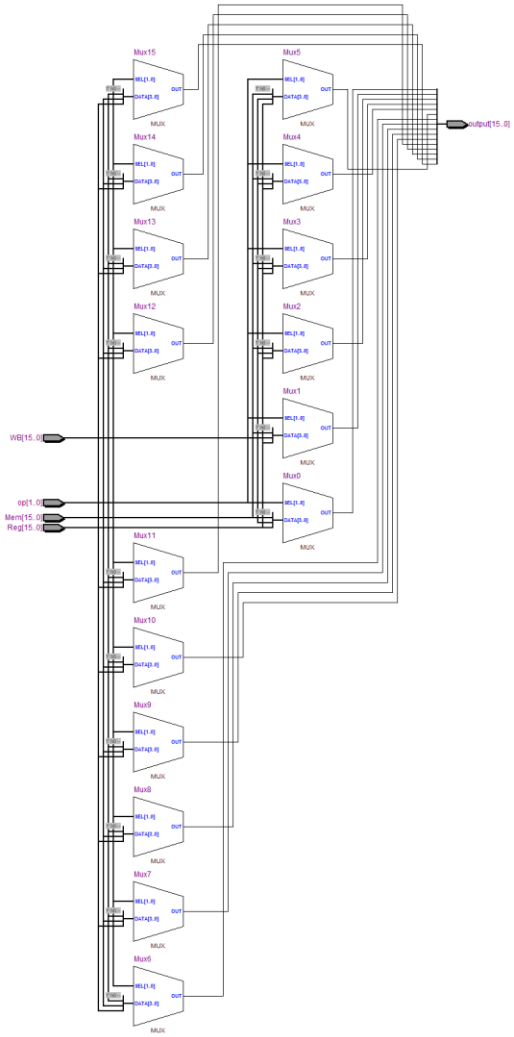
2021

RTLs

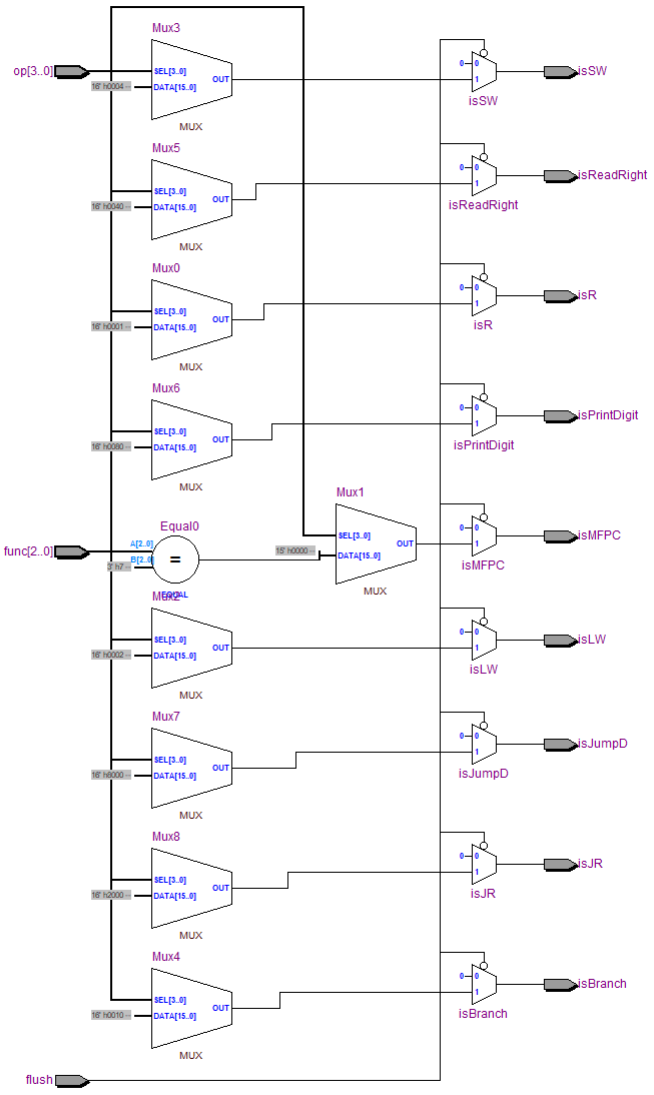
Forwarder



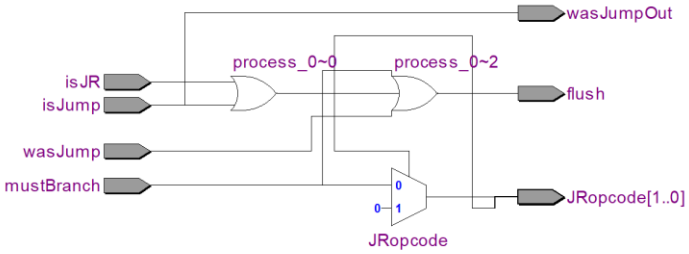
Selector



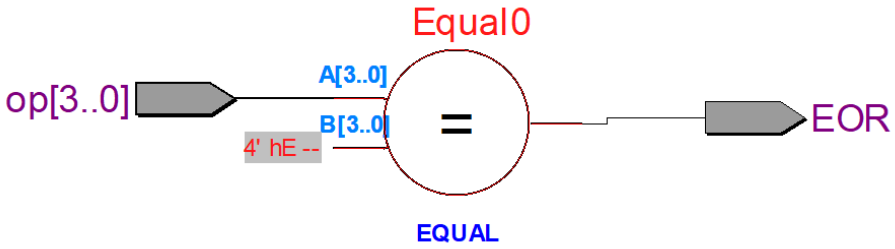
Control (Controller)



Hazard Unit



Trap Unit



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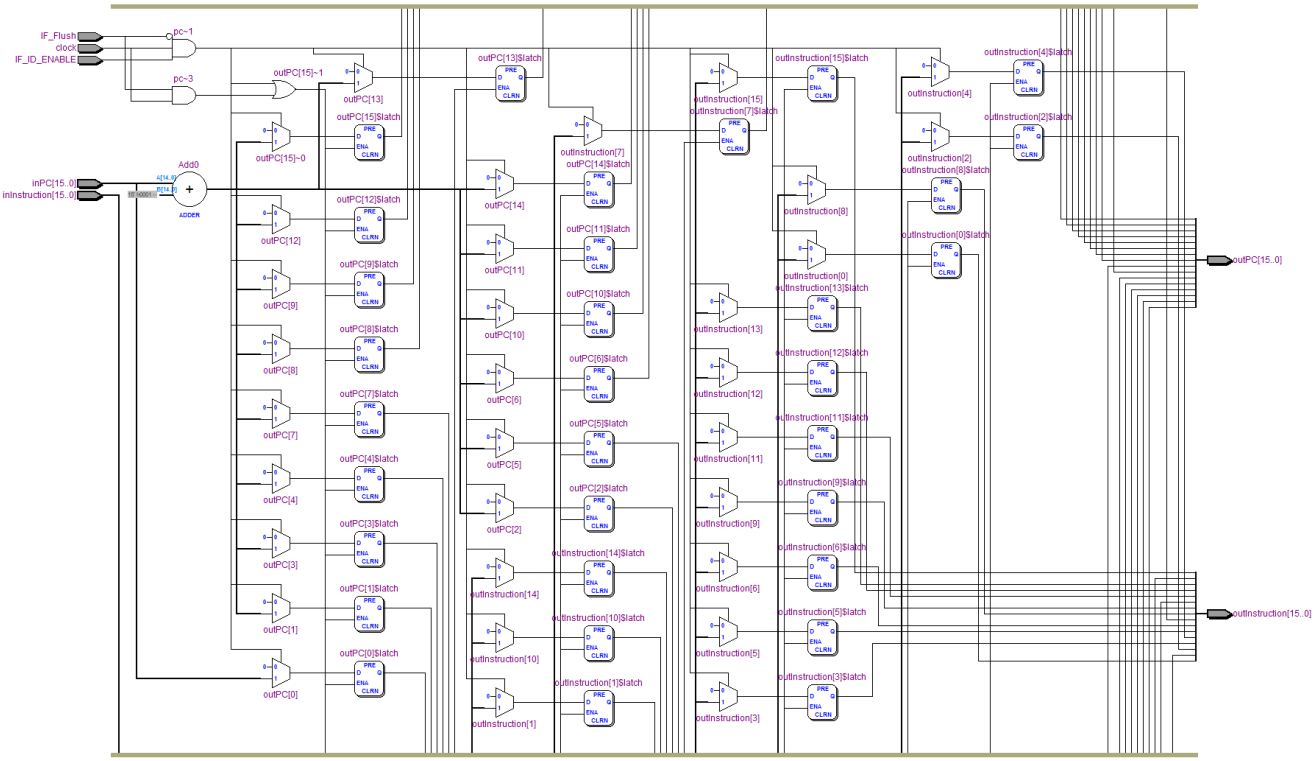

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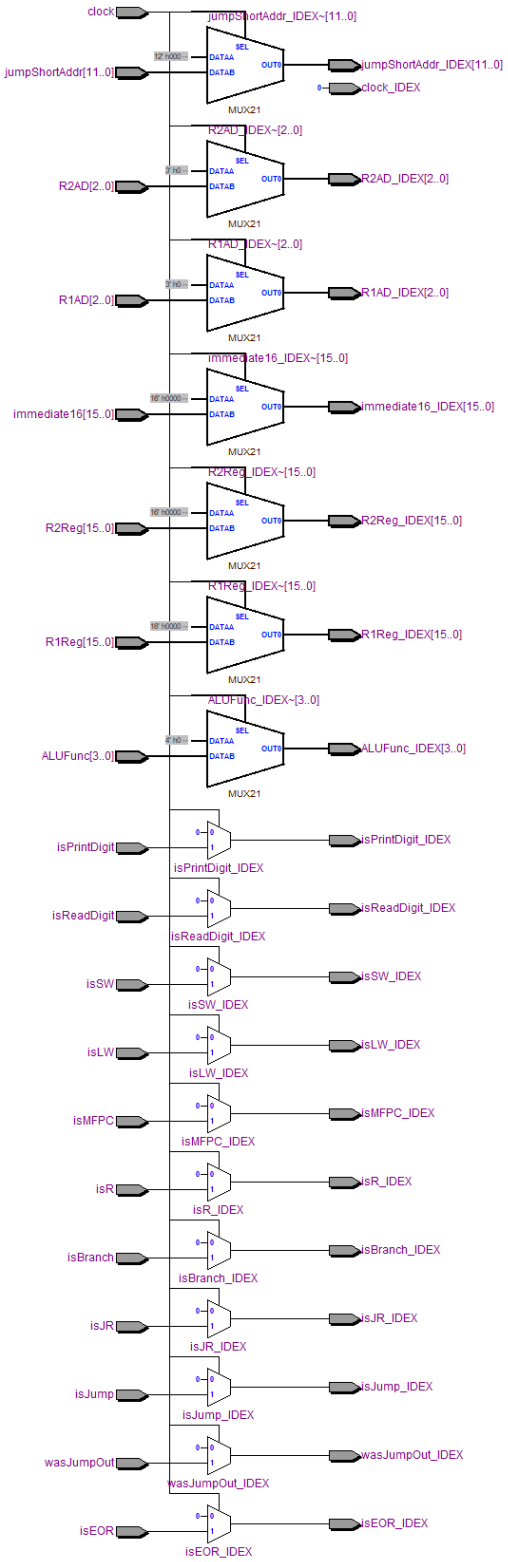
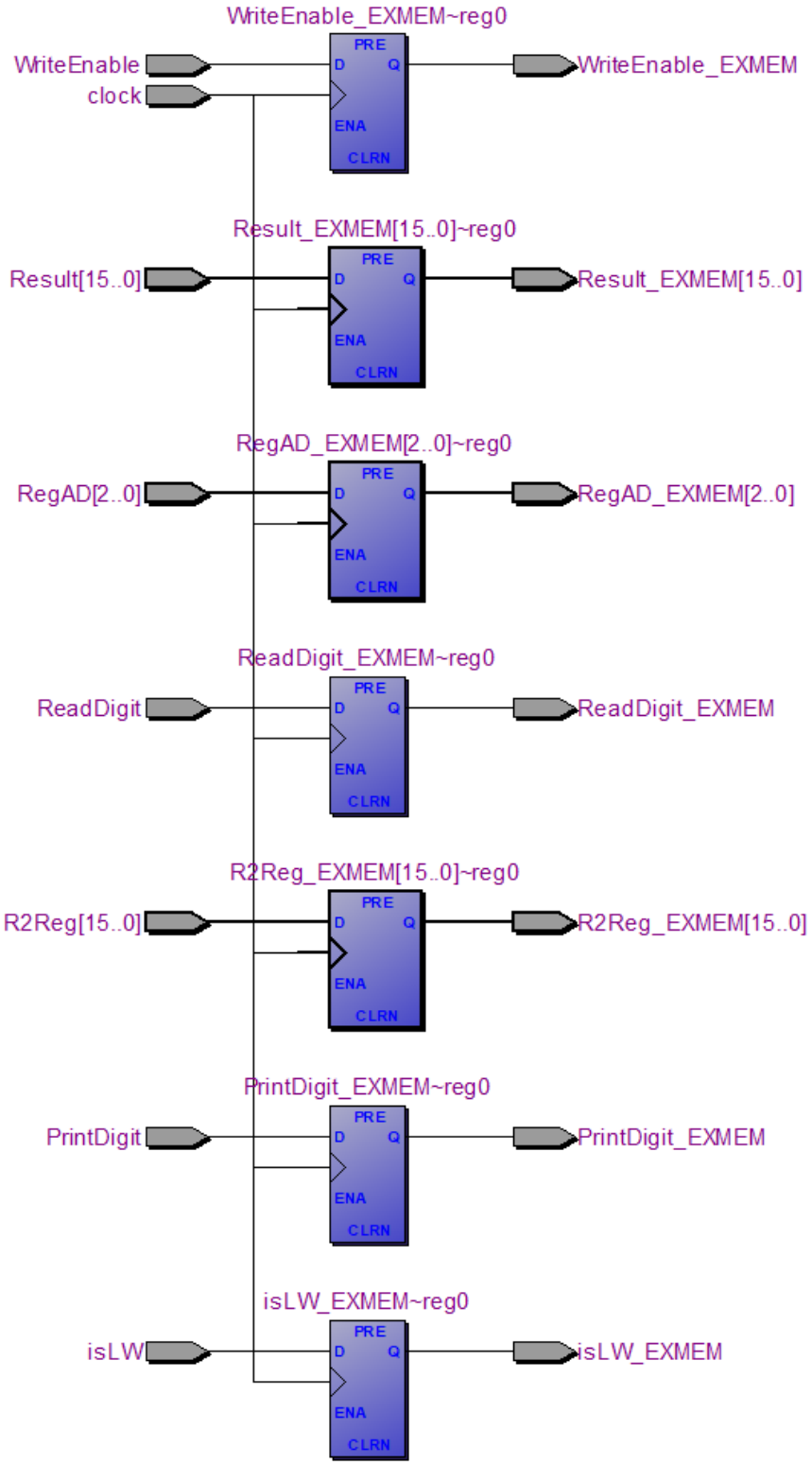
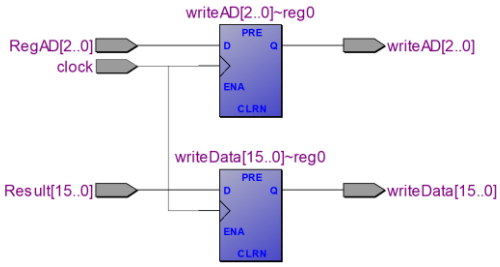


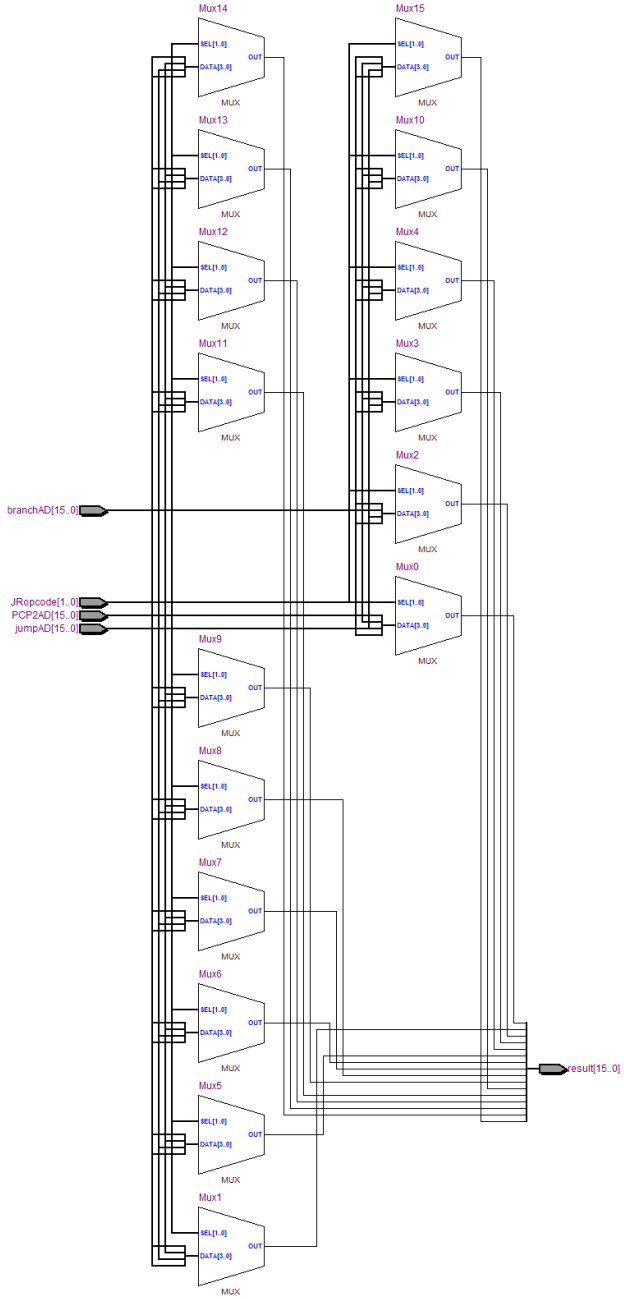
Register EX MEM



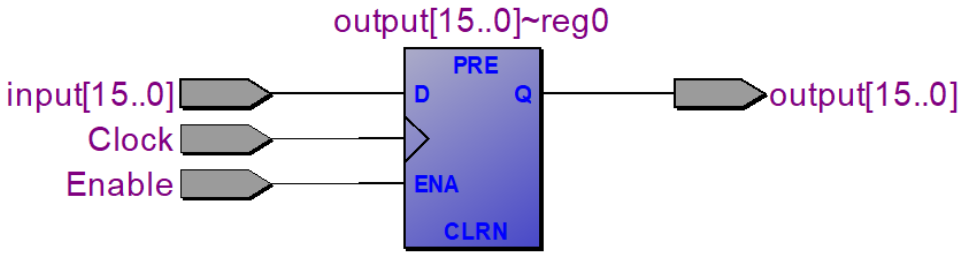
Register MEM WB

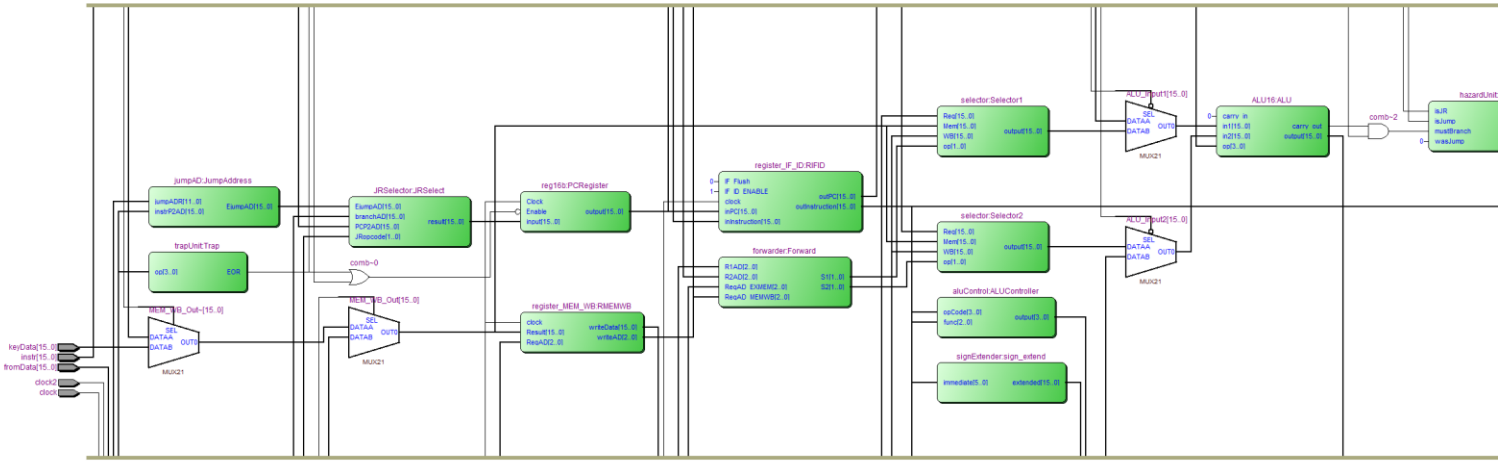


JR Selector



PC Register (Reg16b)

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reg16b:PCRegister
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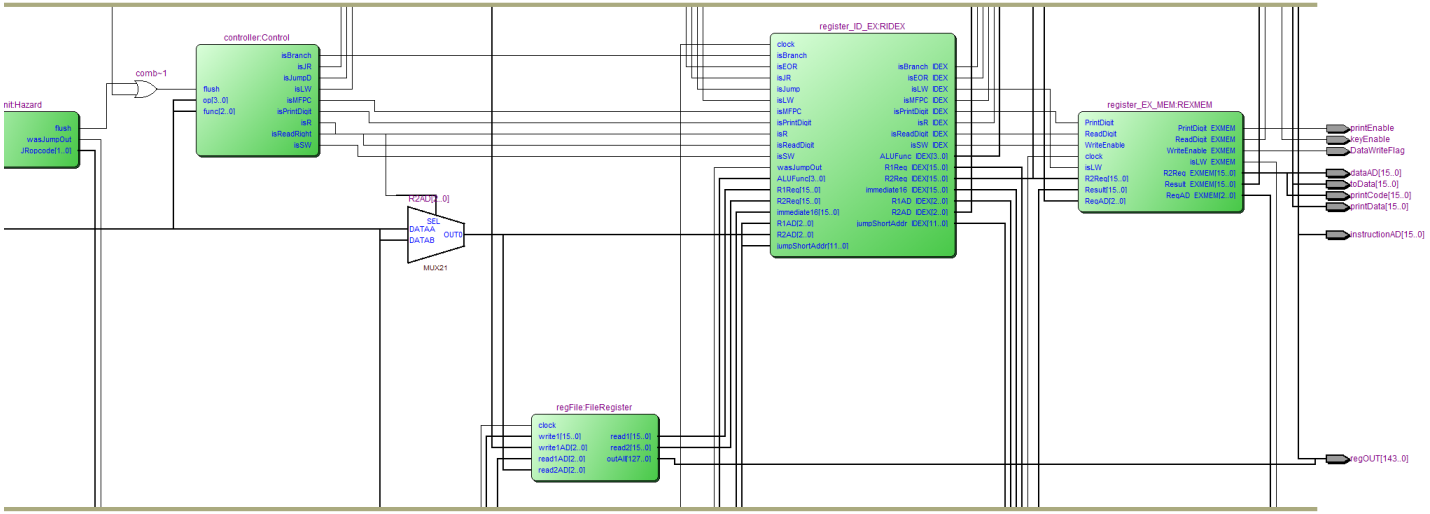
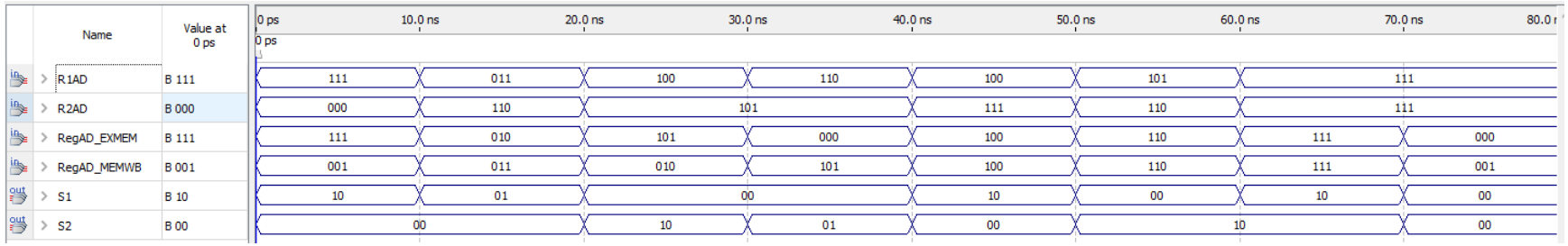
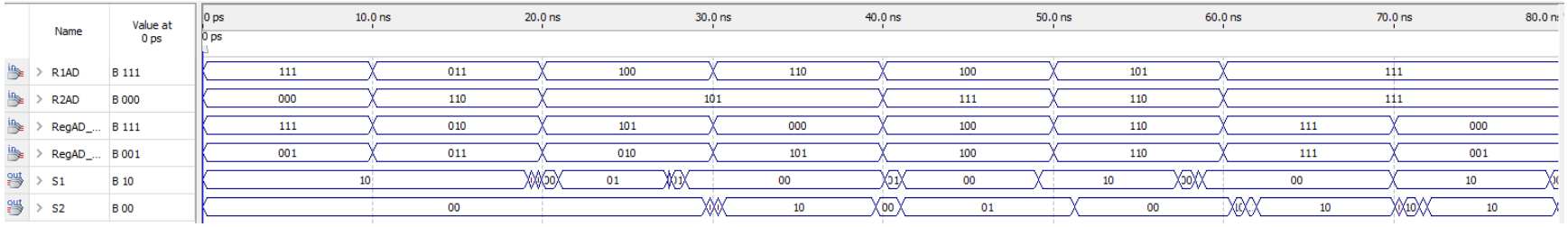
ALU16:ALU
hazardUnit
trapUnit:Trap
forwarder:Forward
selector:Selector2
aluControl:ALUController
signExtender:sign_extend
MUX21


controller:Control
register_ID_EX:RIDEX
register_EX_MEM:REXMEM
regFile:FileRegister
MUX21

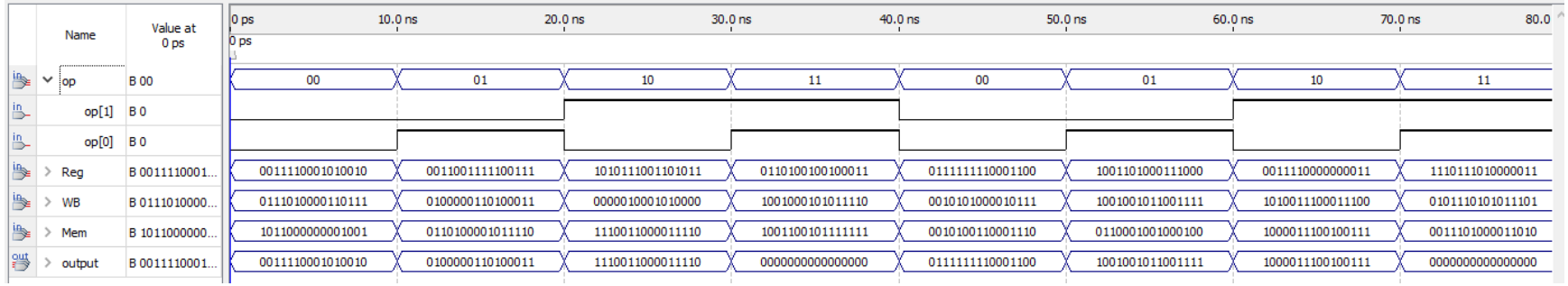
Waveforms (functional / timing simulations)

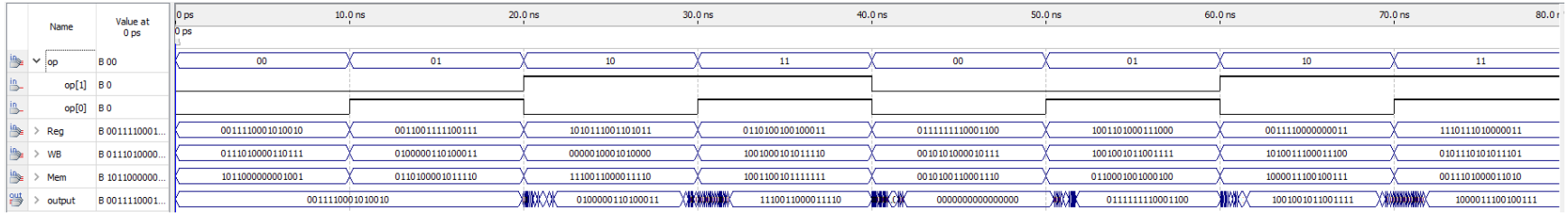
Forwarder



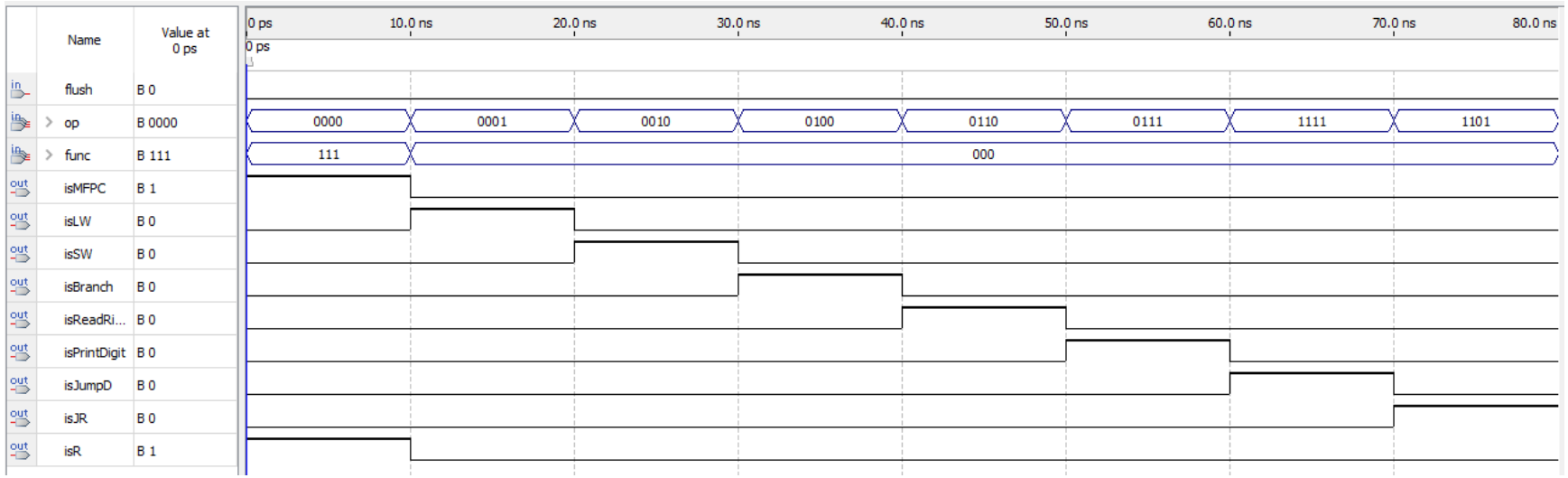


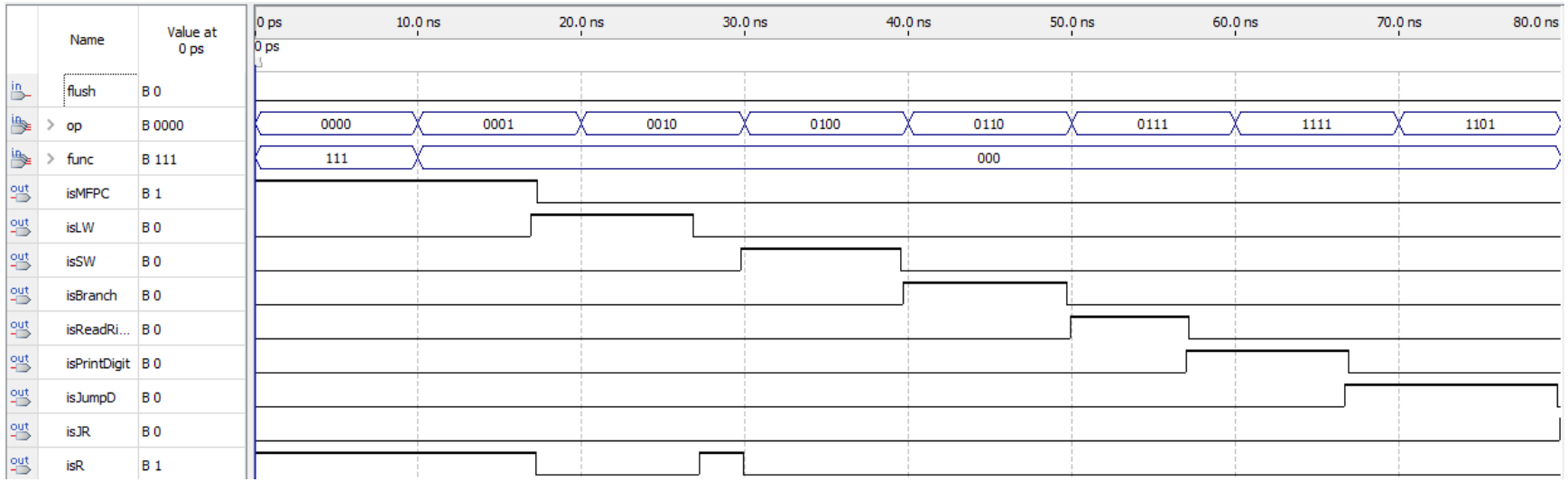
Selector



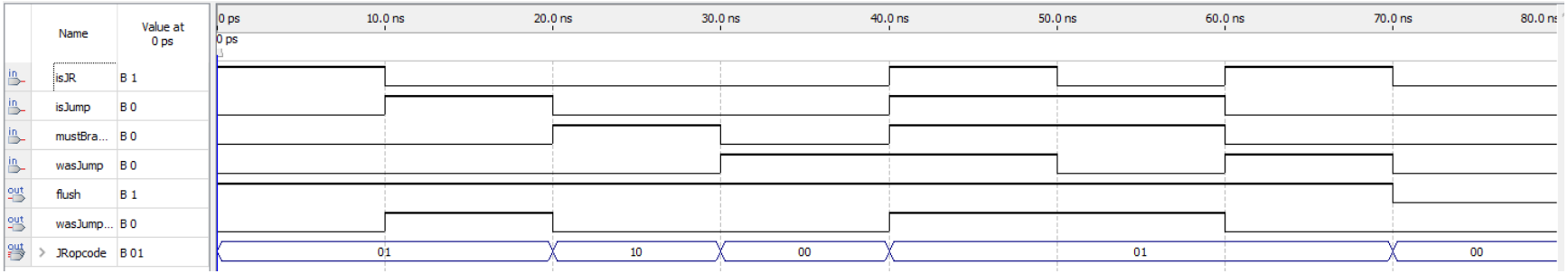


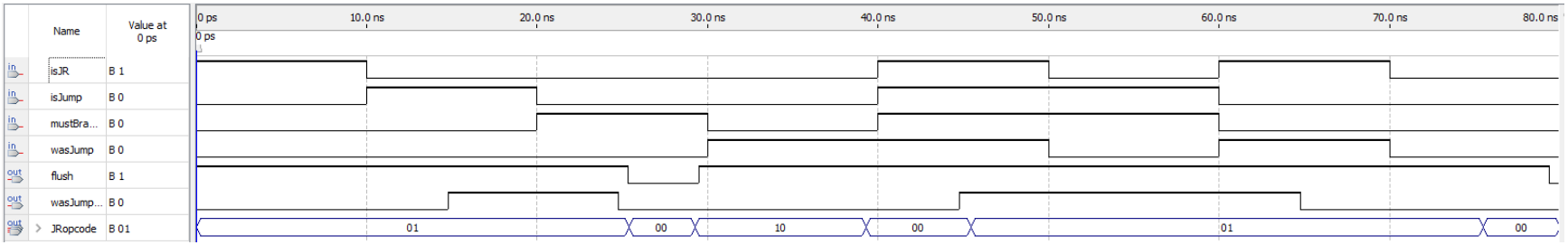
Control (Controller)



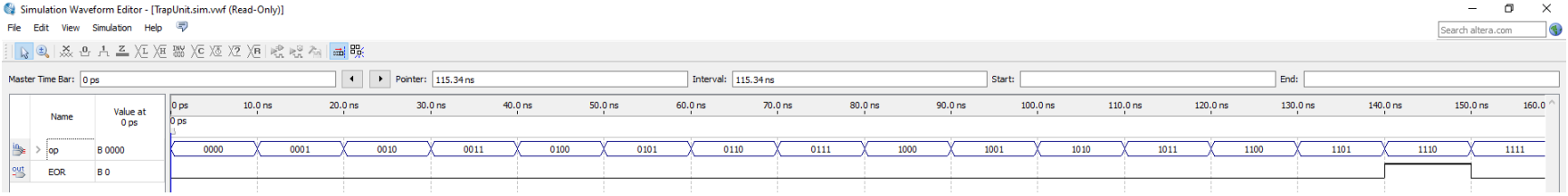


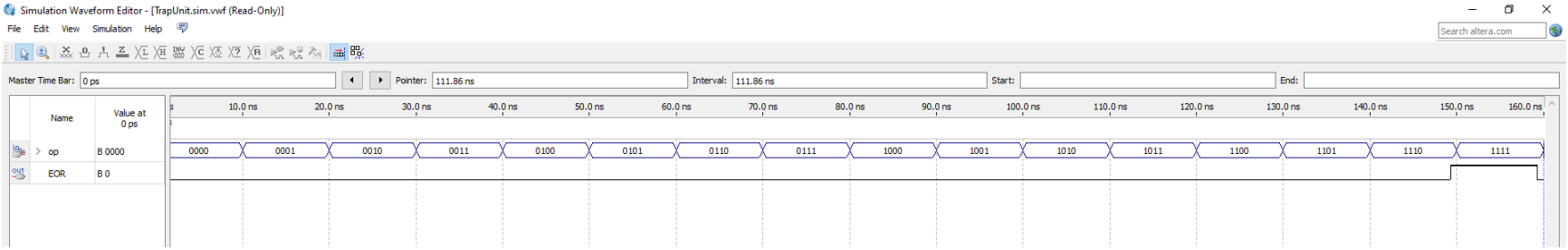
Hazard Unit



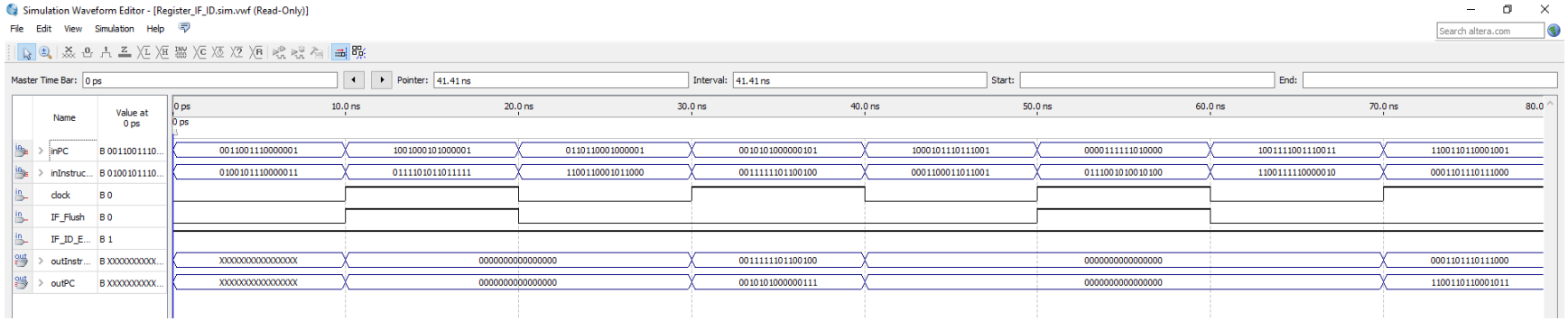


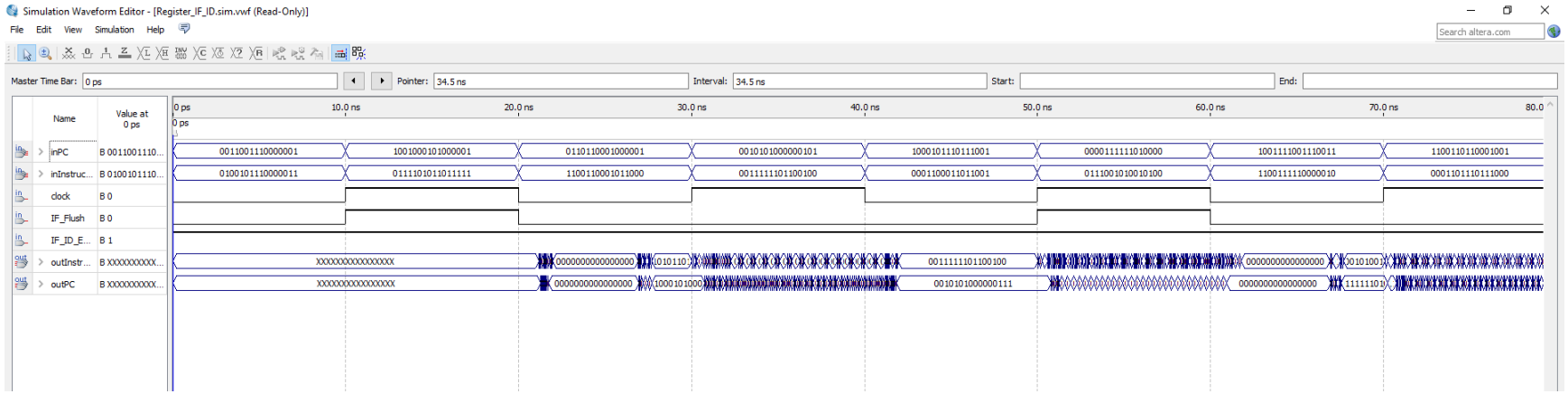
Trap Unit





Register IF ID





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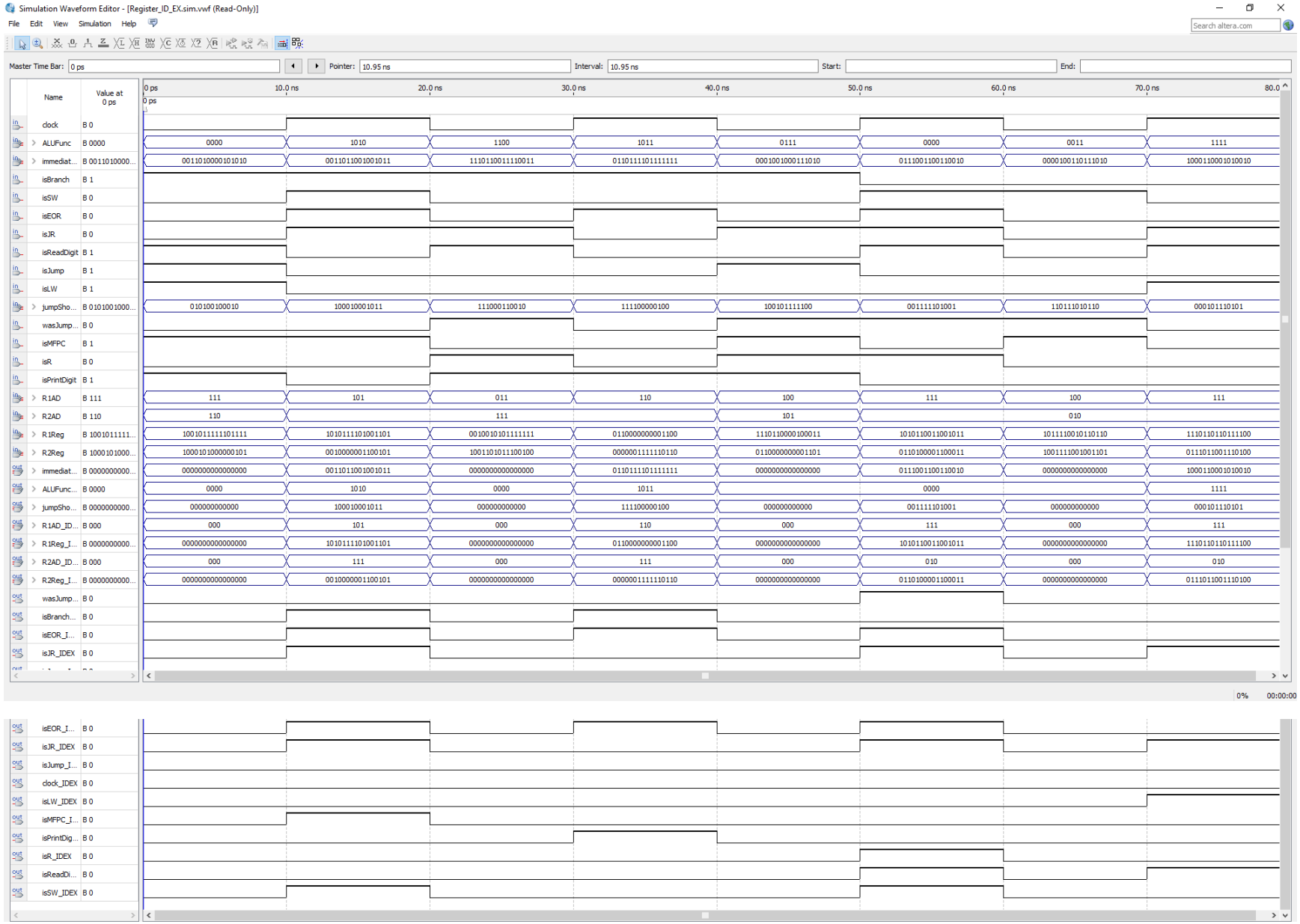

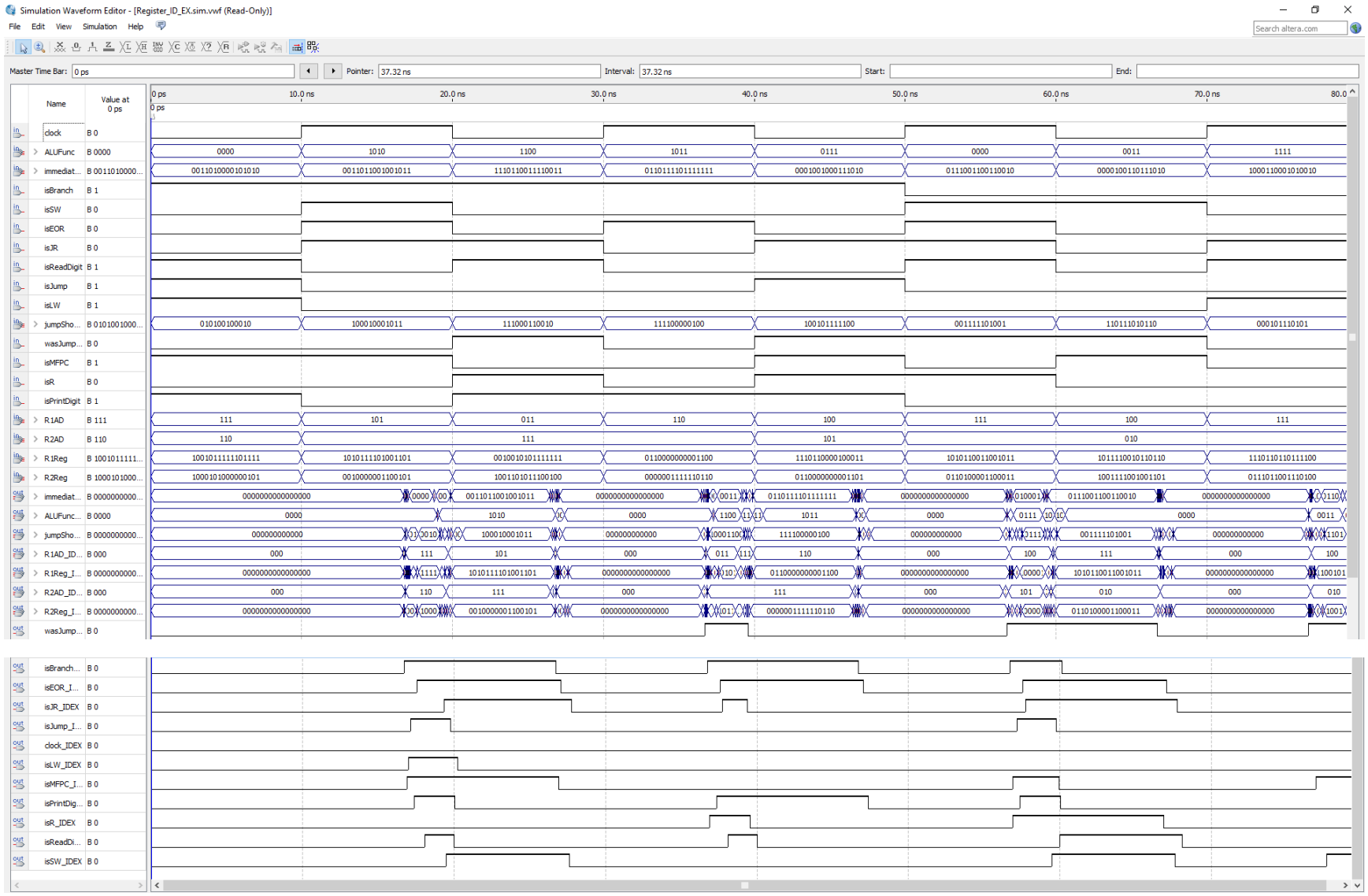
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Search altera.com
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Interval: 37.32 ns
Start:
End:
Name
Value at 0 ps
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0
clock
ALUFunc
immediat...
isBranch
isSW
isEOR
isJR
isReadDigit
isJump
isLW
jumpSho...
wasJump...
isMFPC
isR
isPrintDigit
R1AD
R2AD
R1Reg
R2Reg
immediat...
ALUFunc...
jumpSho...
R1AD_ID...
R1Reg_I...
R2AD_ID...
R2Reg_I...
wasJump...
isBranch...
isEOR_I...
isJR_IDEX
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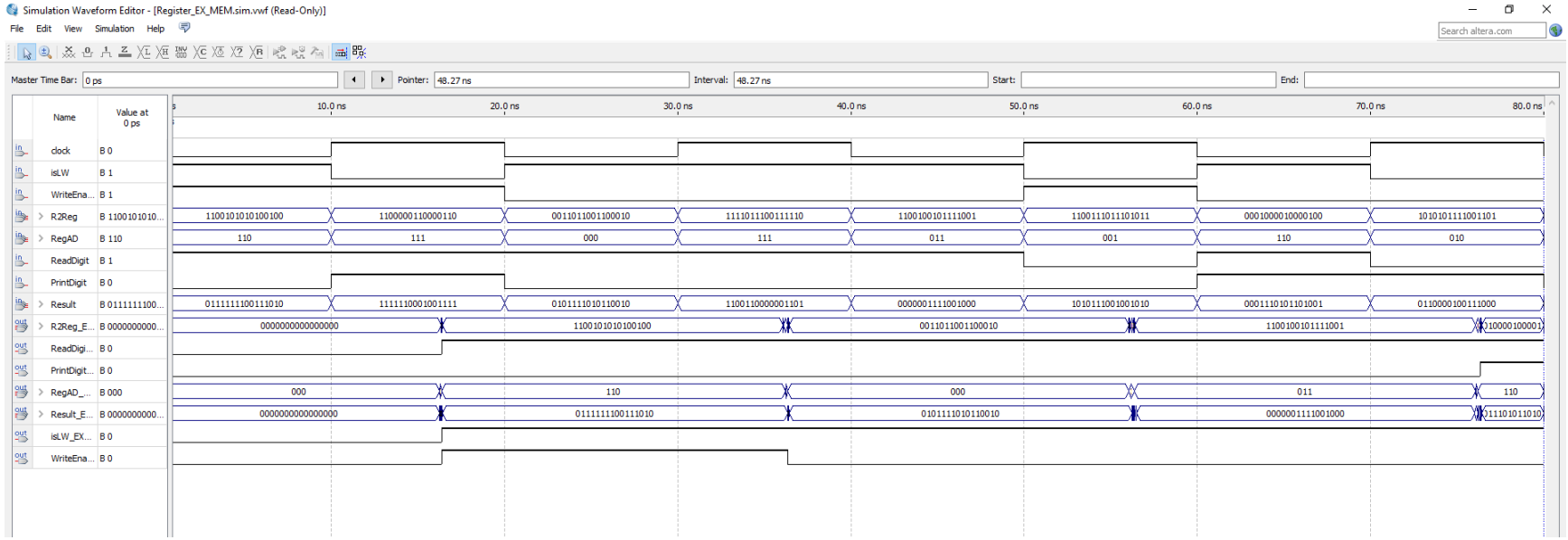
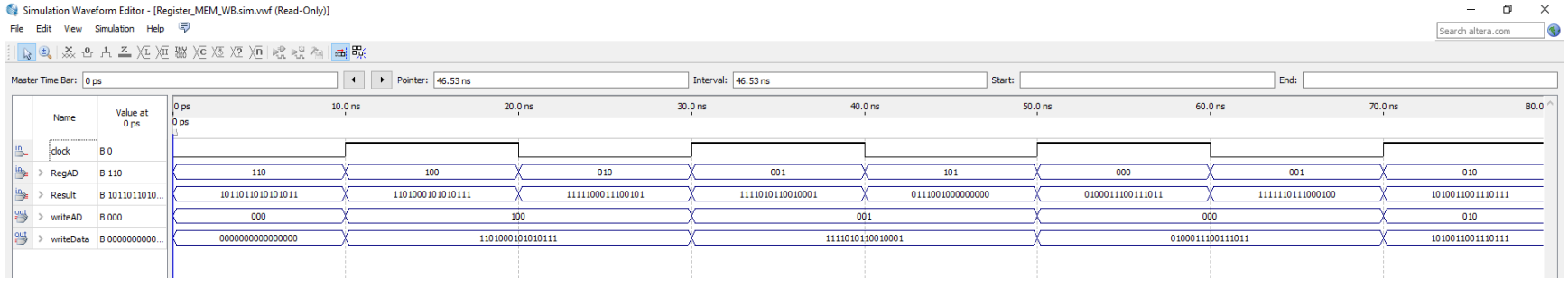
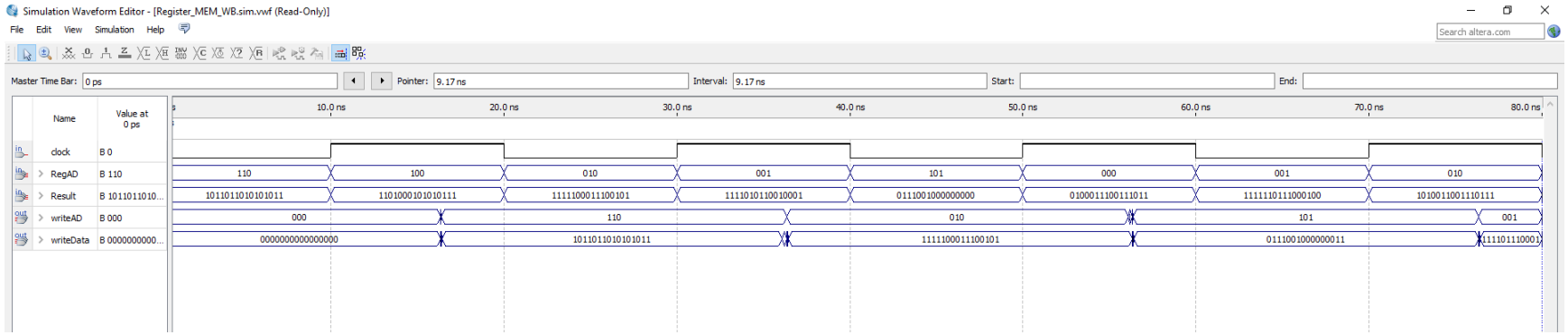
Register EX MEM

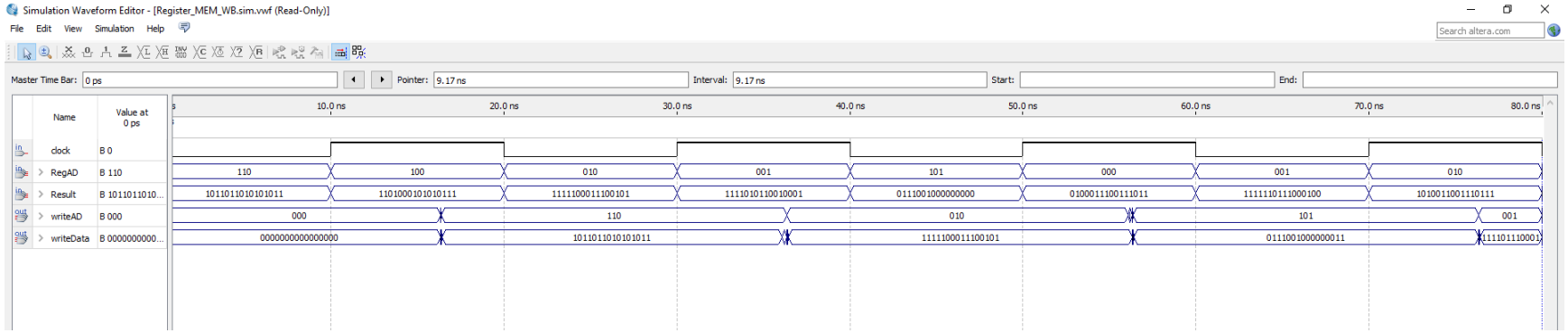


Register MEM WB





JR Selector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Search altera.com
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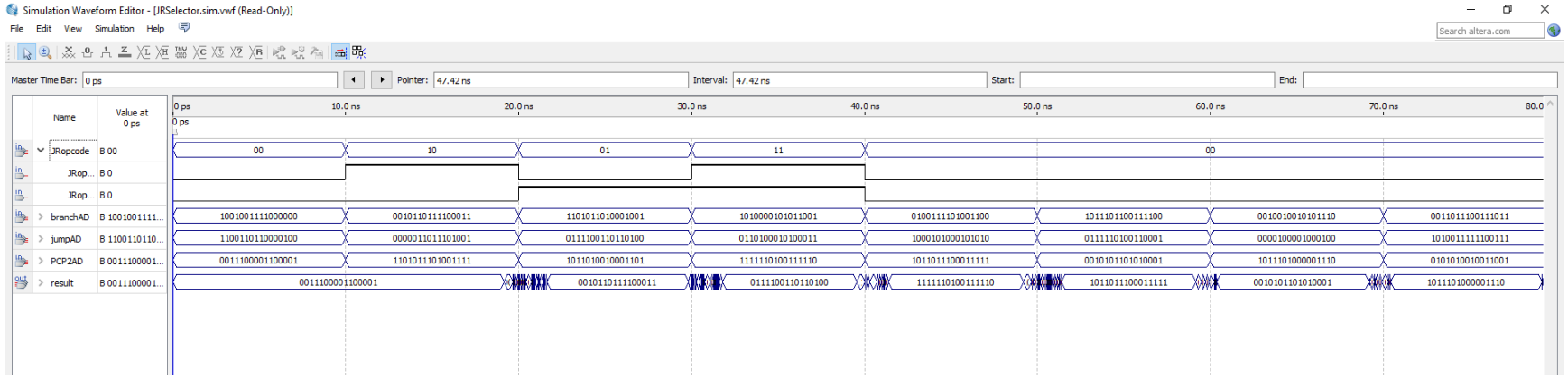
Interval: 9.17 ns
Start:
End:
Name
Value at 0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
clock B 0
RegAD B 110 110 100 010 001 101 000 001 010
Result B 1011011010... 1011011010101011 1101000101010111 1111100011100101 1111010110010001 0111001000000000 0100011100111011 1111110111000100 1010011001110111
writeAD B 000 000 110 010 101 001
writeData B 0000000000... 0000000000000000 1011011010101011 1111100011100101 0111001000000011 1111011100011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File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
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Interval: 47.42 ns
Start:
End:
Name
Value at 0 ps
0 ps
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20.0 ns
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40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0
JRopcode B 00 00 10 01 11 00
JRop... B 0
JRop... B 0
branchAD B 1001001111... 1001001111000000 0010110111100011 1101011010001001 1010000101011001 0100111101001100 1011101100111100 0010010010101110 0011011100111011
jumpAD B 1100110110... 1100110110000100 0000011011101001 0111100110110100 0110100010100011 1000101000101010 0111110100110001 0000100001000100 1010011111100111
PCP2AD B 0011100001... 0011100001100001 1101011101001111 1011010010001101 1111110100111110 1011011100011111 0010101101010001 1011101000001110 0101010010011001
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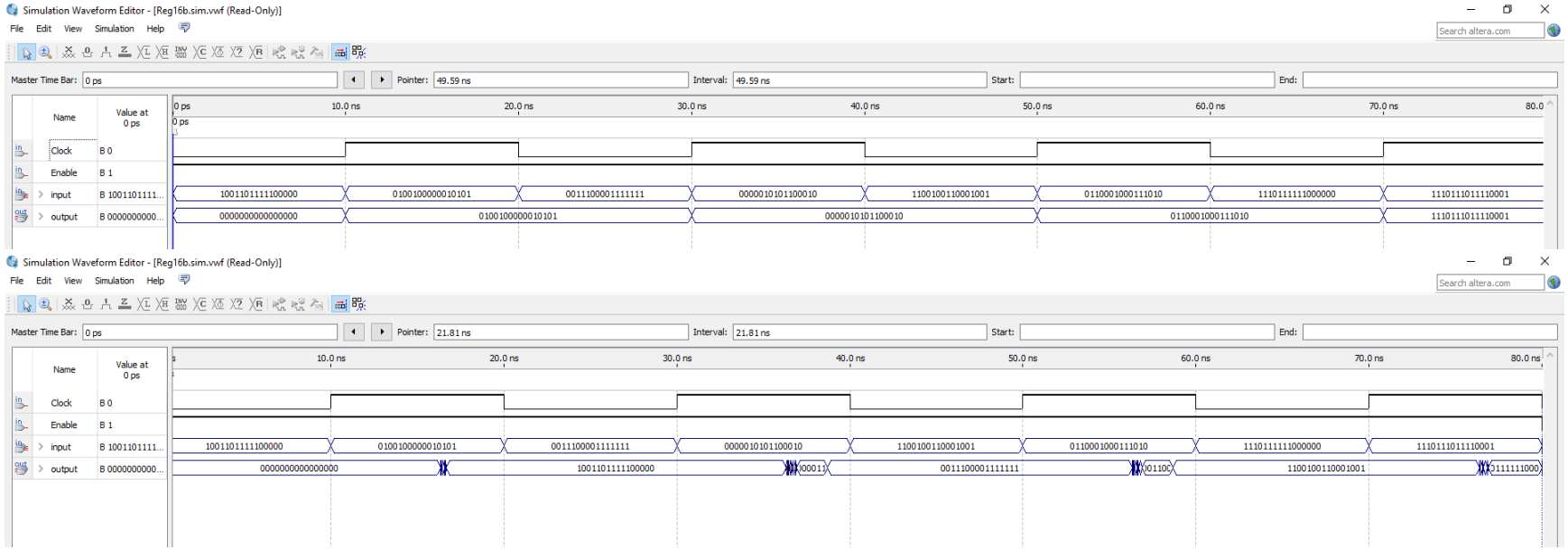
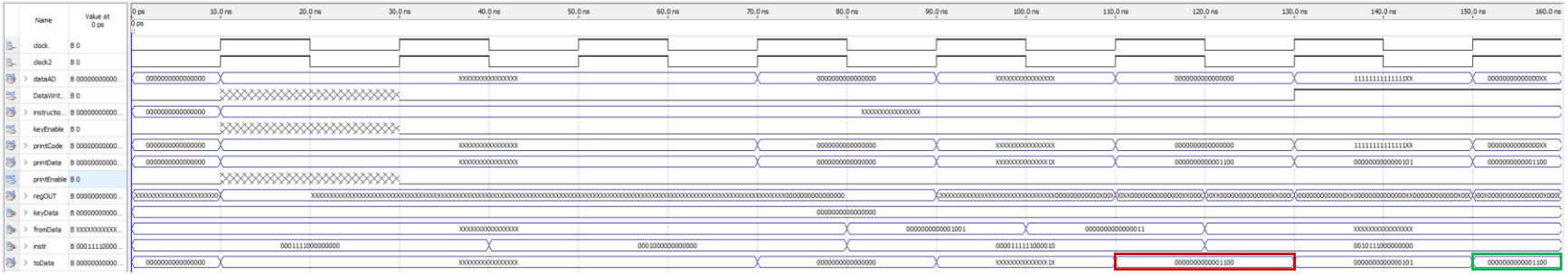
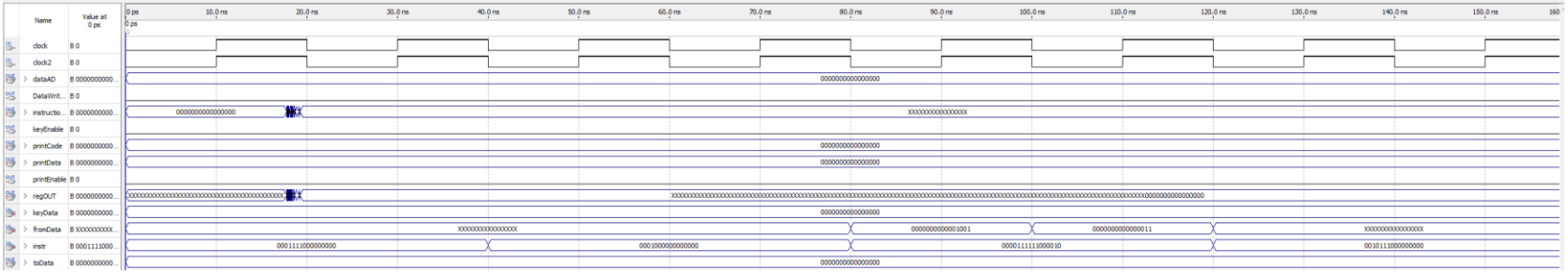
PC Register (Reg16b)



CPU (ADD example)



Functional simulation



Timing simulation

1ο instruction: 0001-111-000-000-000 Φόρτωση στον καταχωρητή 111 την τιμή του fromData (Load Word).
2ο instruction: 0001-000-000-000-000 Φόρτωση στον καταχωρητή 000 την τιμή του fromData (Load Word).
3ο instruction: 0000-111-111-000-010 Πρόσθεση του περιεχομένου των καταχωρητών και με αποτέλεσμα στον καταχωρητή 111 (ADD).
4ο instruction: 0010-111-000-000-000 Αποθήκευση του περιεχομένου του καταχωρητή 111 στη μνήμη (Save Word).

Το αποτέλεσμα του ADD βρίσκεται στο πρώτο πλαίσιο. Το αποτέλεσμα του SW βρίσκεται στο δεύτερο πλαίσιο.

CPU (NOT example)

Functional simulation

Timing Simulation

1ο instruction: 0001-111-000-000-000 Φόρτωσε στον καταχωρητή 000 την τιμή του fromData (Load Word).
2ο instruction: 0000-001-000-000-110 Λογική πράξη NOT στον καταχωρητή 000 και αποθήκευση αποτελέσματος στον 001 (NOT).
3ο instruction: 0010-001-000-000-000 Αποθήκευση του περιεχομένου του καταχωρητή 001 στη μνήμη (Save Word).

Το αποτέλεσμα του NOT βρίσκεται στο πρώτο πλαίσιο. Το αποτέλεσμα του SW βρίσκεται στο δεύτερο πλαίσιο.