

# Diksha Moolchandani

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## Work Experience

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**Researcher (Full-time)**

(Jan. 2022 - present)

*IMEC, Leuven, Belgium*

## Education

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**Ph.D. in Computer Science**

(Jan. 2016 - 2021)

*Indian Institute of Technology Delhi (IIT Delhi)*

*Advisors: Prof. Smruti Ranjan Sarangi and Prof. Anshul Kumar*

**B.Tech. in Electronics and Communication Engineering**

(Aug 2011 - May 2015)

*Indian Institute of Information Technology, Design and Manufacturing, Jabalpur (IIITDM Jabalpur)*

CGPA: 8.6/10

## Research Interests

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- Computer Architecture for Computer Vision
- ML Accelerators
- ML applications in Computer Architecture
- Energy-efficient architecture design for UAVs and autonomous driving vehicles

## Honors & Awards

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- Winner: Technical Blog Competition at IBM Research's flagship event Maitreyee (Sept. 2021)  
*IBM Research*
- Selected to attend the 8th Heidelberg Laureate Forum (Sept. 2021)  
*Heidelberg, Germany*
- Fellowship to attend Robotics: Science and Systems (RSS) (Jul. 2021)  
*virtual event*
- Winner: Technical Blog Competition at IBM Research's flagship event Maitreyee (Oct. 2020)  
*IBM Research*
- Scholarship with short stay: Ph.D. young researcher (Sept.-Nov. 2019)  
*Innopolis University, Russia*

## Publications

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**Game Theory-based Parameter Tuning for Energy-efficient Path Planning on Modern UAVs**  
D. Moolchandani, K. Yadav, G. Prathap, I. Afanasyev, A. Kumar, M. Mazzara, and S.R. Sarangi  
ACM Transactions on Cyber-Physical Systems (under submission)

**Hardware-Assisted Mechanisms to Enforce Control Flow Integrity: A Comprehensive Survey**

S. Kumar, **D. Moolchandani**, and S.R. Sarangi  
Elsevier Journal of Systems Architecture (JSA) 2022 (accepted)

**Performance and Power Prediction for Concurrent Execution on GPUs**

**D. Moolchandani**, A. Kumar, and S.R. Sarangi  
ACM Transactions on Architecture and Code Optimization, 2022

**PredStereo: An Accurate Real-Time Stereo Vision System**

**D. Moolchandani**, N. Shrivastava, A. Kumar, and S.R. Sarangi  
Winter Conference on Applications of Computer Vision (WACV) 2022

**Game Theory-based Parameter-Tuning for Path Planning of UAVs**

**D. Moolchandani**, G. Prathap, I. Afanasyev, A. Kumar, M. Mazzara, and S.R. Sarangi  
International Conference on VLSI Design 2021

**Accelerating CNN Inference on ASICs: A Survey**

**D. Moolchandani**, A. Kumar, and S.R. Sarangi  
Elsevier Journal of Systems Architecture (JSA), Feb. 2021, Vol. 113

**VisSched: An Auction based Scheduler for Vision Workloads on Heterogeneous Processors**

**D. Moolchandani**, A. Kumar, J.F. Martínez, and S.R. Sarangi  
Full paper accepted in ESWEEK CASES 2020  
Published in IEEE International Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Nov. 2020, Vol. 39, Issue 11

**Performance Prediction for Multi-Application Concurrency on GPUs**

**D. Moolchandani**, S. Gupta, A. Kumar, and S.R. Sarangi  
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2020

**A Machine to Machine framework for the charging of Electric Autonomous Vehicles**

Z. Elbanna, I. Afanasyev, L.J.P. Araújo, R. Hussain, M. Khazeev, J. Lamptey, M. Mazzara, S. Megha, **D. Moolchandani**, and D. Strugar  
The Workshops of the IEEE International Conference on Advanced Information Networking and Applications (WAINA) 2020

**F-LaaS: A Control-Flow-Attack Immune License-as-a-Service Model**

S. Kumar, **D. Moolchandani**, T. Ono, and S.R. Sarangi  
IEEE International Conference on Services Computing (SCC) 2019

## Posters

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**Scheduling and Characterization of Computer Vision Workloads on Heterogeneous Systems**

**D. Moolchandani**  
Ph.D. Forum, Design Automation Conference (DAC) 2021

**VisSched: An Auction based Scheduler for Vision Workloads on Heterogeneous Processors**

**D. Moolchandani**, A. Kumar, J.F. Martínez, and S.R. Sarangi  
Design Automation Conference (DAC) 2020

## Patents

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### System and Method for Improving Stereo Vision Accuracy

Diksha Moolchandani, Nivedita Shrivastava, Anshul Kumar, and Smruti R. Sarangi

Filed at the Indian patent office. Date: June 24, 2021. Number: 202111028215

## Research Software

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### Tejas Power Pack

(Aug-Oct 2017)

*Advisor: Prof. Smruti Ranjan Sarangi, IIT Delhi*

- o Power model add-on for Tejas architectural simulator
- o Released under the open source Apache-v2 license [here](#)

## Professional Experience

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- o **Visiting Research Scholar** (Sept.-Nov. 2019)  
*Innopolis University, Republic of Tatarstan, Russia*
- o **Project Associate** (Jun-Dec 2015)  
*IIT Delhi (Top-ranked institute in Computer Science and Engineering in India)*
- o **Project Based Internship** (May-Dec 2014)  
*Bhabha Atomic Research Centre Mumbai (BARC Mumbai)*
- o **Summer Internship** (May-Jul 2013)  
*BARC Mumbai*
- o Summer training in Embedded Systems and Robotics, (May-Jun 2012)  
*BRiCS Simplifix Automation & Solutions Pvt. Ltd., IIT Kanpur*

## Teaching Experience

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- Computer Architecture** (Spring 2020)  
*Instructor: Prof. Preeti Ranjan Panda*
- Accelerator Design for CNNs** (Spring 2020, Fall 2019)  
*Instructor: Prof. Smruti Ranjan Sarangi*
- Operating Systems** (Spring 2019)  
*Instructor: Prof. Smruti Ranjan Sarangi*
- Advanced Computer Architecture** (Fall 2018)  
*Instructor: Prof. Smruti Ranjan Sarangi*
- Computer Architecture** (Spring 2018, Spring 2017)  
*Instructor: Prof. Anshul Kumar*
- Digital Logic and System Design** (Fall 2017, Fall 2016)  
*Instructor: Prof. Anshul Kumar*

## Student Mentoring

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- Kishore Yadav (Master's thesis)** 2020-2021  
*Unity-based simulator for drone swarms*

<b>Mohammad Atif (Bachelor's thesis)</b> <i>Self-driving simulator: lane change, steering, and braking</i>	2020-2021
<b>Satyam Jay (Master's project)</b> <i>Self-driving simulator: lane change, steering, and braking</i>	2020-2021
<b>Kishore Yadav, Yash Malviya, Aniket Kumar (Master's project)</b> <i>Self-driving simulator - detection, tracking, localization</i>	2019-2020
<b>Yash Singla, Pranay Singh, Mudit Soni (Winter Internship)</b> <i>Added scenes and features to our self-driving car simulator</i>	2019
<b>Chinmay Rai (Bachelor's thesis)</b> <i>Compiler for Tejas-CNN</i>	2019-2020
<b>Aditya Jain, Sarthak Vishnoi (Bachelor's thesis)</b> <i>Added multiple dataflows and DRAM module to Tejas-CNN</i>	2019-2020
<b>Shivangi Sharma, Ravi Prakash, Goverdhan Mishra (Summer Internship)</b> <i>Tejas-CNN: Simulator for CNN accelerators (basic implementation)</i>	2019
<b>Prabhleen Kaur (Master's thesis)</b> <i>Unity-based simulator for self-driving cars (basic)</i>	2018-2019
<b>Sudhanshu Gupta (Bachelor's thesis)</b> <i>Characterization of autonomous driving workloads</i>	2018-2019
<b>Rishabh Singh, Parul Gupta (Summer Internship)</b> <i>Generic plotting library for the statistics generated by Tejas architectural simulator</i>	2018
<b>Dhruv Mishra (Summer Internship)</b> <i>Analyzed MEVBench suite for invariants using Daikon</i>	2018
<b>Ryan Dsouza (Bachelor's thesis)</b> <i>Extended Tejas x86 architectural simulator for SIMD instructions</i>	2017-2018

## Talks & Seminars

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- o Scheduling and Characterization of Computer Vision Workloads on Heterogeneous Systems *virtually at DAC Ph.D. Forum (Dec. 2021)*
- o Game Theory-based Parameter-Tuning for Path Planning of UAV *virtually at IBM Research's flagship event Maitreyee (Sept. 2021)*
- o VisSched: An Auction-based Scheduler for Vision Workloads on Heterogeneous Processors *virtually at AMD Bangalore (Sept. 2021)*
- o Accelerating CNN Inference on ASICs: A Survey *virtually at Qualcomm Hyderabad (Sept. 2021)*
- o VisSched: An Auction-based Scheduler for Vision Workloads on Heterogeneous Processors *virtually at IMEC Belgium (July 2021)*
- o Game Theory-based Parameter-Tuning for Path Planning of UAV *virtually at VLSI Design (Feb. 2021)*
- o VisSched: An Auction-based Scheduler for Vision Workloads on Heterogeneous Processors *virtually at IBM Research's flagship event Maitreyee (Oct. 2020)*
- o VisSched: An Auction-based Scheduler for Vision Workloads on Heterogeneous Processors *virtually at ESWEK CASES (Sep. 2020)*

- Performance Prediction for Multi-Application Concurrency on GPUs  
*virtually at ISPASS (Aug. 2020)*
- VisSched: An Auction-based Scheduler for Vision Workloads on Heterogeneous Processors  
*virtually at DAC (July 2020)*
- Benchmark Characterization and Optimizations for Path Planning of Drones  
*Innopolis University, Russia (Nov. 2019)*
- Architectural Characterization of Vision Workloads  
*Innopolis University, Russia (Sept. 2019)*
- Architectures for Vision and Image Processing Applications  
*PhD Symposium CSE IIT Delhi (Dec. 2017)*
- Architectures for Vision and Image Processing Applications: Survey and Research Proposal  
*IIT Delhi, India (Jun. 2017)*
- Implementation of FPGA based Communication Network using High Speed PCIe and Multi Gigabit Transceivers  
*National Workshop on Cryptology (NWC), 2014*
- Implementation of FPGA based Communication Network using High Speed PCIe and Multi Gigabit Transceivers  
*Bhabha Atomic Research Center Mumbai (Aug. 2014)*

## Professional Service

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- Reviewer for JSA Journal, ICCD 2021, ICPP 2021, HPCA 2021, ICPP 2020, HiPC 2020, VDAT 2020, ICCD 2019, *EMC<sup>2</sup>* 2018, IPDPS 2018, ICCD 2017
- PC member Nonlinearity, Information, and Robotics 2021

## Past Selected Projects

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### **Super Resolution Imaging on Reconfigurable Arrays, IIT Delhi** (Jun 2015-May 2016)

*Advisors: Prof. Kolin Paul and Prof. Anshul Kumar, IIT Delhi*

- Implemented a Convolutional Neural Network on a Virtex-6 FPGA to convert an SD video to an HD video at real time.
- Optimizations include computation time reduction by exploiting inherent parallelism, efficient matrix multiplication by using Toeplitz representation and memory footprint reduction by using a rotating buffer instead of a full-size input buffer.
- Designed a self-defined protocol, partially exploiting the OCP protocol, to fetch image data in parallel from four DDR3 banks.

### **FPGA Cluster based Parallel Architecture for Cryptanalysis, BARC Mumbai**

*Advisor: Mr. Abhishek Bajpai, BARC Mumbai* (May-Nov 2014)

- Developed a network of four Virtex-6 FPGAs that communicated via the MGT protocol.
- Developed Python and C wrappers for PCIe bus drivers to implement DMA from Linux Kernel Memory to FPGA BRAM space
- Presented paper at National Workshop on Cryptology 2014 (NWC).

## Course Projects

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- Implemented a distributed ledger of transactions using Google GO, IIT Delhi

- o Designed a resource-constrained scheduling algorithm to maximize the performance in a system with multi-port memories, IIT Delhi
- o Compared the impact of uniform and non-uniform caches on the performance of the processor, IIT Delhi
- o Designed and fabricated a hand-held device to aid in sending flood alerts to the people and rescue location to the rescue team, IIITDM Jabalpur