Diksha Moolchandani

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Education

Ph.D. in Computer Science (2016 - Present)
Indian Institute of Technology Delhi (IIT Delhi)
Advisors: Prof. Smruti Ranjan Sarangi and Prof. Anshul Kumar
CGPA: 8.8/10

B.Tech. in Electronics and Communication Engineering (Aug 2011 - May 2015)
Indian Institute of Information Technology, Design and Manufacturing, Jabalpur (IIITDM Jabalpur)
CGPA: 8.6/10

Work Experience

- **Scholarship with short stay: Ph.D. young researcher** (Sept.-Nov. 2019)
  Innopolis University, Republic of Tatarstan, Russia
- **Project Associate** (Jun-Dec 2015)
  IIT Delhi (Top-ranked institute in Computer Science and Engineering in India)
- **Project Based Internship** (May-Dec 2014)
  Bhabha Atomic Research Centre Mumbai (BARC Mumbai)
- **Summer Internship** (May-Jul 2013)
  BARC Mumbai
- Summer training in Embedded Systems and Robotics, (May-Jun 2012)
  BRiCS Simplifix Automation & Solutions Pvt. Ltd., IIT Kanpur

Publications

VisSched: An Auction based Scheduler for Vision Workloads on Heterogeneous Processors
D. Moolchandani, A. Kumar, J.F. Martínez, S.R. Sarangi
International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2020 (full paper accepted)
Design Automation Conference (DAC), 2020 (accepted as a poster)

Performance Prediction for Multi-Application Concurrency on GPUs
D. Moolchandani, S. Gupta, A. Kumar, S.R. Sarangi
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2020

A Machine to Machine framework for the charging of Electric Autonomous Vehicles
Z. Elbanna, I. Afanasyev, L.J.P. Araújo, R. Hussain, M. Khazeev, J. Lamptey, M. Mazzara, S. Megha, **D. Moolchandani**, and D. Strugar
The Workshops of the IEEE International Conference on Advanced Information Networking and Applications (WAINA), 2020

F-LaaS: A Control-Flow-Attack Immune License-as-a-Service Model
S. Kumar, **D. Moolchandani**, T. Ono, and S.R. Sarangi
IEEE International Conference on Services Computing (SCC), 2019

Talks & Seminars

- Benchmark Characterization and Optimizations for Path Planning of Drones at Innopolis University, Russia (Nov. 2019)
- Architectural Characterization of Vision Workloads at Innopolis University, Russia (Sept. 2019)
- Architectures for Vision and Image Processing Applications at PhD Symposium CSE IIT Delhi (Dec. 2017)
- Architectures for Vision and Image Processing Applications: Survey and Research Proposal at IIT Delhi, India (Jun. 2017)
- Implementation of FPGA based Communication Network using High Speed PCIe and Multi Gigabit Transceivers at National Workshop on Cryptology (NWC), 2014
- Implementation of FPGA based Communication Network using High Speed PCIe and Multi Gigabit Transceivers at BARC Mumbai (Aug. 2014)

Honors & Awards

- Invited to attend the Heidelberg Laureate Forum (virtually in Sept. 2020 & physically in Sept. 2021)
  Heidelberg, Germany
- Scholarship with short stay: Ph.D. young researcher (Sept.-Nov. 2019)
  Innopolis University, Russia

Research Software

Tejas Power Pack (Aug-Oct 2017)
Advisor: Prof. Smruti Ranjan Sarangi, IIT Delhi

- Power model add-on for Tejas architectural simulator
- Released under the open source Apache-v2 license here

Selected Projects

Super Resolution Imaging on Reconfigurable Arrays, IIT Delhi (Jun 2015-May 2016)
Advisors: Prof. Kolin Paul and Prof. Anshul Kumar, IIT Delhi

- Implemented a Convolutional Neural Network on a Virtex-6 FPGA to convert an SD video to an HD video at real time.
- Optimizations include computation time reduction by exploiting inherent parallelism, efficient matrix multiplication by using Toeplitz representation and memory footprint reduction by using a rotating buffer instead of a full-size input buffer.
- Designed a self-defined protocol, partially exploiting the OCP protocol, to fetch image data in parallel from four DDR3 banks.

FPGA Cluster based Parallel Architecture for Cryptanalysis, BARC Mumbai
Advisor: Mr. Abhishek Bajpai, BARC Mumbai (May-Nov 2014)

- Developed a network of four Virtex-6 FPGAs that communicated via the MGT protocol.
- Developed Python and C wrappers for PCIe bus drivers to implement DMA from Linux Kernel Memory to FPGA BRAM space
- Presented paper at National Workshop on Cryptology 2014 (NWC).

Course Projects

- Implemented a distributed ledger of transactions using Google GO, IIT Delhi
- Designed a resource-constrained scheduling algorithm to maximize the performance in a system with multi-port memories, IIT Delhi
- Compared the impact of uniform and non-uniform caches on the performance of the processor, IIT Delhi
- Designed and fabricated a hand-held device to aid in sending flood alerts to the people and rescue location to the rescue team, IIITDM Jabalpur

Hobbies

Yoga, Meditation, Badminton