Diksha Moolchandani

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EDUCATION

Ph.D. in Computer Science

(2016 - Present)

Indian Institute of Technology Delhi (IIT Delhi)

Advisors: Prof. Smruti Ranjan Sarangi and Prof. Anshul Kumar

CGPA: 8.8/10

B.Tech. in Electronics and Communication Engineering

(Aug 2011 - May 2015)

 $Indian\ Institute\ of\ Information\ Technology,\ Design\ and\ Manufacturing,\ Jabalpur\ (IIITDM\ Jabalpur)$

CGPA: 8.6/10

Work Experience

\bullet Scholarship with short stay: Ph.D. young researcher

(Sep-Nov 2019)

Innopolis University, Republic of Tatarstan, Russia

• Project Associate

(Jun-Dec 2015)

IIT Delhi (Top-ranked institute in Computer Science and Engineering in India)

• Project Based Internship

(May-Dec 2014)

Bhabha Atomic Research Centre Mumbai (BARC Mumbai)

• Summer Internship

(May-Jul 2013)

 $BARC\ Mumbai$

 \bullet Summer training in Embedded Systems and Robotics,

(May-Jun 2012)

BRiCS Simplifix Automation & Solutions Pvt. Ltd., IIT Kanpur

RESEARCH SOFTWARE

Tejas Power Pack

(Aug-Oct 2017)

Advisor: Prof. Smruti Ranjan Sarangi, IIT Delhi

- Power model add-on for Tejas architectural simulator
- Released under the open source Apache-v2 license here

PUBLICATIONS

Performance Prediction for Multi-Application Concurrency on GPUs

D. Moolchandani, S. Gupta, A. Kumar, S.R. Sarangi

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Boston, USA, April 2020

A Machine to Machine framework for the charging of Electric Autonomous Vehicles

Z. Elbanna, I. Afanasyev, L.J.P. Araújo, R. Hussain, M. Khazeev, J. Lamptey, M. Mazzara, S. Megha, **D. Moolchandani**, and D. Strugar

The Workshops of the IEEE International Conference on Advanced Information Networking and Applications (WAINA), Caserta, Italy, April 2020

F-LaaS: A Control-Flow-Attack Immune License-as-a-Service Model

S. Kumar, D. Moolchandani, T. Ono, and S.R. Sarangi

IEEE International Conference on Services Computing (SCC), Milan, Italy, July 2019

Selected Projects

Super Resolution Imaging on Reconfigurable Arrays, IIT Delhi

(Jun 2015-May 2016)

Advisors: Prof. Kolin Paul and Prof. Anshul Kumar, IIT Delhi

- Implemented a Convolutional Neural Network on a Virtex-6 FPGA to convert an SD video to an HD video at real time.
- Optimizations include computation time reduction by exploiting inherent parallelism, efficient matrix multiplication by using Toeplitz representation and memory footprint reduction by using a rotating buffer instead of a full-size input buffer.
- Designed a self-defined protocol, partially exploiting the OCP protocol, to fetch image data in parallel from four DDR3 banks.

FPGA Cluster based Parallel Architecture for Cryptanalysis, BARC Mumbai

Advisor: Mr. Abhishek Bajpai, BARC Mumbai

(May-Nov 2014)

- Developed a network of four Virtex-6 FPGAs that communicated via the MGT protocol.
- Developed Python and C wrappers for PCIe bus drivers to implement DMA from Linux Kernel Memory to FPGA BRAM space
- Presented paper at National Workshop on Cryptology 2014 (NWC).

Course Projects

- Implemented a distributed ledger of transactions using Google GO, IIT Delhi
- Designed a resource-constrained scheduling algorithm to maximize the performance in a system with multi-port memories, IIT Delhi
- Compared the impact of uniform and non-uniform caches on the performance of the processor, IIT Delhi
- Designed and fabricated a hand-held device to aid in sending flood alerts to the people and rescue location to the rescue team, IIITDM Jabalpur

Hobbies

Yoga, Meditation, Badminton