UNIVERSITY OF COLOMBO, SRI LANKA

UNIVERSITY OF COLOMBO SCHOOL OF COMPUTING

BACHELOR OF COMPUER SCIENCE

Academic Year 2012/2013 – First Year Examination – Semester I – 2013

IS1002 – Computer Systems

TWO (2) HOURS

To be completed by the candidate

Examination Index No: .....

Important Instructions to candidates:

1. The medium of instruction and questions is **English**.
2. If a page or a part of this question paper is not printed, please inform the supervisor immediately.
3. Note that questions appear on both sides of the paper. If a page is not printed, please inform the supervisor immediately.
4. Write your index number in each and every page of the question paper.
5. This paper has **4** questions and **14** pages.
6. Answer **ALL** questions. All questions carry equal marks (**25** marks).
7. Any electronic device capable of storing and retrieving text including electronic dictionaries and mobile phones are not allowed.
8. Non-programmable calculators are allowed.

For Examiner's use only	
Question No	**Marks**
1	
2	
3	
4	
Total	

1. (a) Convert the number **+127.9375** from decimal into **16-bit floating point representation.** Assume 10 bits for the mantissa and 5 bits for the exponent.

[7 Marks]

$+127.9375 = 1111111.1111_b$

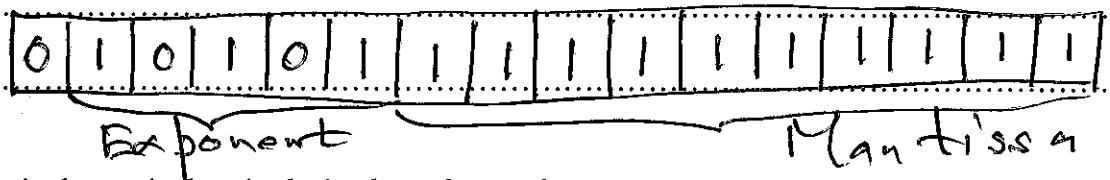
$= 1.1111111111 \times 2^6$

$N = 1$ $S = 1$

$k = 2^{N-1} - 1 = 2^5 - 1 = 15$

$\therefore$ Exponent $= 15 + 6 = 21$

Answer is



(b) What is the equivalent in decimal number to the **16-bit floating point representation** of the **1 10100 1111111111**. Assume 10 bits for the mantissa and 5 bits for the exponent.

[6 Marks]

Exponent $= 10100 = 20$

$k = 15$

$\therefore$ Actual Exponent $= 20 - 15 = 5$

Answer is $= -1.1111111111 \times 2^5$

$= -111111.11111$

$= -63.96875$

(c) What is the equivalent in decimal number to the **32-bit floating point representation** of the **0 10000011 10111000000000000000000**.

[6 Marks]

8-1

$k = 2^{8-1} - 1 = 127$

∴ Exponent = 131 − 127 = 4

+4

∴ Answer is = + 1.10111 × 2

= + 11011.1

= + 27.5

(d) Convert the number **-43.75** from decimal into **32-bit floating point representation.**

[6 Marks]

− 43.75 = − 101011.11

+5

= − 1.0101111 × 2

∴ Exponent = 127 + 5 = 132

∴ Answer is

1	1	0	0	0	0	1	0	0	0	1	0	1	1	1	1	1	0	0	0

Exponent Mantissa

2. An assembly line has 3 failsafe sensors and one emergency shutdown switch. The line should keep moving unless any of the following conditions arises:

- If the emergency switch is pressed, the system shuts down.
- If sensor 1 and sensor 2 are activated at the same time, the system shuts down.
- If sensor 2 and sensor 3 are activated at the same time, the system shuts down.
- If sensor 1 and sensor 3 are activated at the same time, the system shuts down.
- If all three sensors are activated at the same time, the system shuts down.

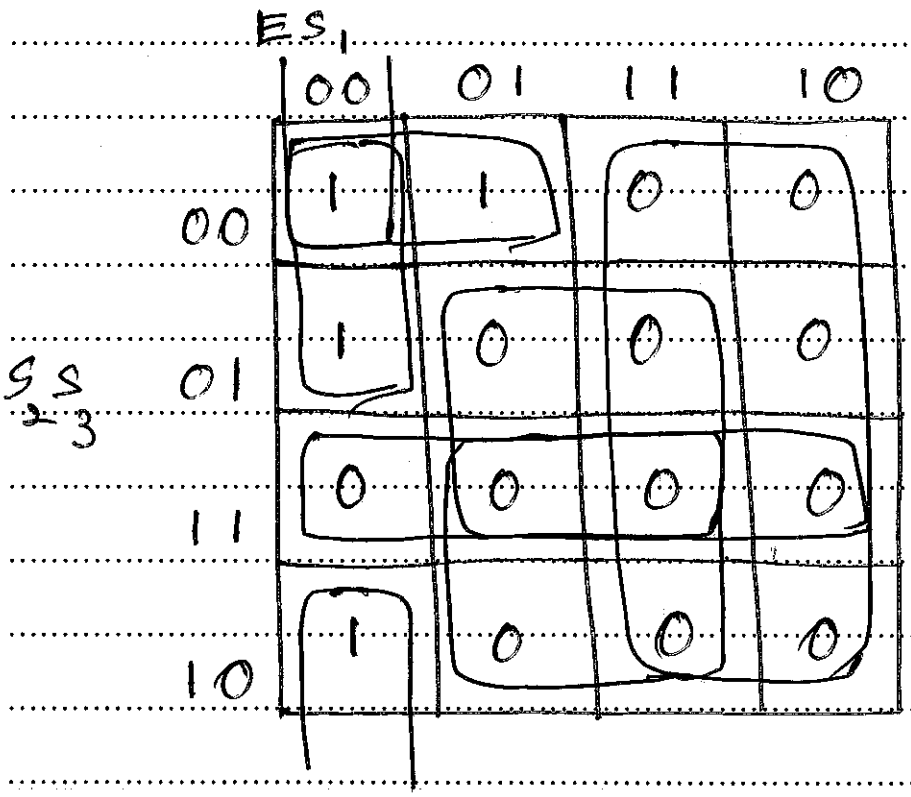
Assume that ***Logic one*** is for an activated switch, ***logic one*** for an activated sensor and output of the circuit should be ***logic one*** to run the assembly line.

(a) Provide the **truth table** for the above system. **[8 Marks]**

E	S_1	S_2	S_3	$f(E S_1 S_2 S_3)$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(b) Get the simplified **Sum of Products** (SOP) and **Product of Sums** (POS) expression that represents the logic function of the above system in (a).

[7 Marks]



Sum of products = $\bar{E}\bar{S}_2\bar{S}_3 + \bar{E}S_1\bar{S}_2 + \bar{E}\bar{S}_1S_3$

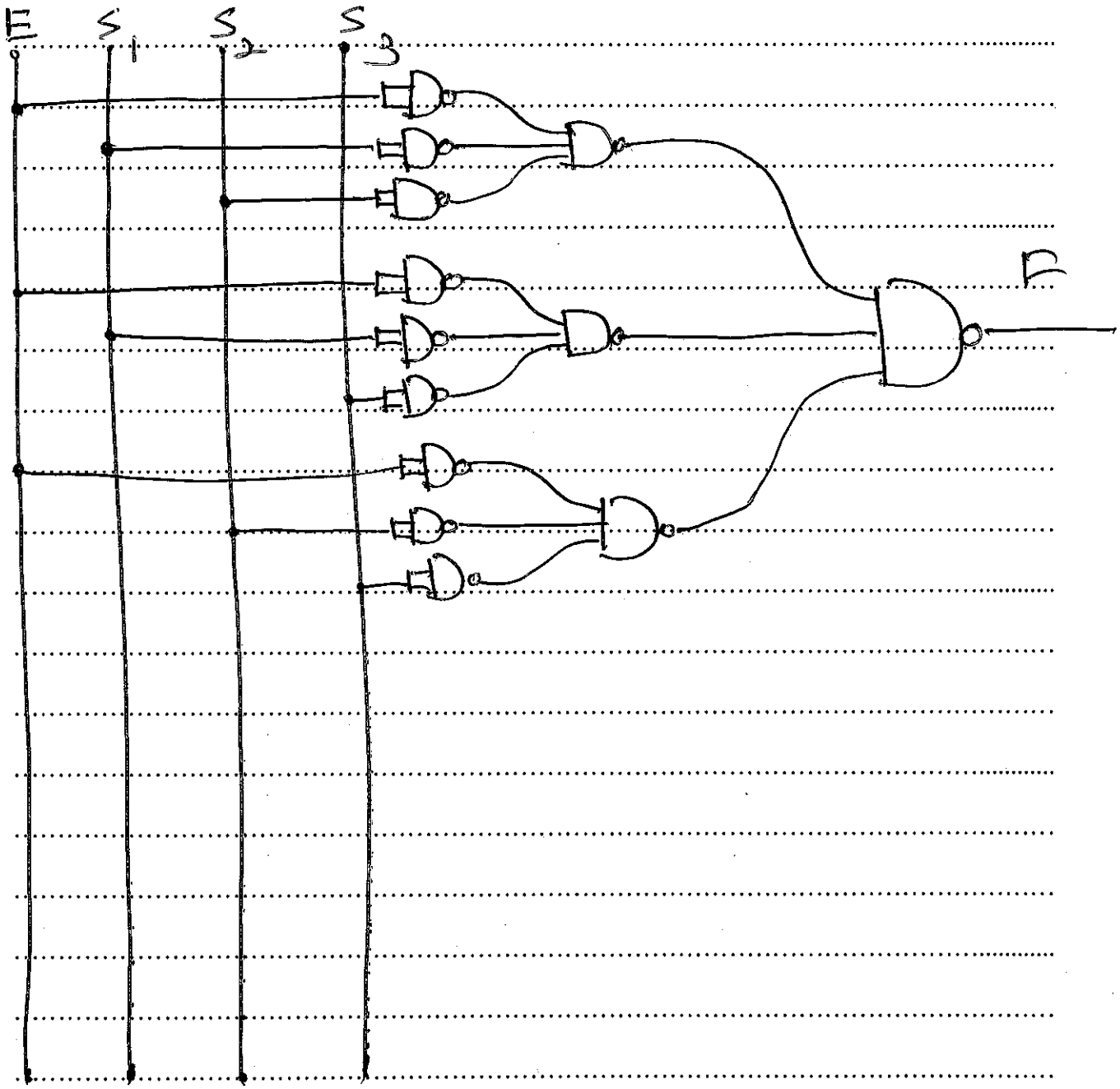
Product of Sums = $(\bar{E}) \cdot (S_2 + \bar{S}_3) \cdot (\bar{S}_1 + S_3) \cdot (\bar{S}_1 + \bar{S}_2)$

(c) Design the logic circuit for the above **SOP** expression in (**b**) using only **NAND** gates. Clearly indicate the method and steps.

[5 Marks]

$$\overline{E}\,\overline{S}_1\overline{S}_2 + \overline{E}\,\overline{S}_1\overline{S}_3 + \overline{E}\,\overline{S}_2\overline{S}_3$$

$$= \overline{\left(\overline{E}\,\overline{S}_1\overline{S}_2\right)} \cdot \overline{\left(\overline{E}\,\overline{S}_1\overline{S}_3\right)} \cdot \overline{\left(\overline{E}\,\overline{S}_2\overline{S}_3\right)}$$

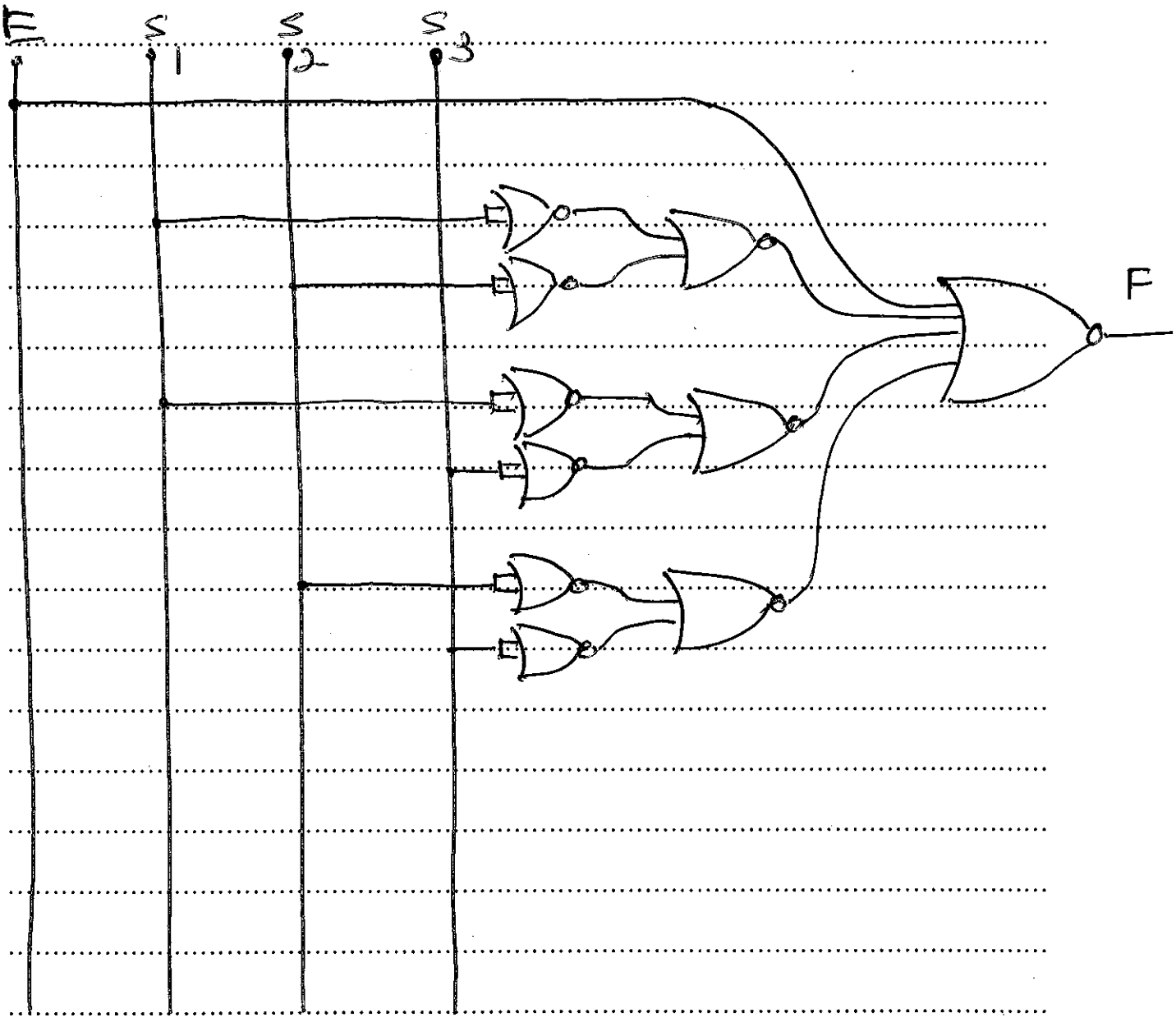


(d) Design the logic circuit for the above **POS** expression in **(b)** using only **NOR** gates. Clearly indicate the method and steps.

[5 Marks]

$$= (\overline{E}) \cdot (\overline{S_1} + \overline{S_2}) \cdot (\overline{S_1} + \overline{S_3}) \cdot (\overline{S_2} + \overline{S_3})$$

$$= \overline{(E)} + \overline{(\overline{S_1} + \overline{S_2})} + \overline{(\overline{S_1} + \overline{S_3})} + \overline{(\overline{S_2} + \overline{S_3})}$$



3. **(a)** Briefly explain about each of the following components of the CPU. Clearly state the task(s) they perform.

(i) Arithmetic Logic Unit (ALU)

[2 Marks]

• Carries out logical and arithmetic operations

(ii) Registers

[2 Marks]

• Hold data that can be readily accessed by CPU

(iii) Program Counter (PC)

[2 Marks]

• Hold the memory address of currently executing instruction. Increment by word size at the end of each instruction.

(iv) Instruction Register (IR)

[2 Marks]

• Hold the currently executing instruction

(v) Address Bus

[2 Marks]

• Pass the address to fetch memory address of data or instruction.

(b) Consider the arithmetic expression **r = (a * b * c) / a** . Generate the instructions required to evaluate this expression in the following three architectures.

(i) Accumulator Architecture (One Operand).

[2 Marks]

Load a
Mult b
Mult c
Div a
Store r

(ii) Stack Architecture.

[2 Marks]

```
Push  a
Push  a
Push  b
Multiply
Push  c
Multiply
Div
Pop   v
```

(iii) General Purpose Register Architecture.

[2 Marks]

```
Load  R1  a
Load  R2  b
Load  R3  c
Add   R4  R1  R2
Add   R5  R3  R4
Div   R0  R5  R1
Store R0  v
```

(c) Consider a machine with instruction format of the form **opcode R M** where **R** is a register address and **M** is a memory address. Instructions are 16 bits long and one of the instruction formats provides 4 bits for the op-code, 4 bits for the register and other 8 bits for the memory address of the operand. Assume that the word size of this machine is 8 bits (byte addressable).

Some of the op-codes of the above (a) processor is given below:

0001 – L R, A	**LOAD** the register **R** with the content of memory cell **A**
0010 – LI R, I	**LOAD** the register **R** with the value **I**

0011 – ST R, A	**STORE** the content of the register **R** to the memory cell whose address is **A**
0101 – ADD R0, R1, R2	**ADD** the numbers in registers **R1** and **R2** and place the result in register **R0**
1001 - XOR R0, R1, R2	**XOR** the bit patterns in **R1** and **R2** and place the result in **R0**
1000 - AND R0, R1, R2	**AND** the bit patterns in **R1** and **R2** and place the result in **R0**
1110 – JMP R, A	**JUMP t**o the instruction located in the memory cell **A** if the bit pattern in **R** is equal to the one in **R0**
1111 - HALT	**HALT** the execution

Write down the machine code instructions sequence to execute the following program statements.

```
A = 33 ;
B = 55 ;
C = B - A ;
```

Assume that **A** and **B** are variables refer the memory addresses **80**, **81** and the initial program counter (PC) as hexadecimal **30**.

[9 Marks]

LI R1 21 } A = 33 ;
Store R1 80
LI R1 37 } B = 55 ;
Store R2 81

LI R3 FF
XOR R4 R1 R3
LI R3 01
Add R1 R3 R4 } C = B - A ;
Add R3 R1 R2
Store R3 82

4. **(a)** Random Access Memory (RAM) is a volatile, read and write memory. Write down two (2) types of RAM.

[4 Marks]

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(b) Answer the following questions by indicating whether they are **true** or **false**. Mark your choice with a √.

[6 Marks]

	True	**False**
Solid Sate Drives (SSD) use less power compared to Hard Disk Drives (HDD).		
In a 2-level cache implementation, L1 cache has more space than L2 cache.		
Both Instructions and data are stored in the cache.		

(c) For a Simple cache model, find the **Effective Access Time (EAT)** in Nano seconds (**ns**) for the following situation: cache hit rate is **80%**, cache access time is **10 ns** and memory access time is **10 µs**.

[5 Marks]

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(d) What is the Low Order Address Bits (LOAB) in hexadecimal of the memory address **0xCAFE844** if the cache has 256 cache lines?

[5 Marks]

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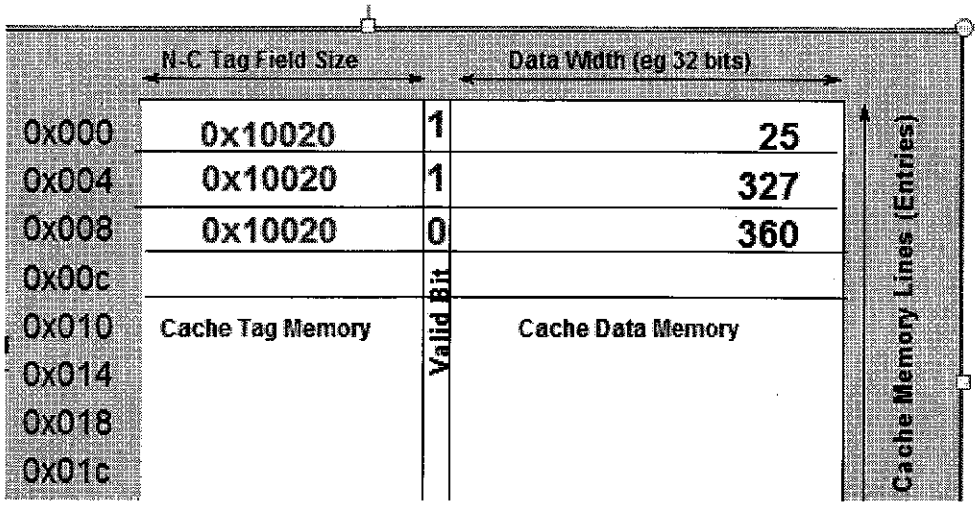
(e) Consider the diagram below.

(i) Assume that a particular program refers into the address denoted by **0x10020008** from the cache. What is the value represented by that location?

(ii) Assume that the CPU wants to write the value 540 into the address denoted by **0x10020004**. What would happen, if the cache management uses write-back policy? Explain your answer.

[5 Marks]



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