1)

State	Highway Output	Farm Road Output	Delay	Delay
S0	Red	Red	1	50,000,000
S1	Green	Red	31	1,500,000,000
S2	Yellow	Red	3	150,000,000
S3	Red	Red	1	50,000,000
S4	Red	Green	15	750,000,000
S5	red	yellow	3	150,000,000

2)

Min = 0, Max = 30, Therefore we need 0 to 30, 30 takes 5 bits to create 1110, n = 5

```
`timescale 1ns/1ps
//default_nettype none;

module tlc_fsm(
    output reg [3:0] state,
    output reg RstCount,
    output reg [1:0] highwaySignal, farmSignal,
    input wire [n-1:0] Count,
    input wire Clk, Rst);

    reg [2:0] nextState; // declare internal nets

    // parameters for easy understanding
    parameter S0 = 3'b000,
              S1 = 3'b001,
              S2 = 3'b010,
              S3 = 3'b011;
              S4 = 3'b100;
              S5 = 3'b101;
              Srst = 3'b110;

    parameter red = 2'b00,
              yellow = 2b'01,
              green = 2b'10;

    reg [3:0] state;
    reg [3:0] nextState;

    always@(state)
        case(state)
            Srst: begin
                highwaySignal = red;
                farmSignal = red;
                RstCount = 1;
            end
            S0: begin
                highwaySignal = red;
                farmSignal = red;
                if(Count == 1 && RstCount == 1)
                    nextState = S1;
                else
                    nextState = S0;
            end
            S1: begin
                highwaySignal = green;
                farmSignal = red;
                if(Count == 1 && RstCount == 1)
                    nextState = S2;
                else
                    nextState = S1;
            end
            S2: begin
                highwaySignal = yellow;
                farmSignal = red;
                if(Count == 1 && RstCount == 1)
                    nextState = S3;
                else
                    nextState = S3;
            end
            S3: begin
                highwaySignal = red;
                farmSignal = green;
                if(Count == 1 && RstCount == 1)
                    nextState = S4;
                else
                    nextState = S3;
            end
            S4: begin
                highwaySignal = red;
                farmSignal = green;
                if(Count == 1 && RstCount == 1)
                    nextState = S5;
                else
                    nextState = S4;
            end
            S5: begin
                highwaySignal = red;
                farmSignal = yellow;
                if(Count == 1 && RstCount == 1)
                    nextState = S0;
                else
                    nextState = S5;
            end
        endcase

    always@(posedge Clk)
        if(RstCount)
            state <= S0; // reset state
        else
            state <= nextState; // set next state

endmodule
```