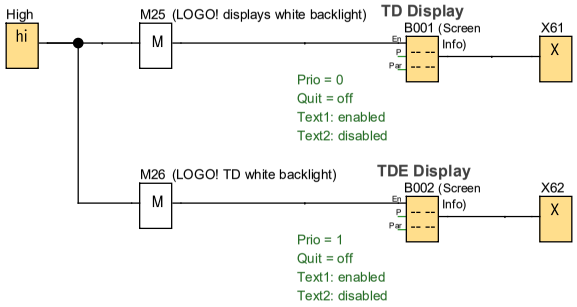
SCREEN CONTROL

==========



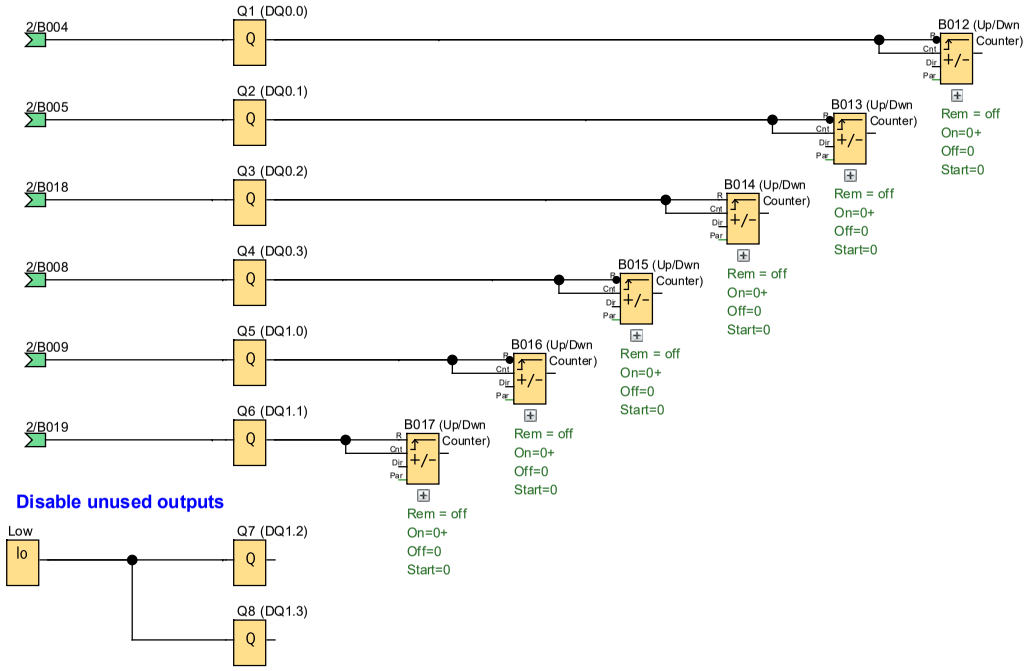
Web Info:
http://192.168.0.100
user password: TVETuser
admin password: TVETadmin

I/O Mapping:
S1 ---> IN1
S2 ---> IN2
S3 ---> IN3
S4 ---> IN4
S5 ---> IN5
S6 ---> IN6
S7 ---> IN7
S8 ---> IN8

Project Summary:
Demonstration of the available AND gates on a LOGO!
Wire the Input Actuators (S1-8) to the corresponding numbers of the LOGO! inputs (IN1-8).
Up/Down counters are used to display values on the TDE Display.

OUTPUT CONTROL

==========



AND Gates:
- Inputs 1 & 2 are required to energize Output1.
Switch Inputs 1 & 2 to various positions and observe Output 1's counter behaviour.
Complete the 2-input AND Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

- Inputs 3, 4 & 5 are required to energize Output2 (note the inverted AND-block input).
Switch Inputs 3, 4 & 5 to various positions and observe Output 2's counter behaviour.
Complete the 3-input AND Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

AND-Edge Gate:
- Inputs 6 & 7, with Input 8 are required to energize Output3.
Switch Inputs 6, 7 & 8 to various positions and observe Output 3's counter behaviour.
Complete the AND-Edge Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

NAND Gates:
- Inputs 1 & 2 are required to energize Output4.
Switch Inputs 1 & 2 to various positions and observe Output 4's counter behaviour.
Complete the 2-input NAND Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

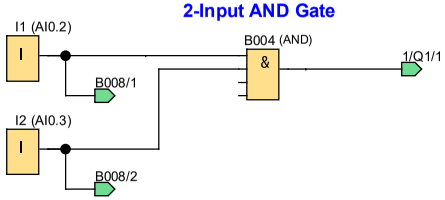
- Inputs 3, 4 & 5 are required to energize Output5 (note the inverted NAND-block input).
Switch Inputs 3, 4 & 5 to various positions and observe Output 5's behaviour.
Complete the 3-input NAND Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

NAND-Edge Gate:
- Inputs 6 & 7, with Input 8 are required to energize Output6.
Switch Inputs 6, 7 & 8 to various positions and observe Output 6's counter behaviour.
Complete the NAND-Edge Gate Truth Table and identify the control bit
Q: what bit is controlling the output?

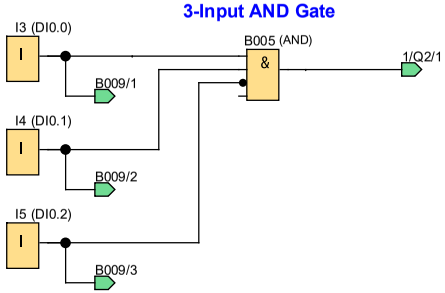
AND GATE LOGIC

==========

2-Input AND Gate

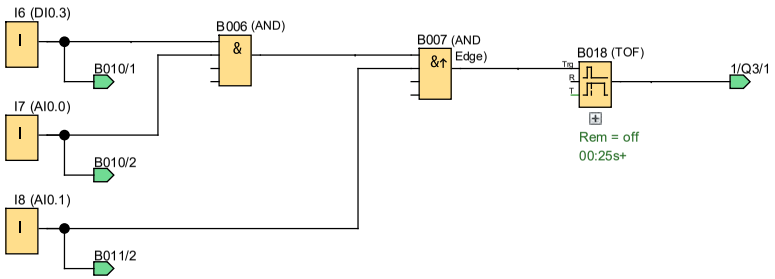


3-Input AND Gate



AND-EDGE GATE LOGIC

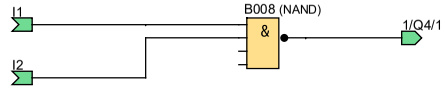
==========



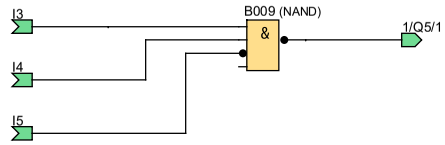
NAND GATE LOGIC

==========

2-Input NAND Gate

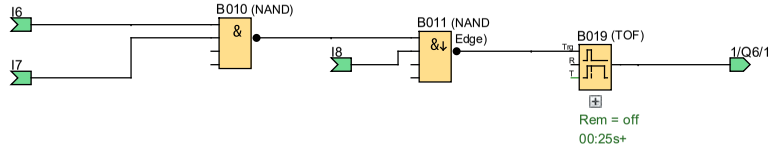


3-Input NAND Gate

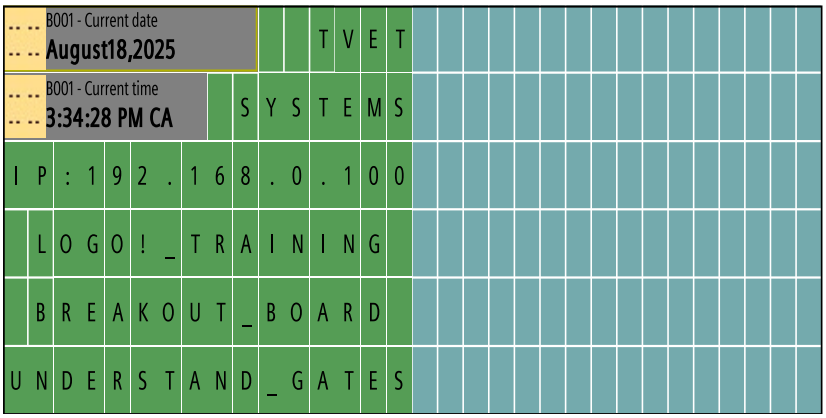
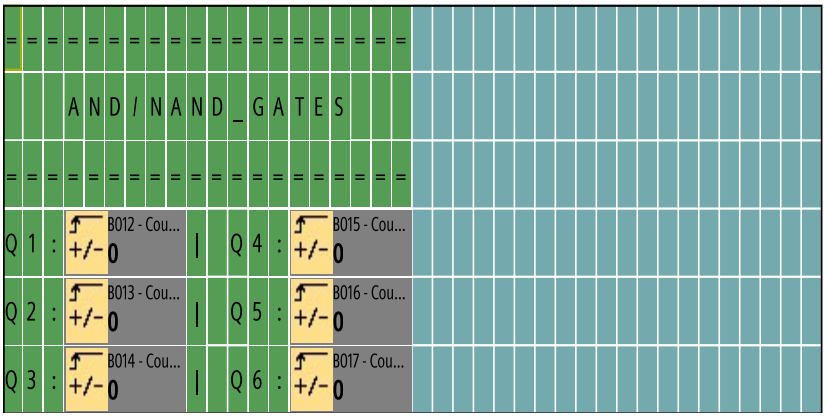


NAND-EDGE GATE LOGIC

==========



Creator:	Admin		Project:		Customer:		
Checked:			Installation:		Diagram No.:		
Date:	7/25/25 9:58 AM/8/18/25 3:34 PM		File:		Page:	2 / 5	

Block Number (Type)	Parameter
B001(Message texts) : (Screen Info)	Prio = 0 Quit = off Text1: enabled Text2: disabled
 Line1.1 B001-Date Line2.1 B001-Time	--> Ticker setting - CBC - Line1: N - Line2: N - Line3: N - Line4: N - Line5: N - Line6: N Message Destination - LOGO! Display
B002(Message texts) : (Screen Info)	Prio = 1 Quit = off Text1: enabled Text2: disabled
 Line4.4 B012-Cnt Line4.15 B015-Cnt Line5.4 B013-Cnt Line5.15 B016-Cnt Line6.4 B014-Cnt Line6.15 B017-Cnt	--> Ticker setting - CBC - Line1: N - Line2: N - Line3: N - Line4: N - Line5: N - Line6: N Message Destination - LOGO! TD
B004(AND) : (AND)	
B005(AND) : (AND)	
B006(AND) : (AND)	
B007(AND (Edge)) : (AND Edge)	
B008(NAND) : (NAND)	

Block Number (Type)	Parameter
B009(NAND) : (NAND)	
B010(NAND) : (NAND)	
B011(NAND (Edge)) : (NAND Edge)	
B012(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B013(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B014(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B015(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B016(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B017(Up/Down counter) : (Up/Dwn Counter)	Rem = off On=0+ Off=0 Start=0
B018(Off-Delay) : (TOF)	Rem = off 00:25s+
B019(Off-Delay) : (TOF)	Rem = off 00:25s+

Connection	Label
I1	AI0.2
I2	AI0.3
I3	DI0.0
I4	DI0.1
I5	DI0.2
I6	DI0.3
I7	AI0.0
I8	AI0.1
M25	LOGO! displays white backlight
M26	LOGO! TD white backlight
Q1	DQ0.0
Q2	DQ0.1
Q3	DQ0.2
Q4	DQ0.3
Q5	DQ1.0
Q6	DQ1.1
Q7	DQ1.2
Q8	DQ1.3
X61	
X62	