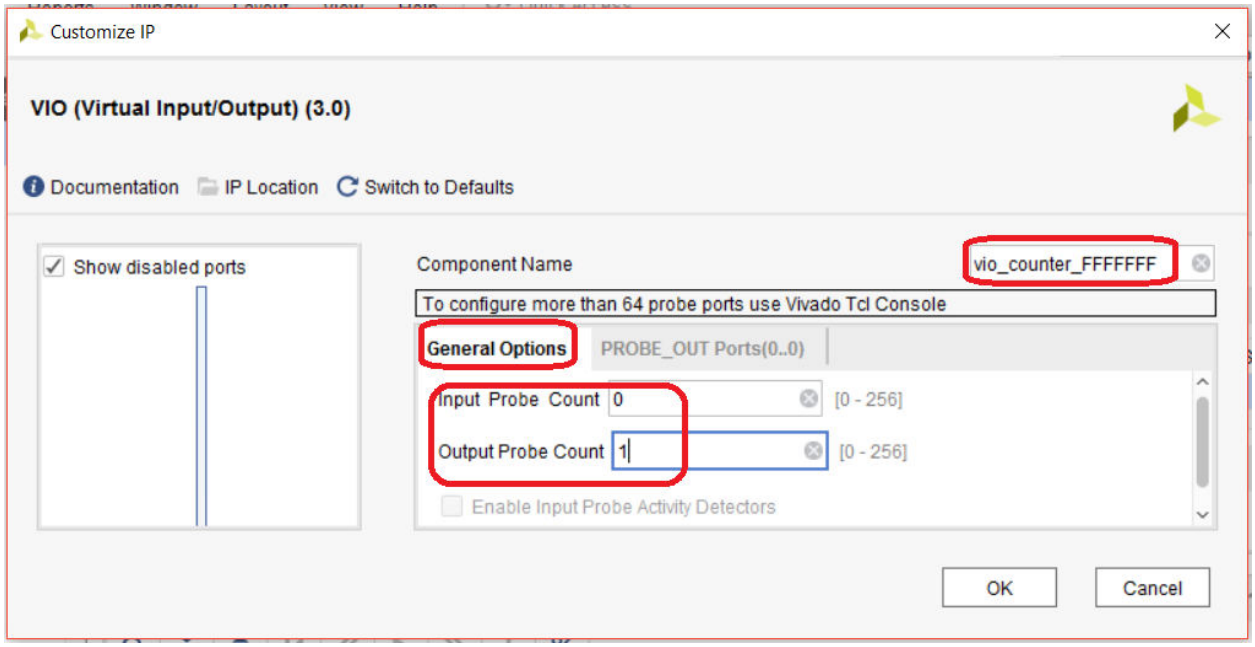
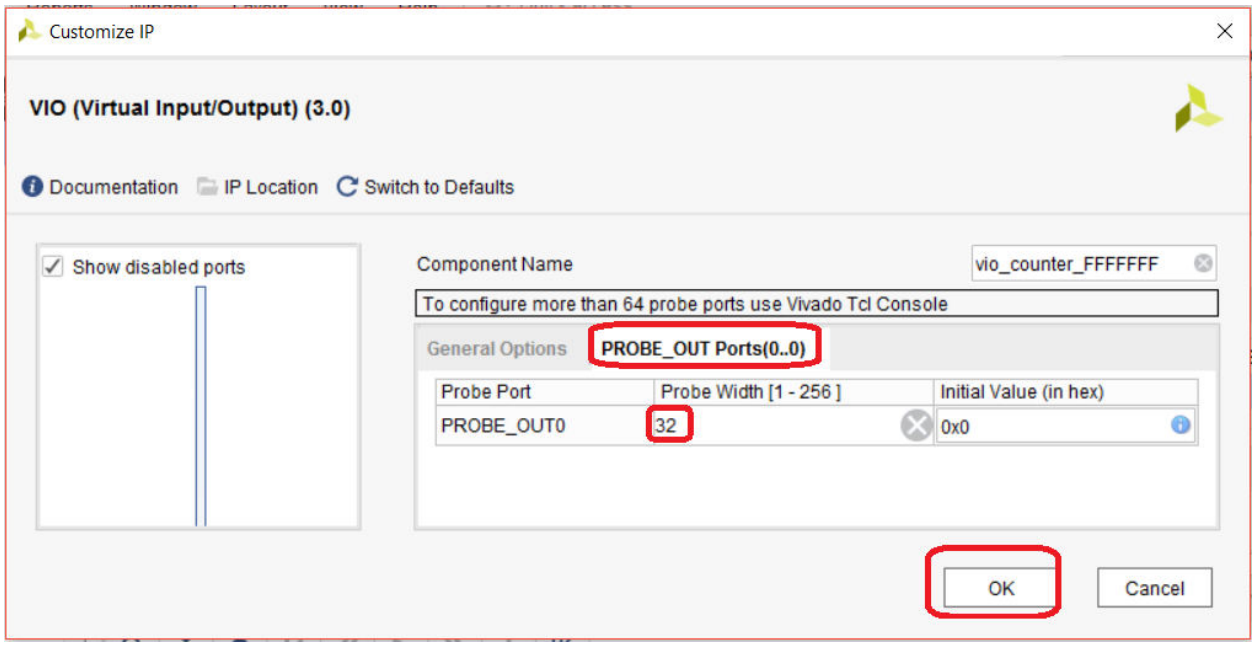
1. Instantiation of Virtual Input Output(VIO) IP

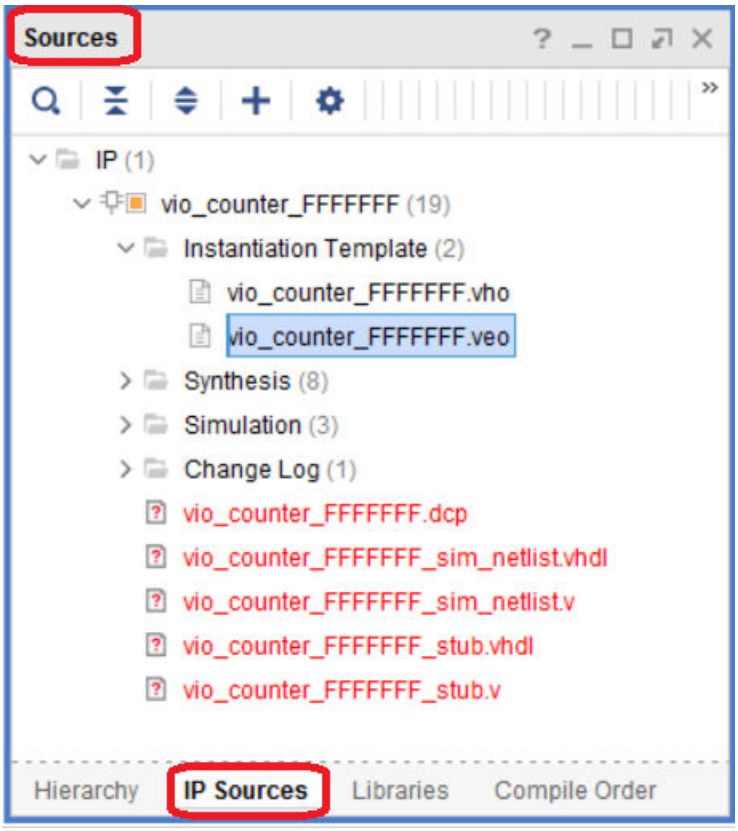
Project Manager → IP Catalog → Vivado Repository
→ Debug & verification → Debug → VIO (Virtual Input/Output)

Double click on VIO (Virtual Input/Output) to get Customize IP window





Double click on .veo icon to generate instantiation template in verilog

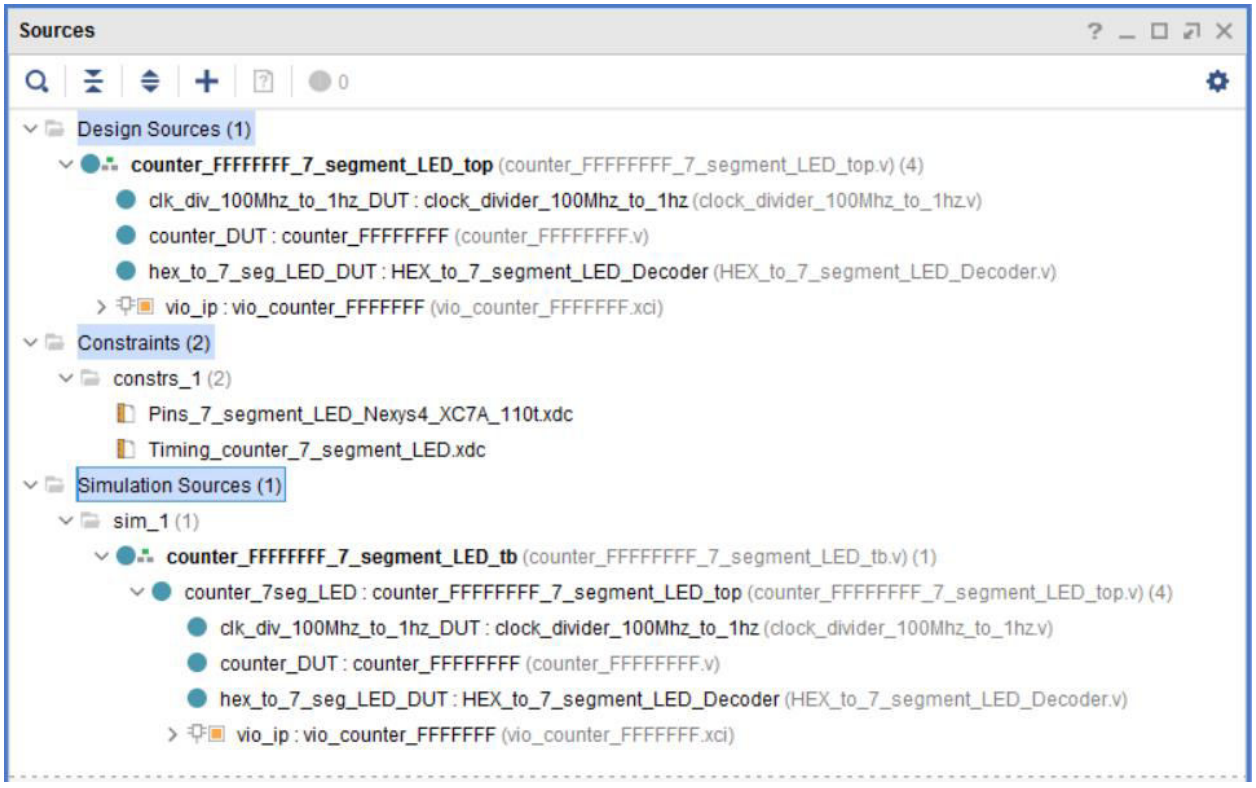



```
vio_counter_FFFFFFF your_instance_name (
  .clk(clk),              // input wire clk
  .probe_out0(probe_out0)  // output wire [31 : 0] probe_out0
);
```

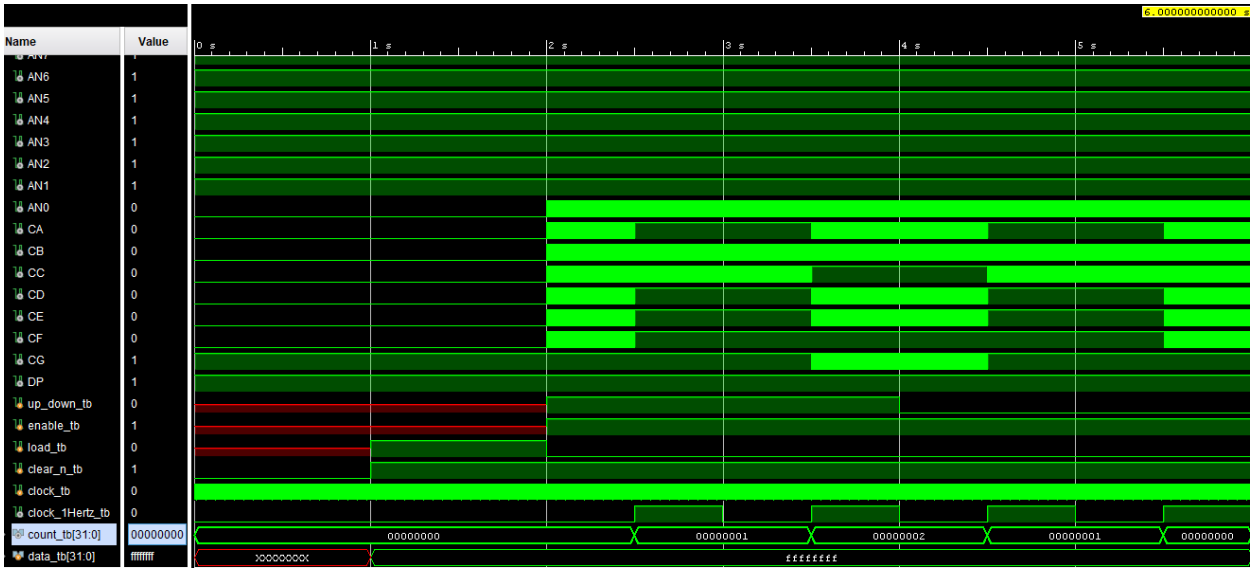
Copy and paste the above instantiation template in top module and
Change your_instance_name to vio_ip and do the port mapping

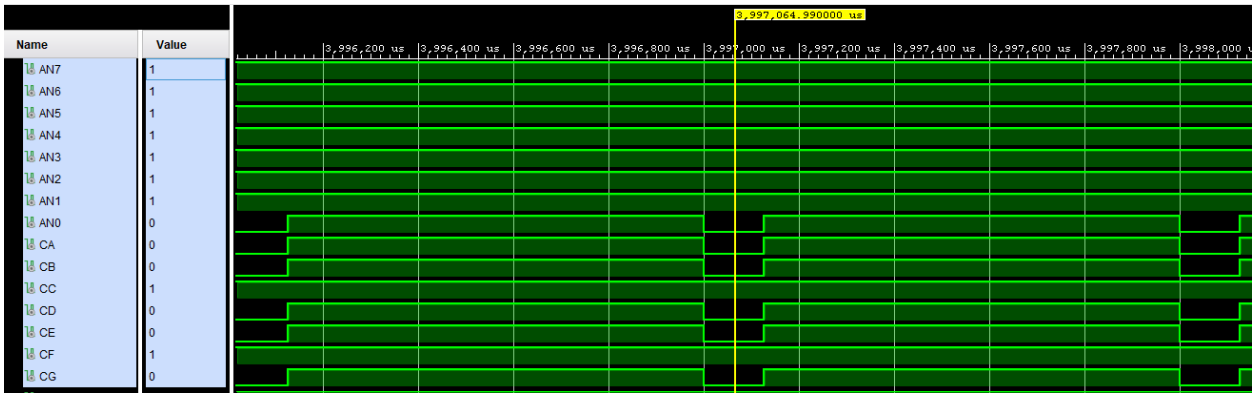
```
vio_counter_FFFFFFF vio_ip (.clk(Clock_100Mhz),  // input wire clk
                    .probe_out0(Data)  // output wire [31 : 0] probe_out0
                    );
```

Project Hierarchy

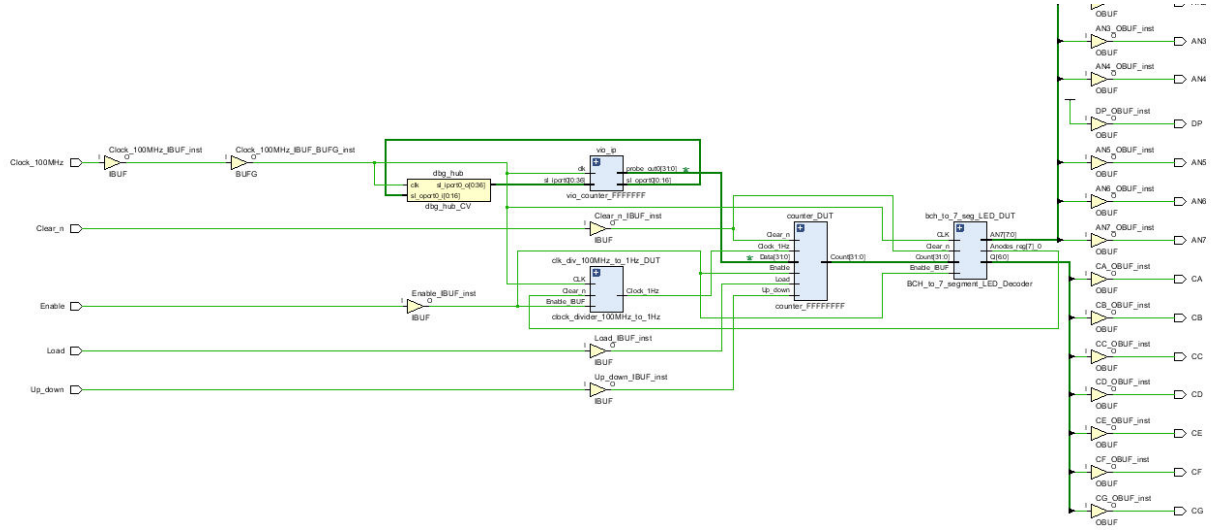


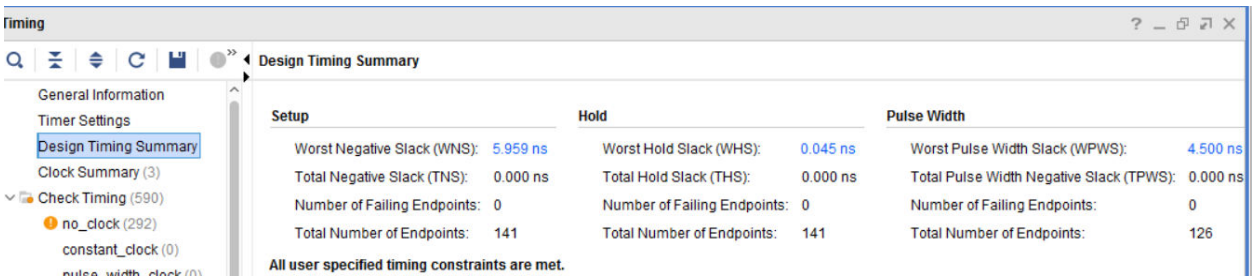
2. Simulation





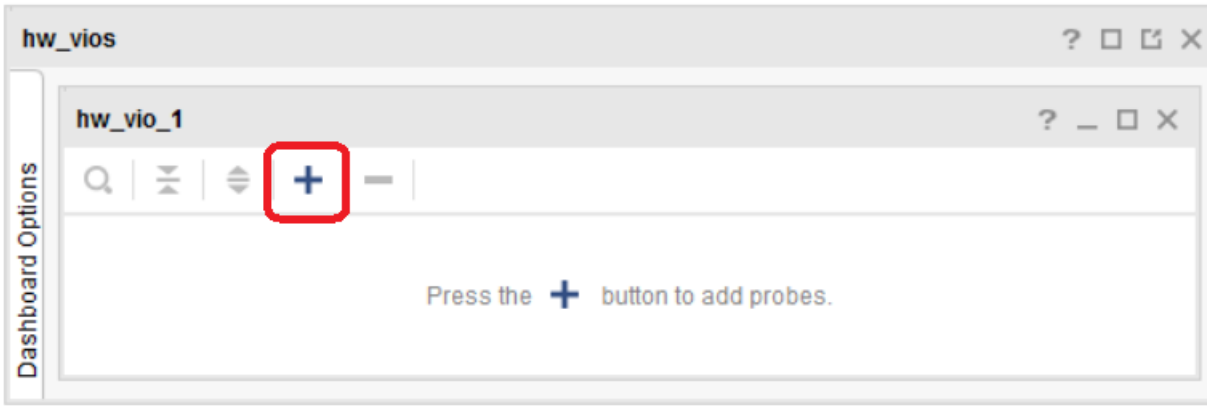
3. Synthesis

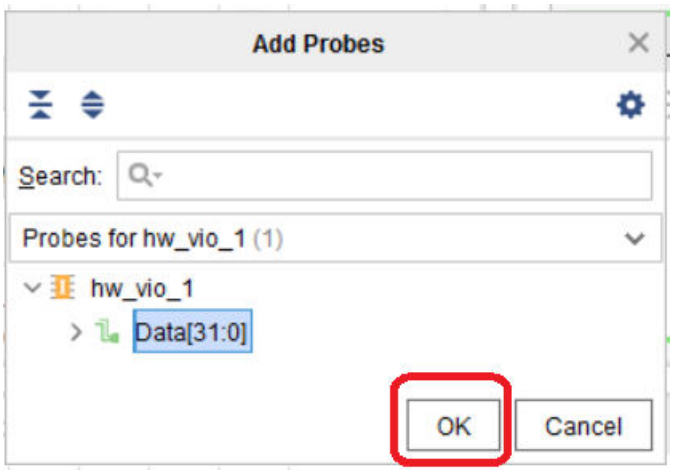

Clock_100MHz
Clock_100MHz_IBUF_inst
IBUF
Clock_100MHz_IBUF_BUFG_inst
BUFG
dbg_hub
dbg_hub_CV
vio_ip
vio_counter_FFFFFFF
Clear_n
Clear_n_IBUF_inst
Enable
Enable_IBUF_inst
clk_div_100MHz_to_1Hz_DUT
clock_divider_100MHz_to_1Hz
Load
Load_IBUF_inst
Up_down
Up_down_IBUF_inst
counter_DUT
counter_FFFFFFFF
bch_to_7_seg_LED_DUT
BCH_to_7_segment_LED_Decoder
AN3_OBUF_inst
AN4_OBUF_inst
DP_OBUF_inst
AN5_OBUF_inst
AN6_OBUF_inst
AN7_OBUF_inst
CA_OBUF_inst
CB_OBUF_inst
CC_OBUF_inst
CD_OBUF_inst
CE_OBUF_inst
CF_OBUF_inst
CG_OBUF_inst
OBUF
AN3
AN4
DP
AN5
AN6
AN7
CA
CB
CC
CD
CE
CF
CG


Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (3)
Check Timing (590)
no_clock (292)
constant_clock (0)
Setup
Worst Negative Slack (WNS): 5.959 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 141
Hold
Worst Hold Slack (WHS): 0.045 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 141
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 126
All user specified timing constraints are met.

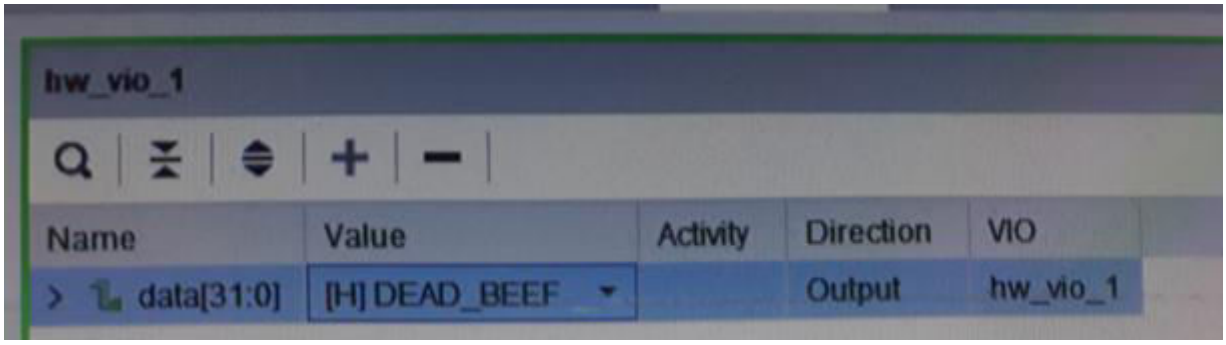
4. Implementation

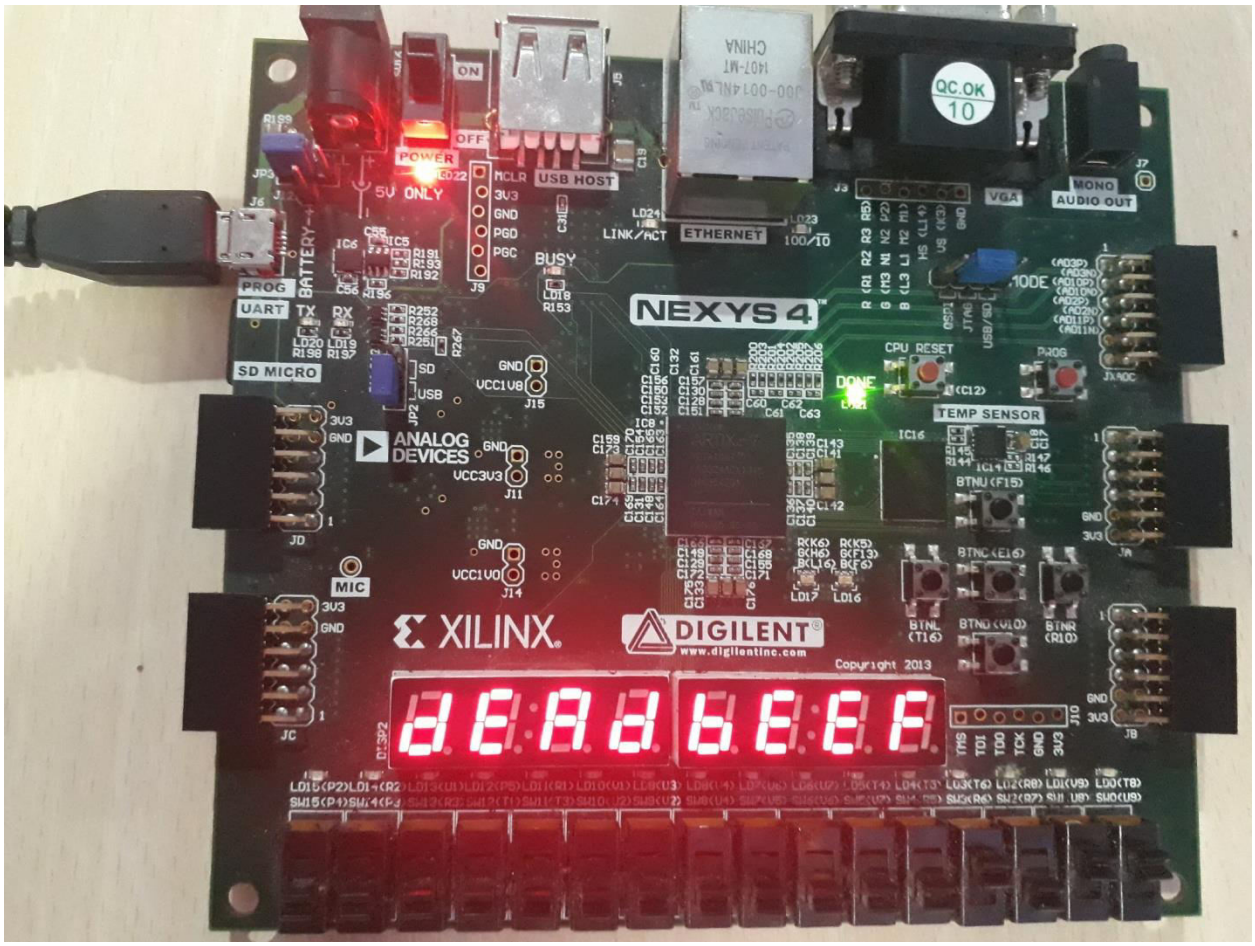
Add VIO Probe





Enable = 1; Load = 1; Data = DEADBEEF





Enable = 1; Load = 1; Data = 76543210