

1. Instantiation of Virtual Input Output(VIO) IP

Project Manager → IP Catalog → Vivado Repository
→ Debug & verification → Debug → VIO (Virtual Input/Output)

Double click on VIO (Virtual Input/Output) to get Customize IP window

Customize IP

VIO (Virtual Input/Output) (3.0)

Documentation IP Location Switch to Defaults

☒ Show disabled ports

Component Name: **vio_counter_99999999**

To configure more than 64 probe ports use Vivado Tcl Console

General Options

PROBE_OUT Ports(0..0)

Input Probe Count: 0 [0 - 256]

Output Probe Count: 1 [0 - 256]

OK Cancel

Customize IP

VIO (Virtual Input/Output) (3.0)

Documentation IP Location Switch to Defaults

☒ Show disabled ports

Component Name: **vio_counter_99999999**

To configure more than 64 probe ports use Vivado Tcl Console

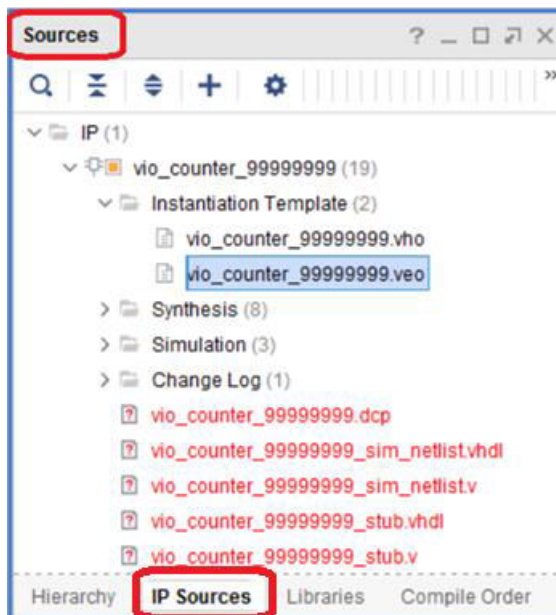
General Options

PROBE_OUT Ports(0..0)

Probe Port	Probe Width [1 - 256]	Initial Value (in hex)
PROBE_OUT0	27	0x0

OK Cancel

Double click on .veo icon to generate instantiation template in verilog



```
vio_counter_99999999 your_instance_name (  
    .clk(clk),           // input wire clk  
    .probe_out0(probe_out0) // output wire [26 : 0] probe_out0  
);
```

Copy and paste the above instantiation template in top module and
Change your_instance_name to vio_ip and do the port mapping

```
vio_counter_99999999 vio_ip (  
    .clk(Clock_100MHz),      // input wire clk  
    .probe_out0(data) // output wire [26 : 0] probe_out0  
);
```

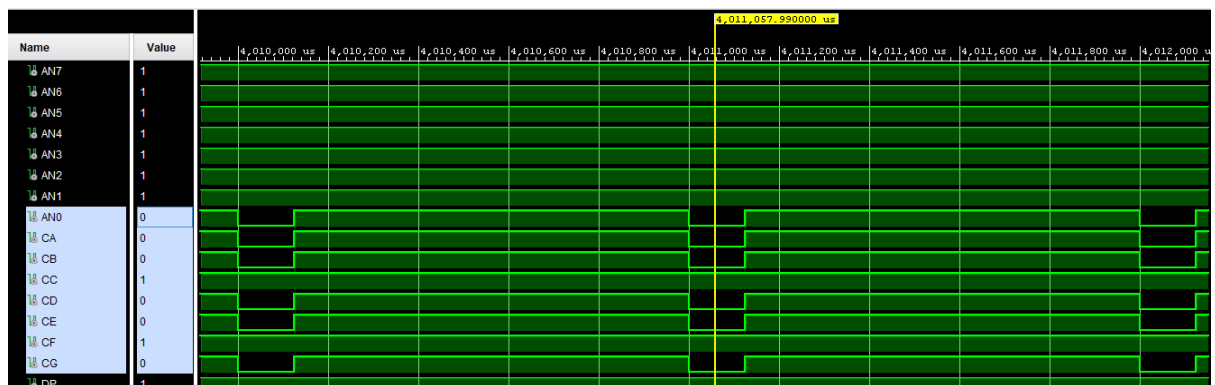
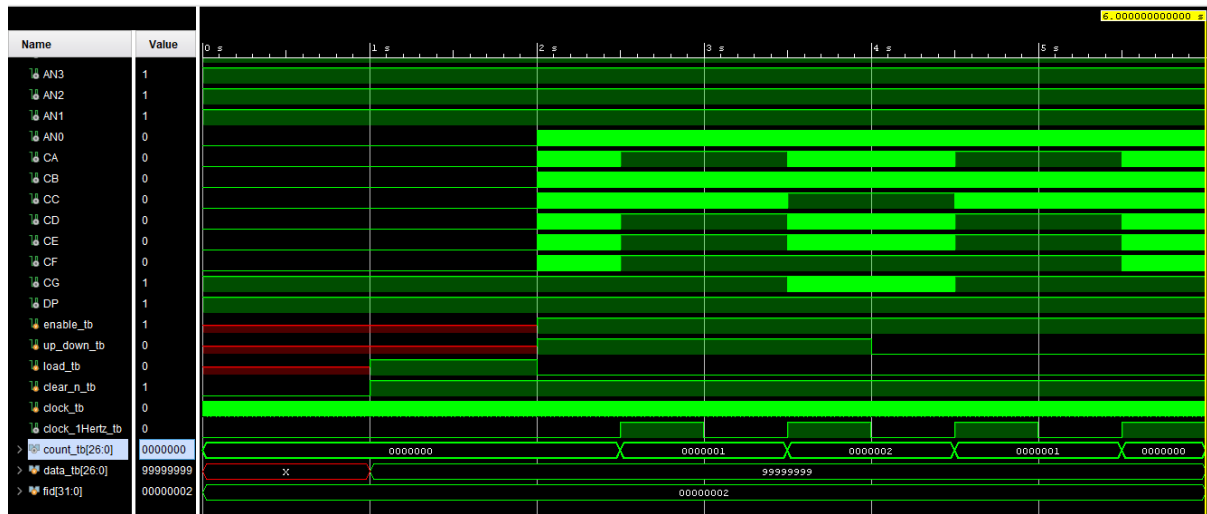
Project Hierarchy

Sources

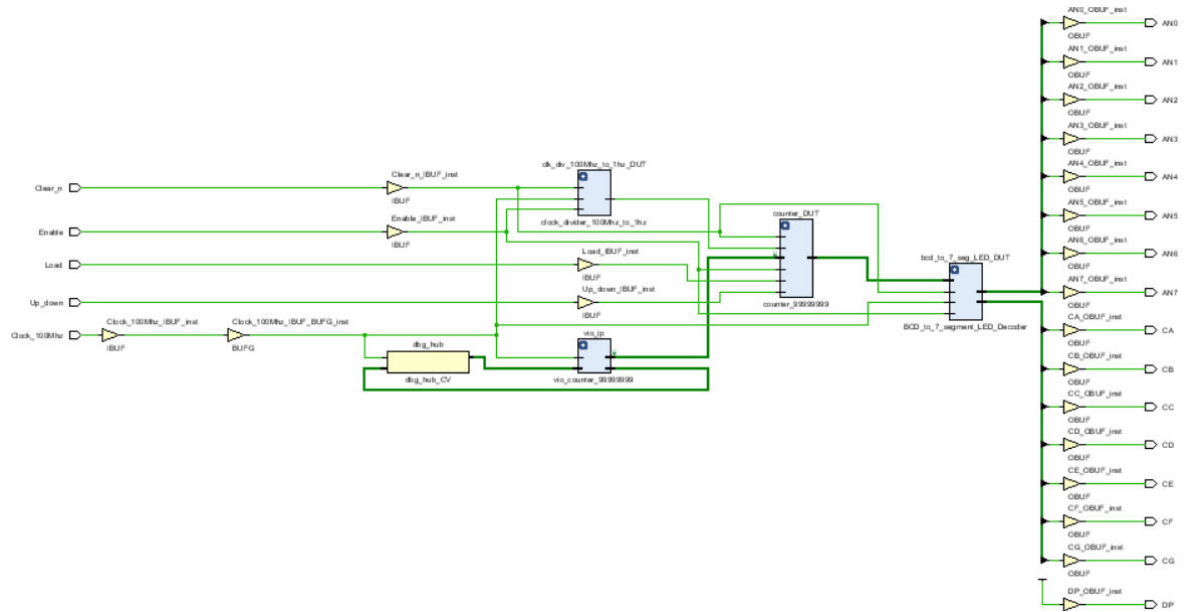
Q [] + [?] 0

- Design Sources (1)
 - counter_99999999_7_segment_LED_top (counter_99999999_7_segment_LED_top.v) (4)
 - clk_div_100Mhz_to_1hz_DUT : clock_divider_100Mhz_to_1hz (clock_divider_100Mhz_to_1hz.v)
 - counter_DUT : counter_99999999 (counter_99999999.v)
 - bcd_to_7_seg_LED_DUT : BCD_to_7_segment_LED_Decoder (BCD_to_7_segment_LED_Decoder.v)
 - > vio_ip : vio_counter_99999999 (vio_counter_99999999.xci) (1)
- Constraints (2)
 - constrs_1 (2)
 - Pins_7_segment_LED_Nexys4_XC7A_110t.xdc
 - Timing_counter_7_segment_LED.xdc
- Simulation Sources (1)
 - sim_1 (1)
 - counter_99999999_7_seg_LED_tb (counter_99999999_7_seg_LED_tb.v) (1)
 - counter_7seg_LED : counter_99999999_7_segment_LED_top (counter_99999999_7_segment_LED_top.v) (4)
 - clk_div_100Mhz_to_1hz_DUT : clock_divider_100Mhz_to_1hz (clock_divider_100Mhz_to_1hz.v)
 - counter_DUT : counter_99999999 (counter_99999999.v)
 - bcd_to_7_seg_LED_DUT : BCD_to_7_segment_LED_Decoder (BCD_to_7_segment_LED_Decoder.v)
 - > vio_ip : vio_counter_99999999 (vio_counter_99999999.xci)

2. Simulation



3. Synthesis



Timing

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Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (3)

Check Timing (590)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

Unconstrained Paths

Setup

Hold

Pulse Width

Worst Negative Slack (WNS):

5.804 ns

Worst Hold Slack (WHS):

0.045 ns

Worst Pulse Width Slack (WPWS):

4.500 ns

Total Negative Slack (TNS):

0.000 ns

Total Hold Slack (THS):

0.000 ns

Total Pulse Width Negative Slack (TPWS):

0.000 ns

Number of Failing Endpoints:

0

Number of Failing Endpoints:

0

Number of Failing Endpoints:

0

Total Number of Endpoints:

165

Total Number of Endpoints:

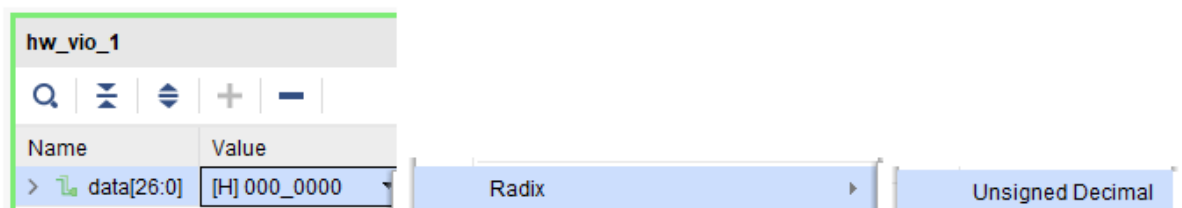
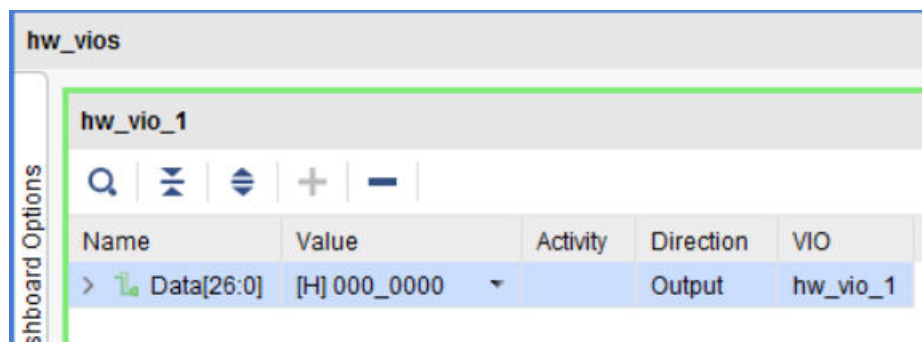
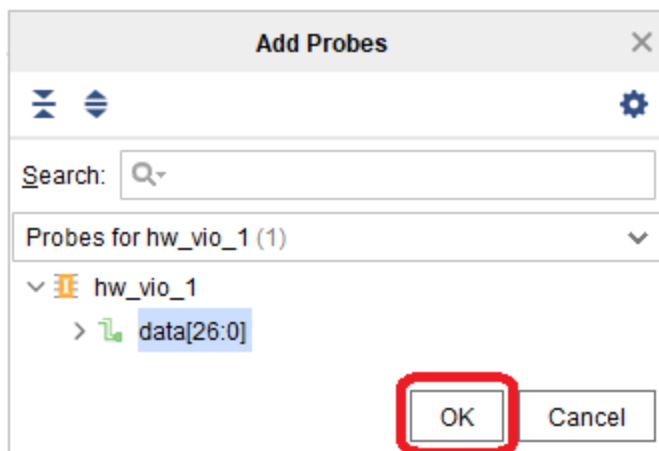
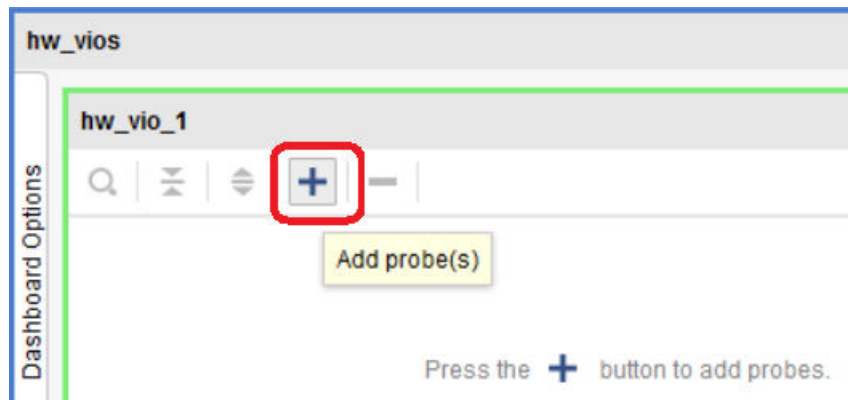
165

Total Number of Endpoints:

116

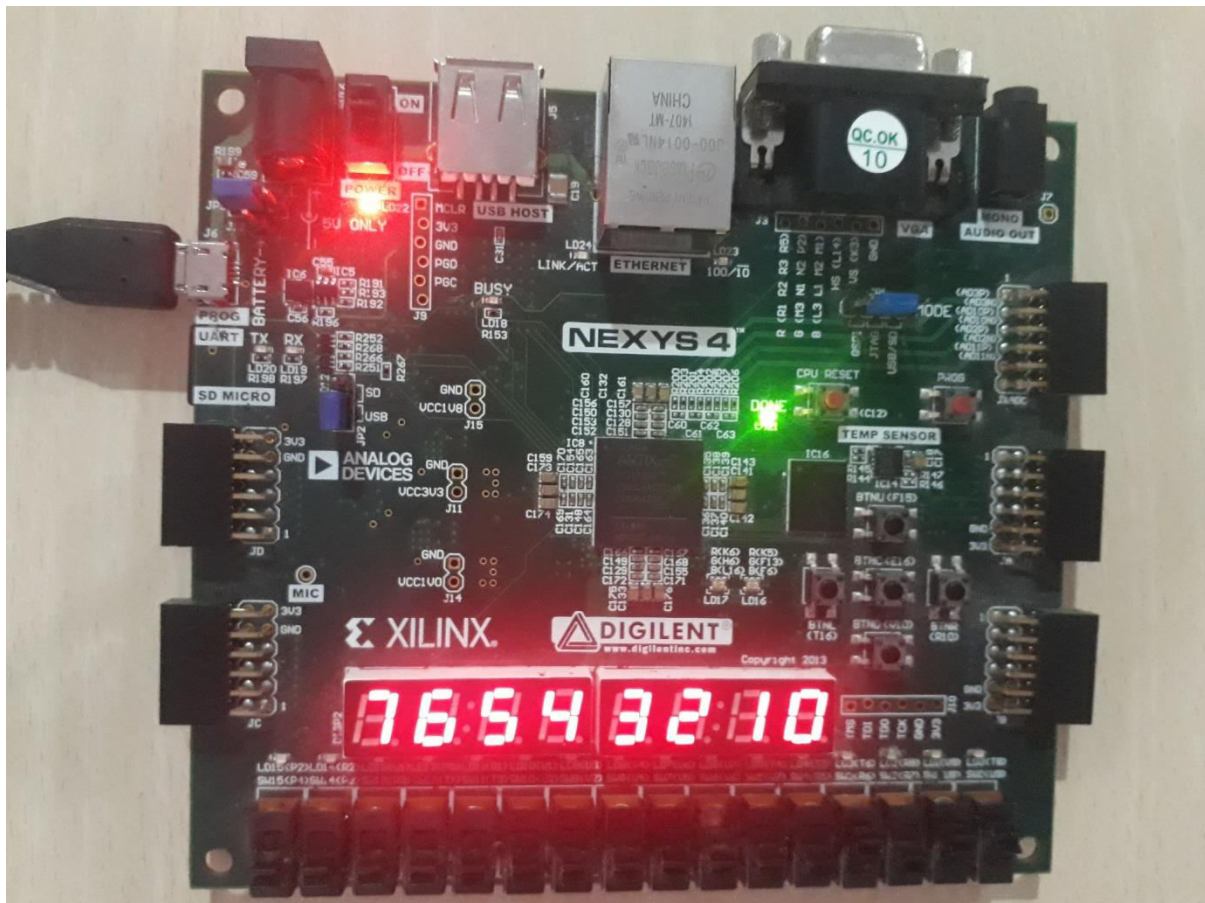
All user specified timing constraints are met.

4. Implementation

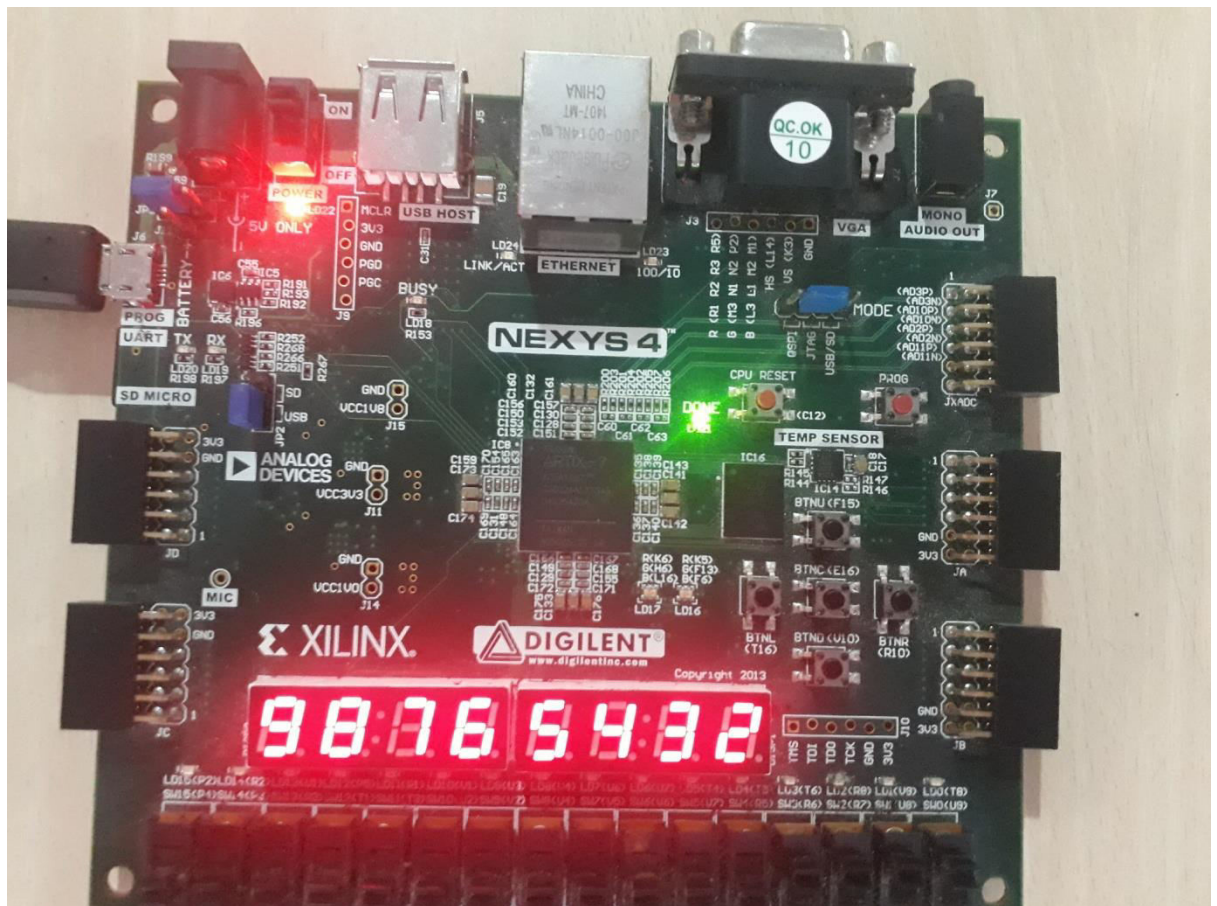
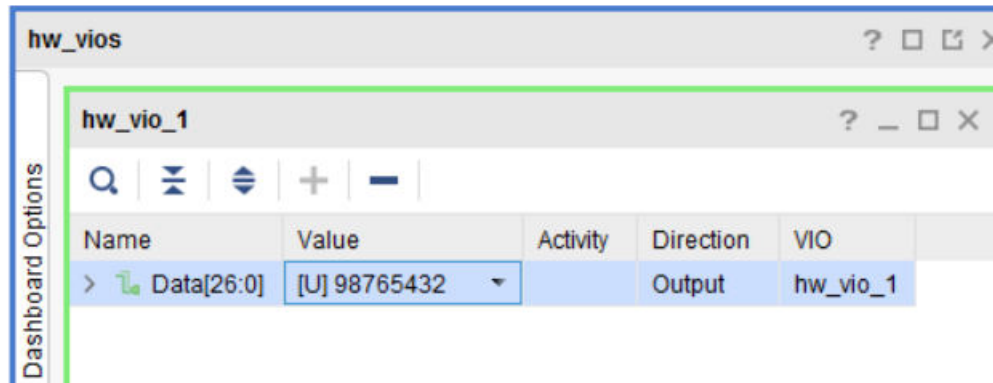


4.1. Enable = 1; Load = 1; Data = 76543210

hw_vios					
hw_vio_1					
<div>Dashboard Options</div> <div><div>🔍</div><div>⏮</div><div>⏭</div><div>+</div><div>-</div></div>					
Name	Value	Activity	Direction	VIO	
> Data[26:0]	[U] 76543210		Output	hw_vio_1	



4.2. Enable = 1; Load = 1; Data = 98765432



4.3. Enable = 1; Load = 1; Data = 134217727

