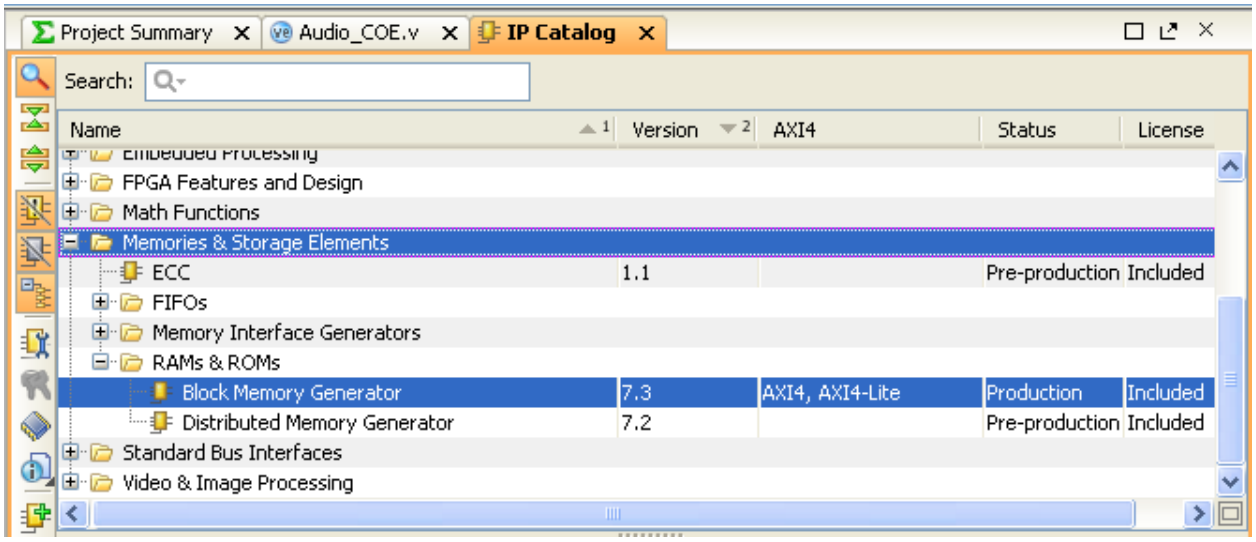
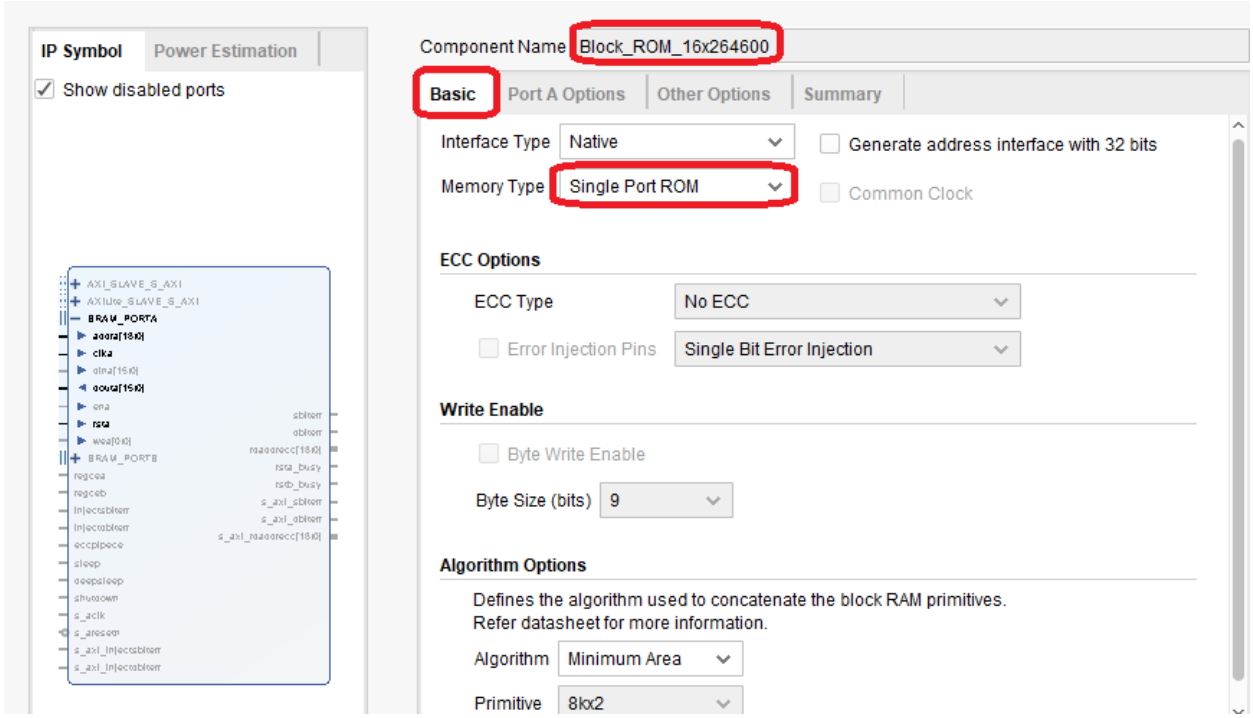
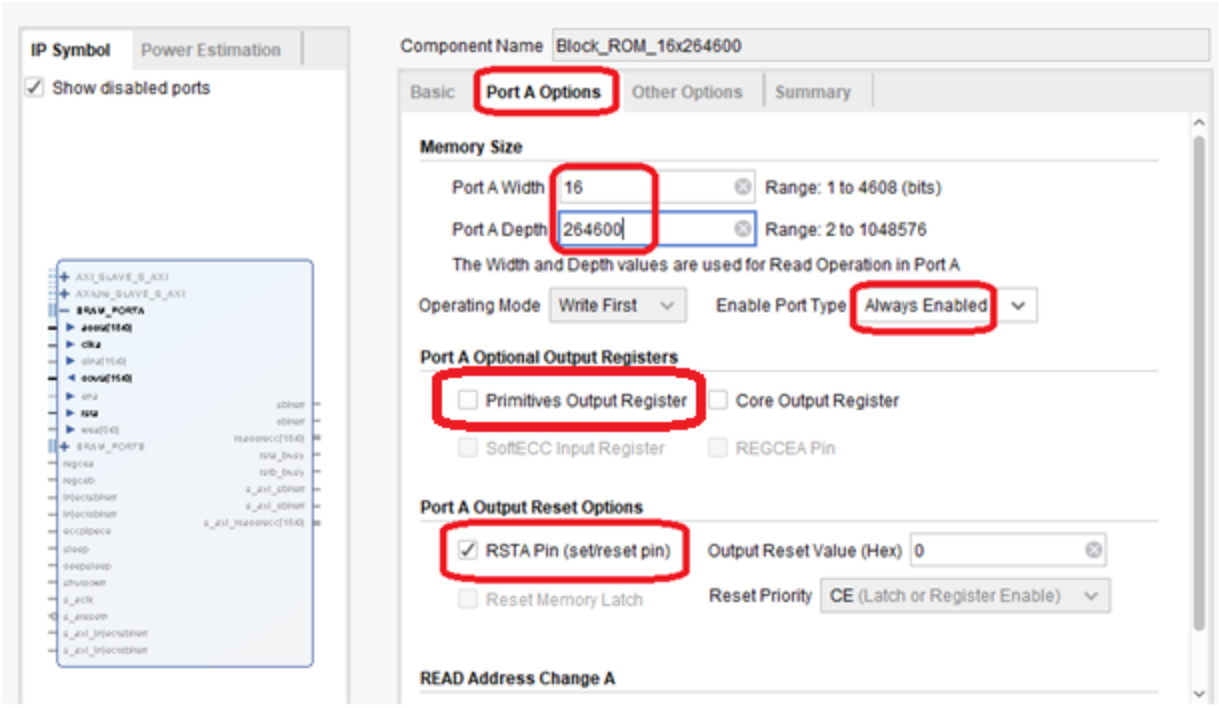
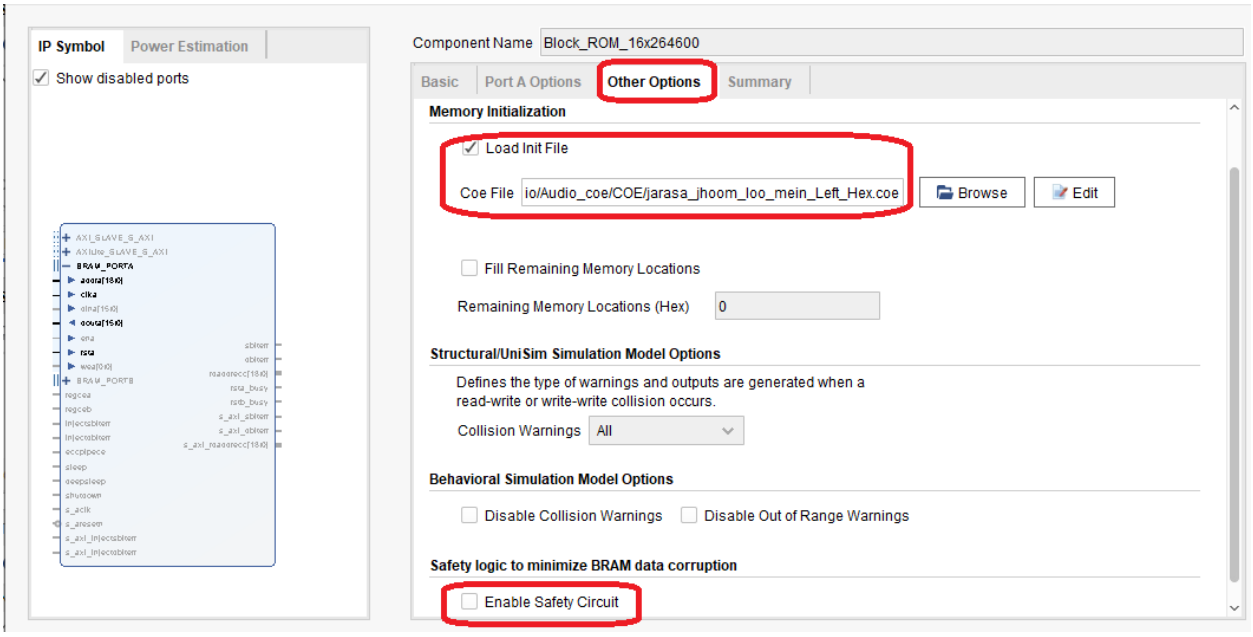
1. Block ROM ip instantiation

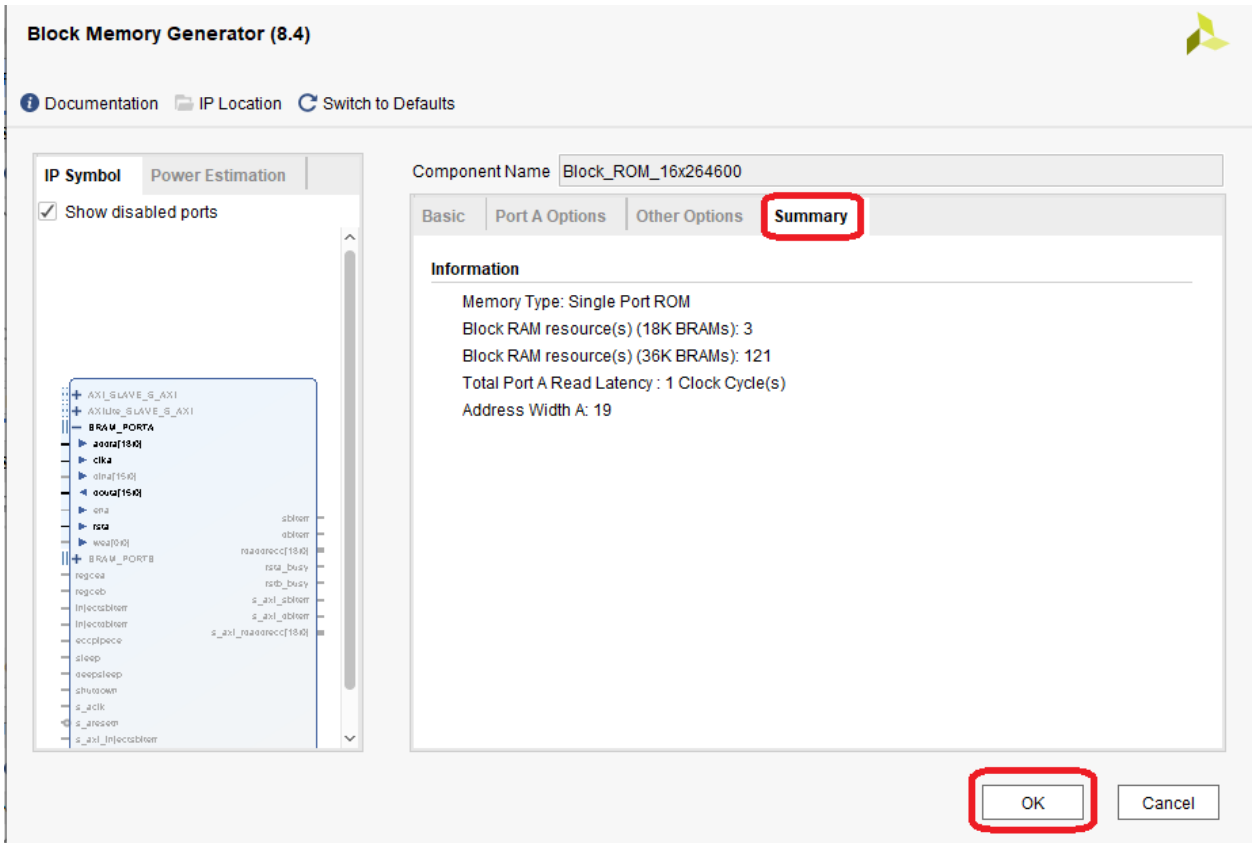
1.1. **Vivado** → Project Manager → IP Catalog → Memories & Storage Elements → RAMs & ROMs → Block Memory Generator





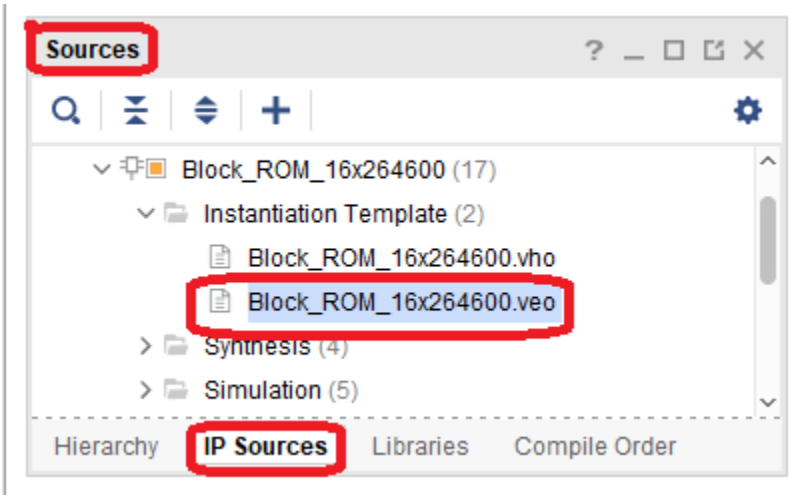

IP Symbol
Power Estimation
Show disabled ports
Component Name
Block_ROM_16x264600
Basic
Port A Options
Other Options
Summary
Memory Size
Port A Width
16
Range: 1 to 4608 (bits)
Port A Depth
264600
Range: 2 to 1048576
The Width and Depth values are used for Read Operation in Port A
Operating Mode
Write First
Enable Port Type
Always Enabled
Port A Optional Output Registers
Primitives Output Register
Core Output Register
SoftECC Input Register
REGCEA Pin
Port A Output Reset Options
RSTA Pin (set/reset pin)
Output Reset Value (Hex)
0
Reset Memory Latch
Reset Priority
CE (Latch or Register Enable)
READ Address Change A


IP Symbol
Power Estimation
Show disabled ports
Component Name
Block_ROM_16x264600
Basic
Port A Options
Other Options
Summary
Memory Initialization
Load Init File
Coe File
io/Audio_coe/COE/jarasa_jhoom_loo_mein_Left_Hex.coe
Browse
Edit
Fill Remaining Memory Locations
Remaining Memory Locations (Hex)
0
Structural/UniSim Simulation Model Options
Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.
Collision Warnings
All
Behavioral Simulation Model Options
Disable Collision Warnings
Disable Out of Range Warnings
Safety logic to minimize BRAM data corruption
Enable Safety Circuit

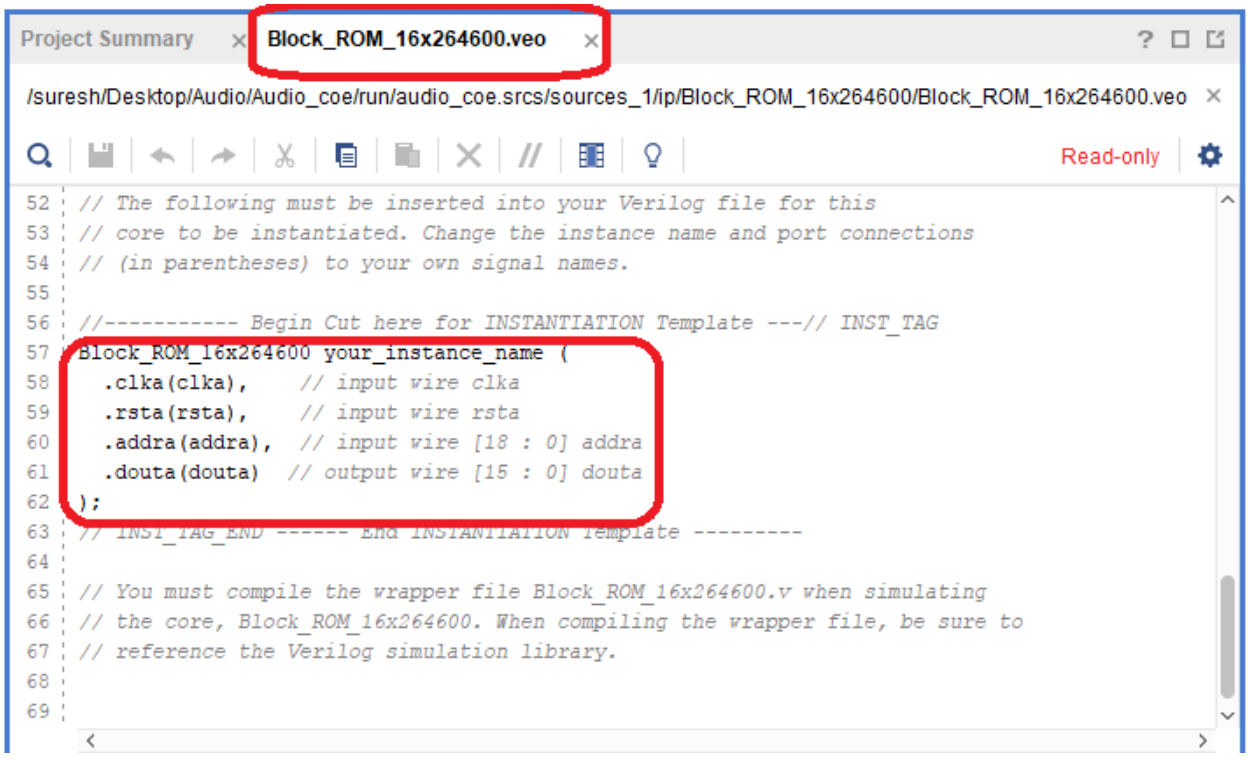


Wait till Vivado Finishes IP customization

1.2. Generate Instantiation Template



1.2.1. Double click on .veo for Verilog Instance



1.2.3. Copy and Paste Instantiation Template into Audio_COE.v file

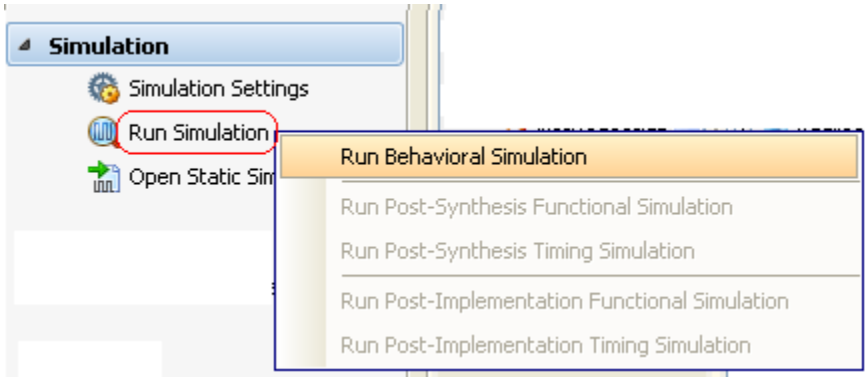
Change your_instance_name to any user defined instance name(eg: BROM_ip in this tutorial)

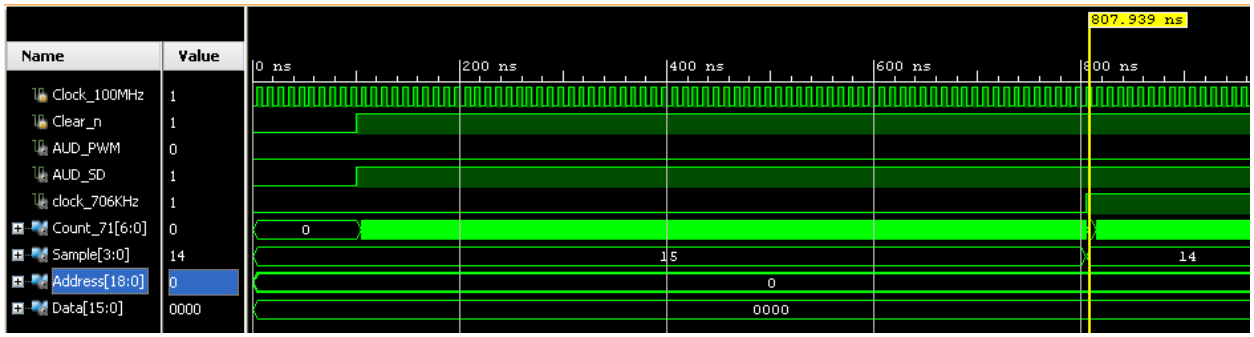
```
Block_ROM_16x264600 your_instance_name (
        .clka(clka),    // input wire clka
        .rsta(rsta),    // input wire rsta
       .addra(addra),  // input wire [18 : 0] addra
       .douta(douta)  // output wire [15 : 0] douta
);
```

1.2.4. Do port mapping

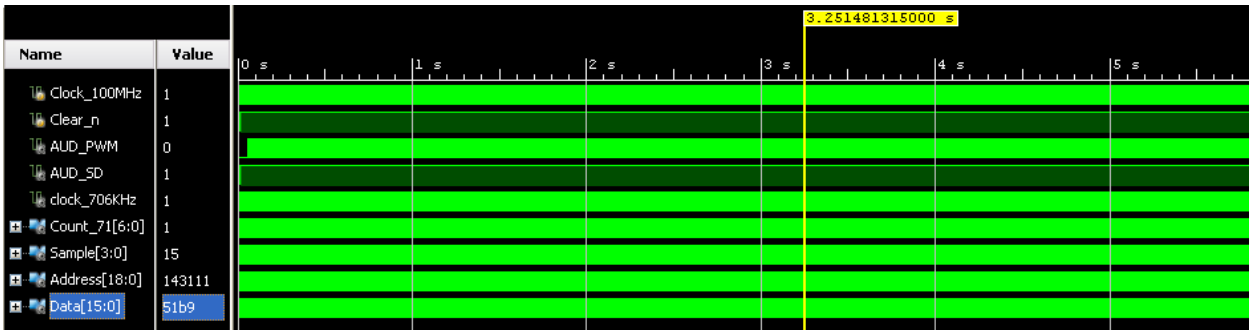
```
  Block_ROM_16x264600 BROM_ip (
       .clka(clock_706KHz), // input clka
       .rsta(!Clear_n),    // input rsta
       .addra(Address),    // input [18 : 0] addra
       .douta(Data)       // output [15 : 0]  douta
      );
```

2. Simulation

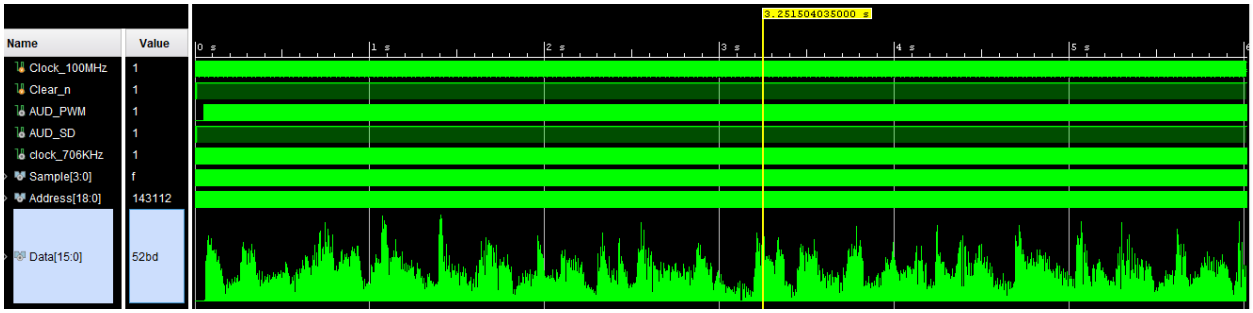


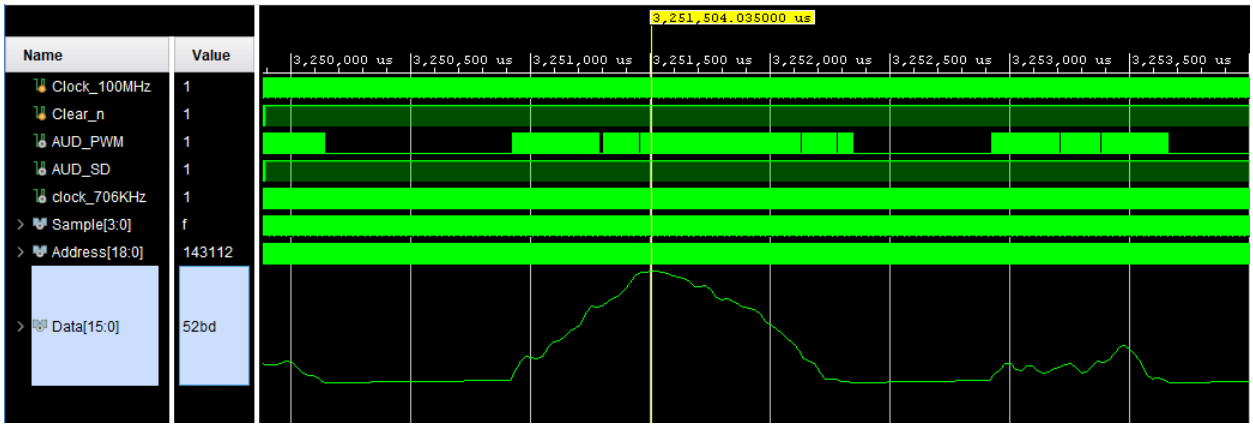


TCL console → run –all

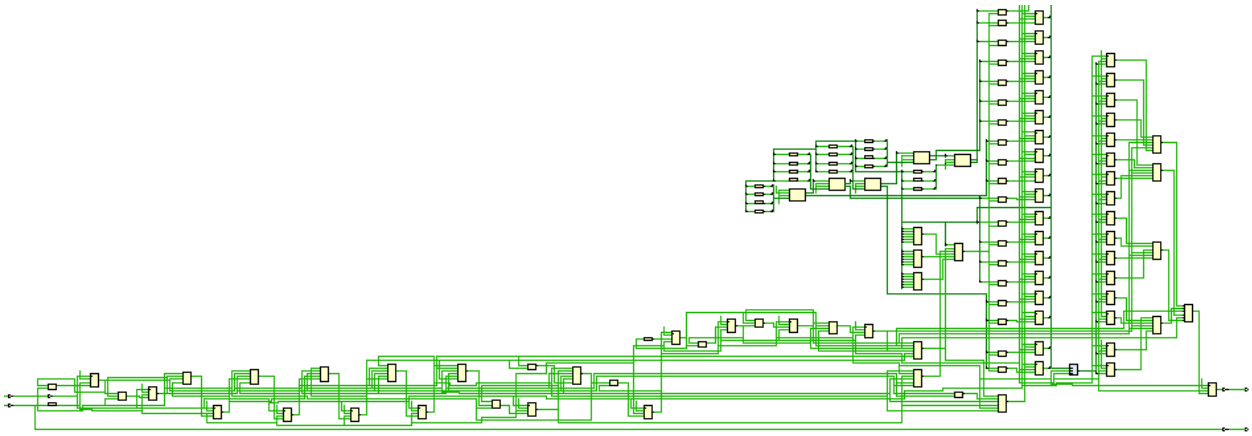


Right click on **Data** and Change waveform style to Analog





3. Synthesis



4. Implementation

Audio_from_coe.mp4