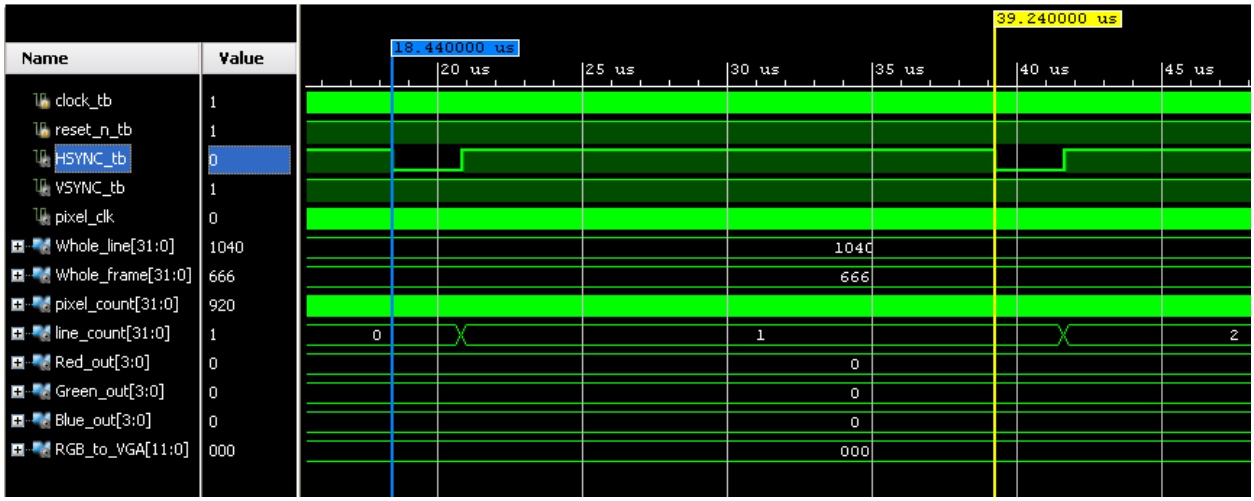
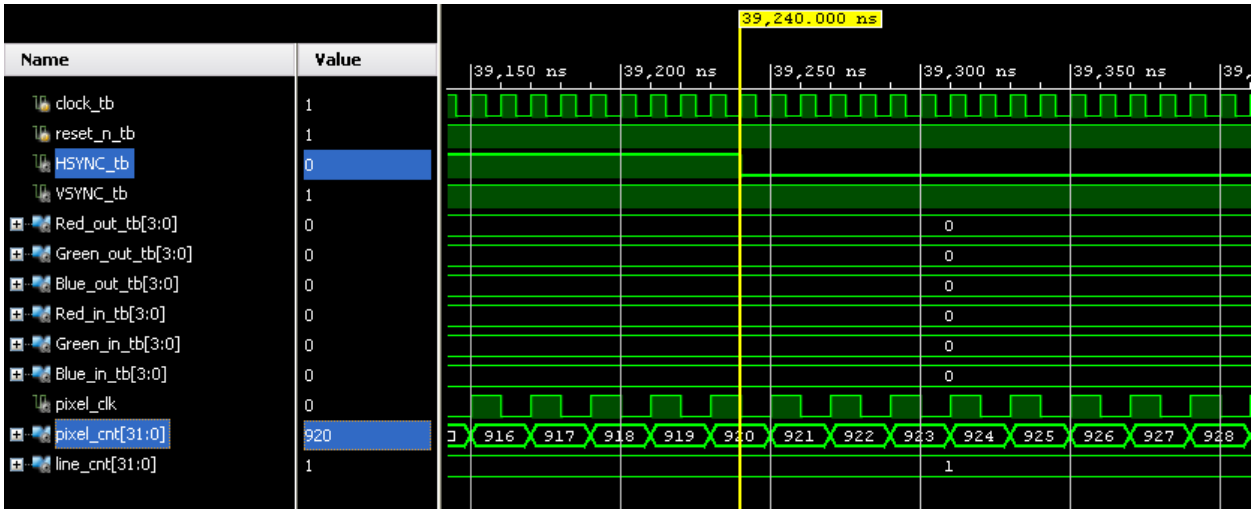
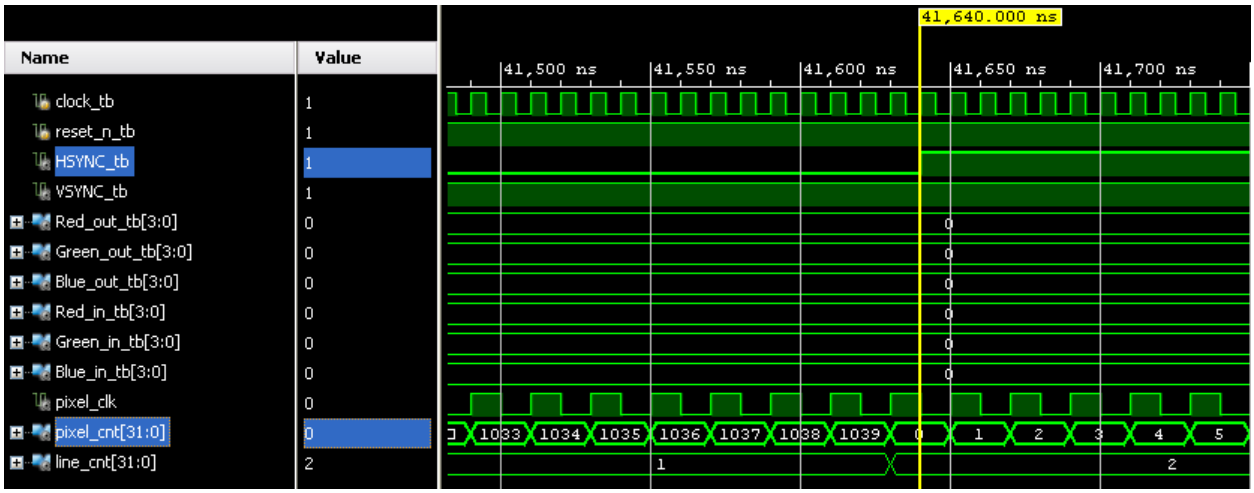
1. Simulation Full

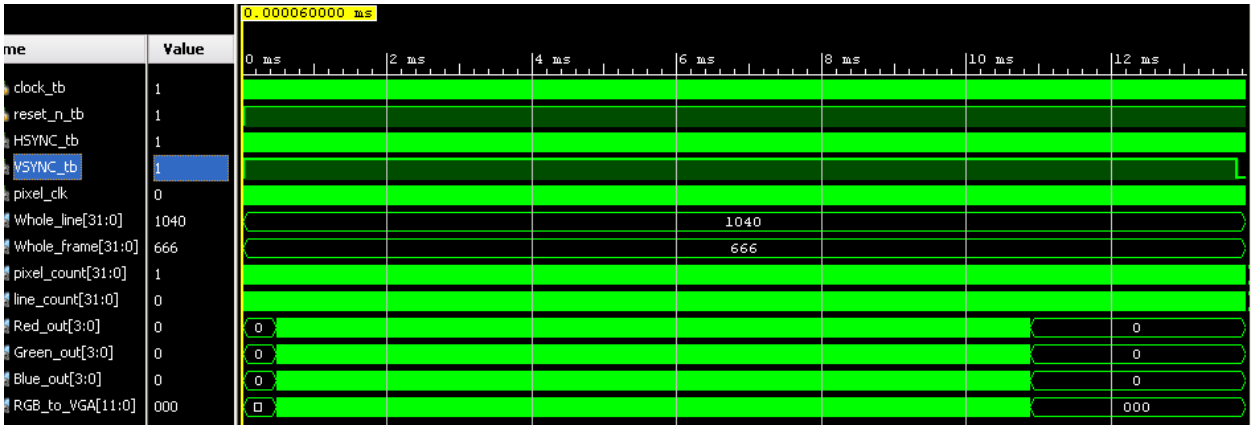
1.1. HSync



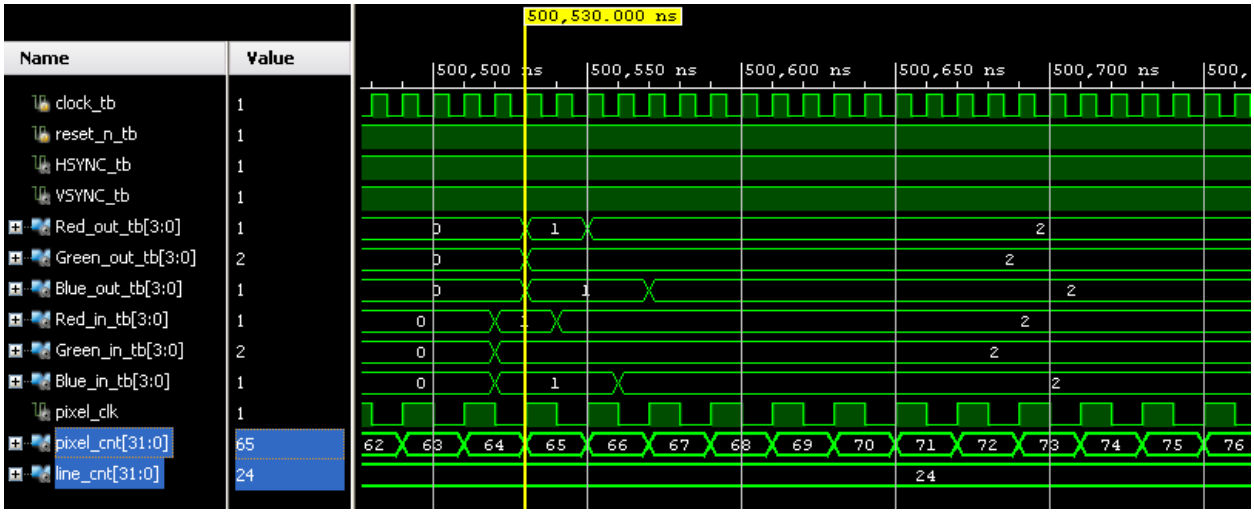


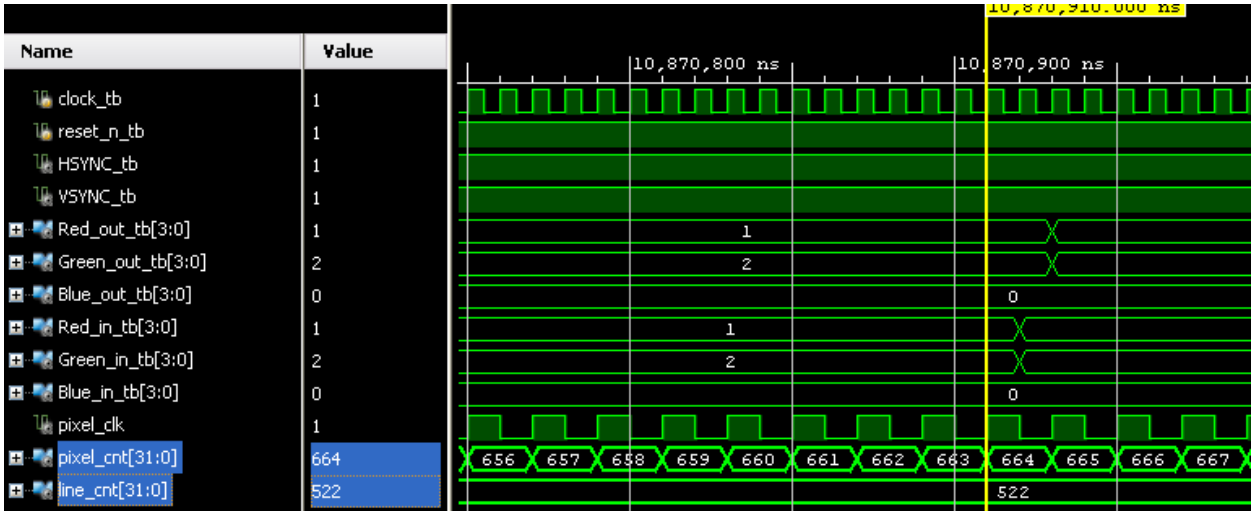

Name
Value
clock_tb
reset_n_tb
HSYNC_tb
VSYNC_tb
Red_out_tb[3:0]
Green_out_tb[3:0]
Blue_out_tb[3:0]
Red_in_tb[3:0]
Green_in_tb[3:0]
Blue_in_tb[3:0]
pixel_clk
pixel_cnt[31:0]
line_cnt[31:0]
1
1
1
1
0
0
0
0
0
0
0
0
2
41,640.000 ns
41,500 ns
41,550 ns
41,600 ns
41,650 ns
41,700 ns
1033
1034
1035
1036
1037
1038
1039
0
1
2
3
4
5

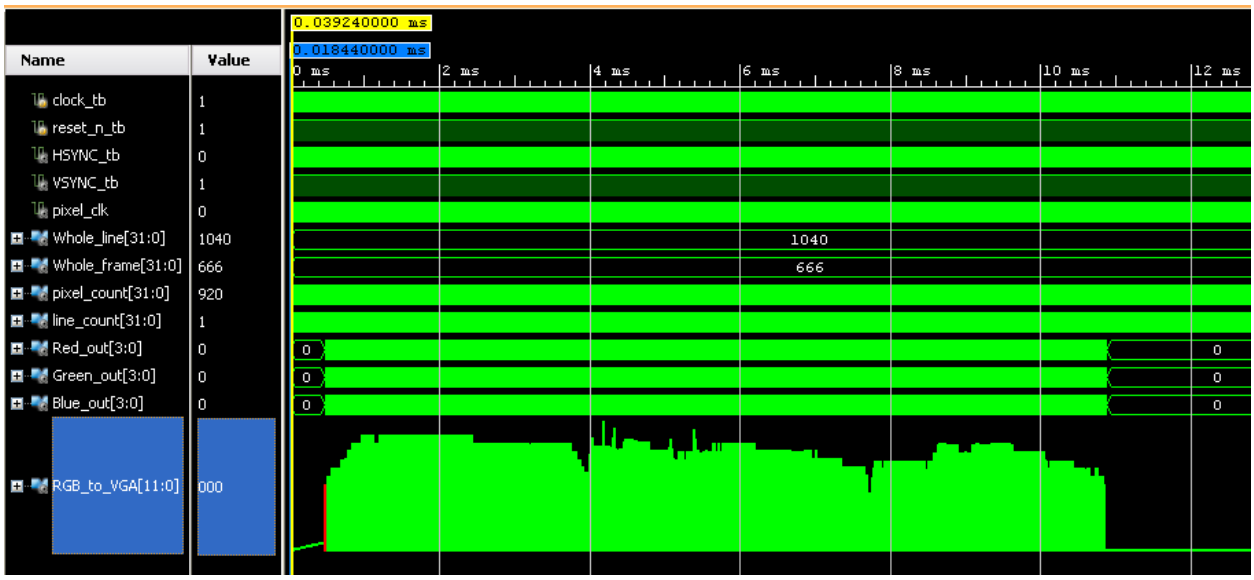
1.2. VSync


Value
clock_tb
reset_n_tb
HSYNC_tb
VSYNC_tb
pixel_clk
Whole_line[31:0]
Whole_frame[31:0]
pixel_count[31:0]
line_count[31:0]
Red_out[3:0]
Green_out[3:0]
Blue_out[3:0]
RGB_to_VGA[11:0]
1
1
1
1
0
1040
666
1
0
0
0
0
000
0.000060000 ms
0 ms
2 ms
4 ms
6 ms
8 ms
10 ms
12 ms
1040
666
000

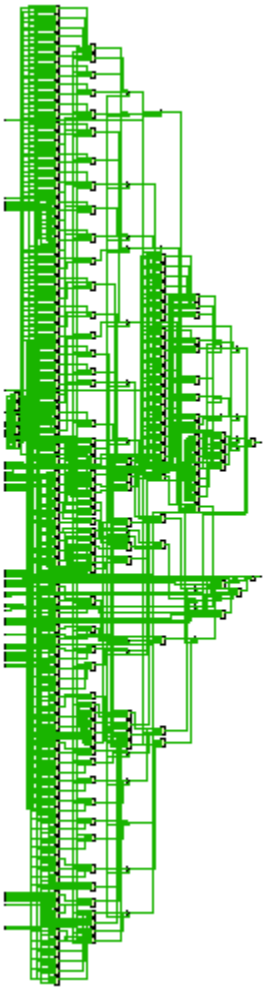
1.3. Data


Name
Value
clock_tb
reset_n_tb
HSYNC_tb
VSYNC_tb
Red_out_tb[3:0]
Green_out_tb[3:0]
Blue_out_tb[3:0]
Red_in_tb[3:0]
Green_in_tb[3:0]
Blue_in_tb[3:0]
pixel_clk
pixel_cnt[31:0]
line_cnt[31:0]
1
1
1
1
1
2
1
1
2
1
65
24
500,530.000 ns
500,500 ns
500,550 ns
500,600 ns
500,650 ns
500,700 ns
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
24


Name
Value
clock_tb
reset_n_tb
HSYNC_tb
VSYNC_tb
Red_out_tb[3:0]
Green_out_tb[3:0]
Blue_out_tb[3:0]
Red_in_tb[3:0]
Green_in_tb[3:0]
Blue_in_tb[3:0]
pixel_clk
pixel_cnt[31:0]
line_cnt[31:0]
1
1
1
1
1
2
0
1
2
0
664
522
10,870,800 ns
10,870,900 ns
656
657
658
659
660
661
662
663
664
665
666
667
522


0.039240000 ms
0.018440000 ms
0 ms
2 ms
4 ms
6 ms
8 ms
10 ms
12 ms
Name
Value
clock_tb
1
reset_n_tb
1
HSYNC_tb
0
VSYNC_tb
1
pixel_clk
0
Whole_line[31:0]
1040
Whole_frame[31:0]
666
pixel_count[31:0]
920
line_count[31:0]
1
Red_out[3:0]
0
Green_out[3:0]
0
Blue_out[3:0]
0
RGB_to_VGA[11:0]
000
1040
666

2. Synthesis



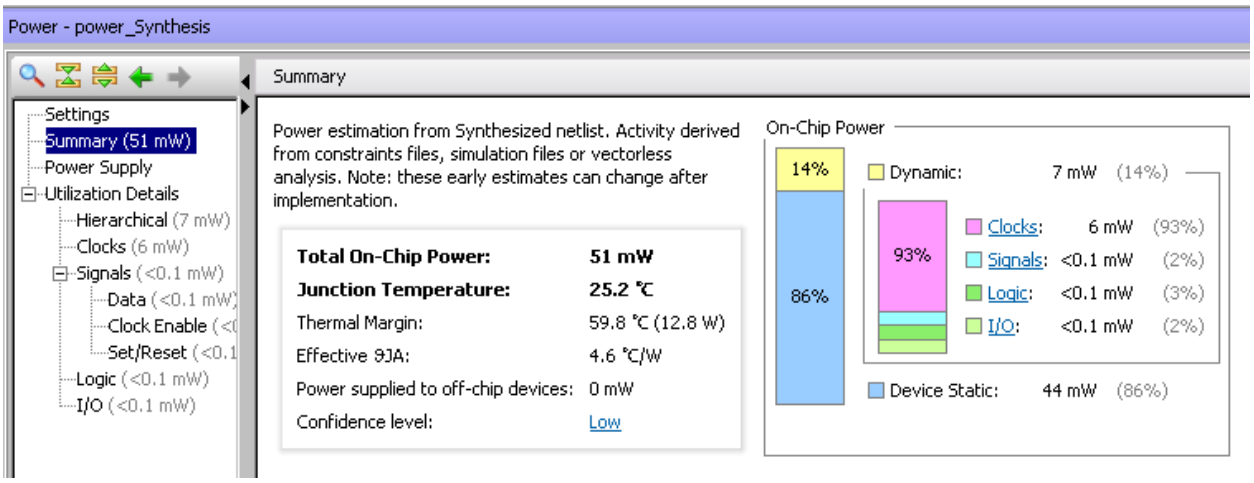
Timing - Timing Summary - timing_Synthesis

General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Path Groups
User Ignored Paths
Unconstrained Paths

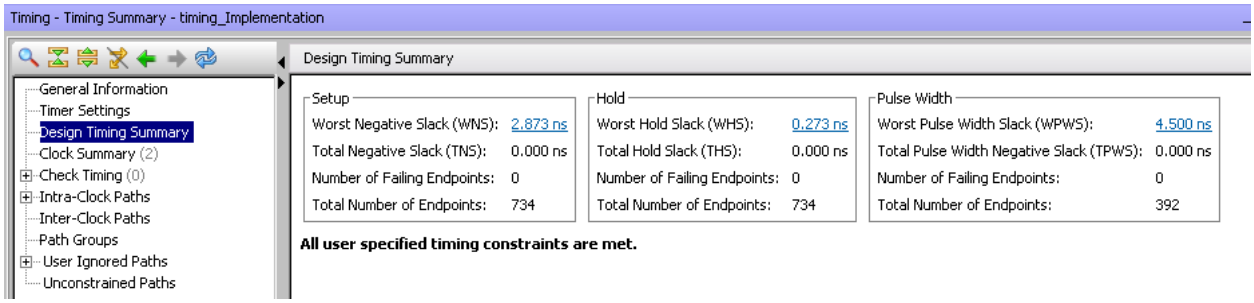
Design Timing Summary

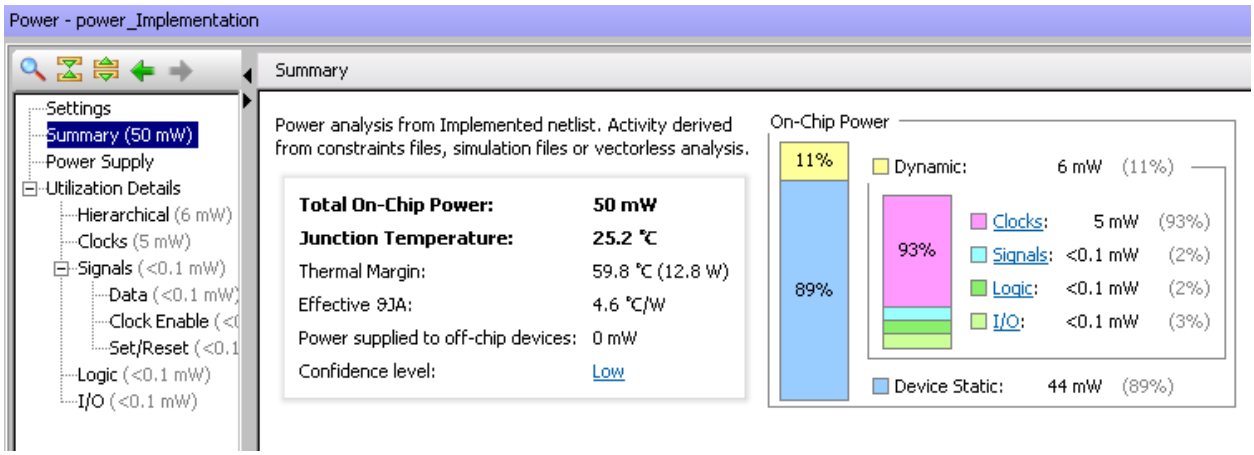
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.689 ns	Worst Hold Slack (WHS):	0.248 ns	Worst Pulse Width Slack (WPWS):	4.404 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	734	Total Number of Endpoints:	734	Total Number of Endpoints:	392

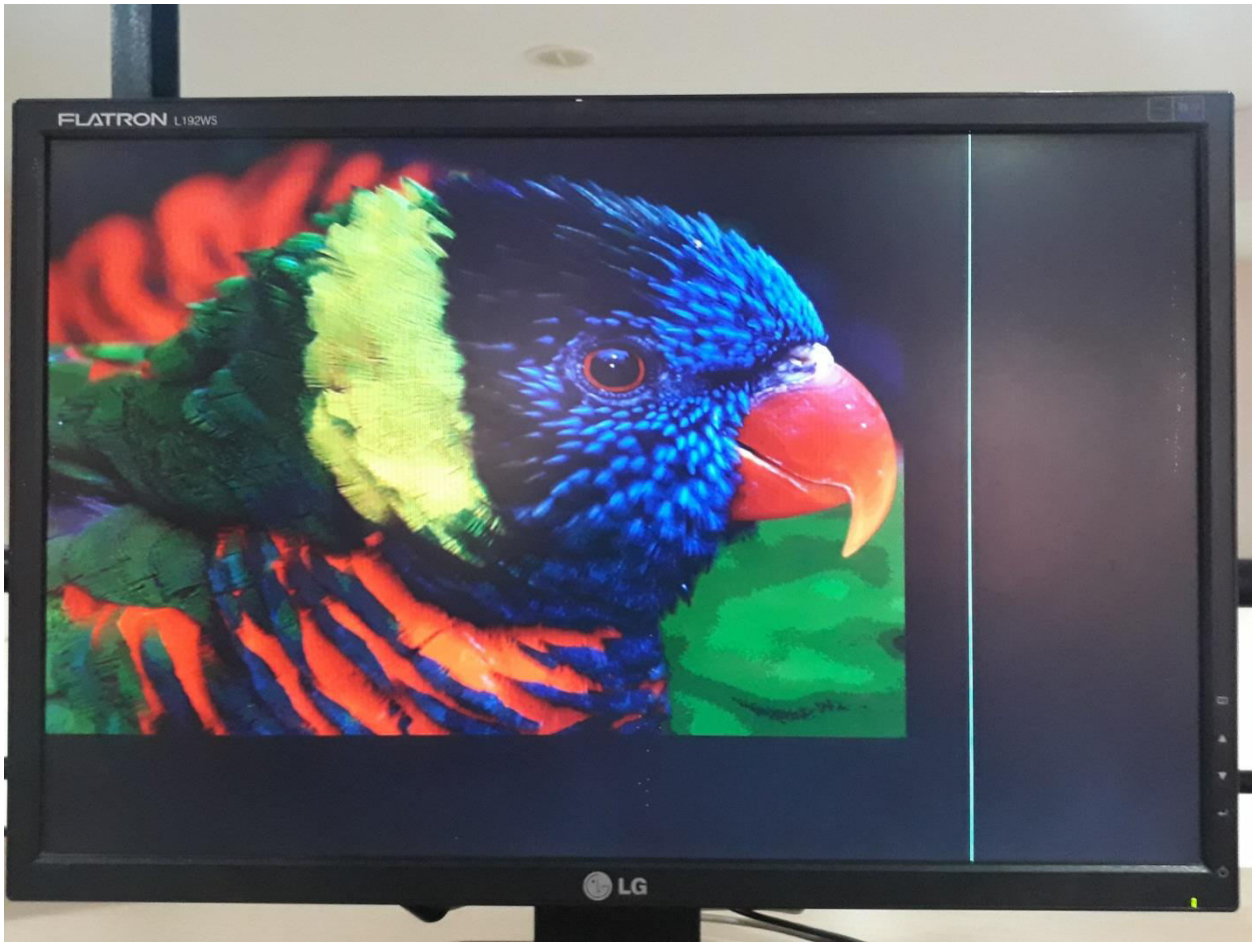
All user specified timing constraints are met.



3. Implementation






FLATRON L192WS
LG