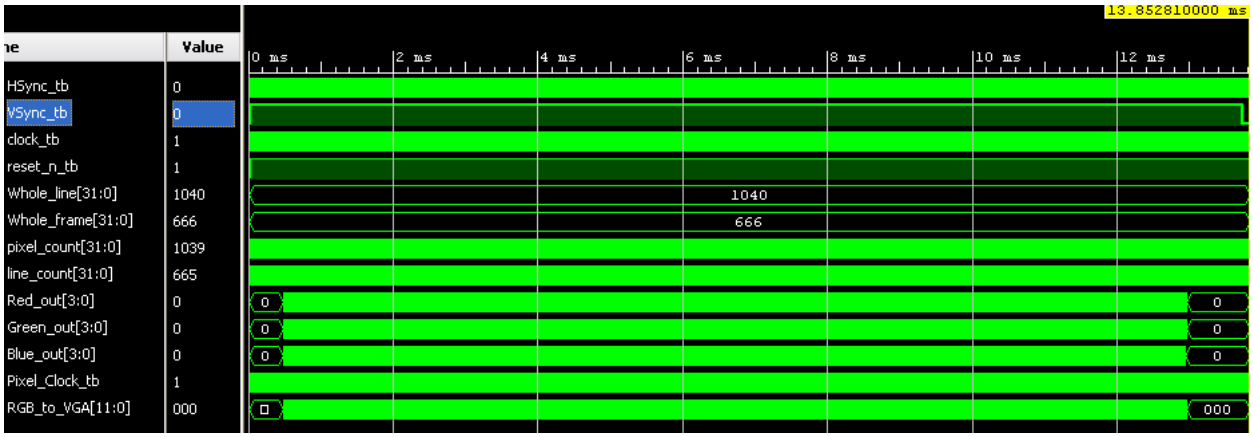
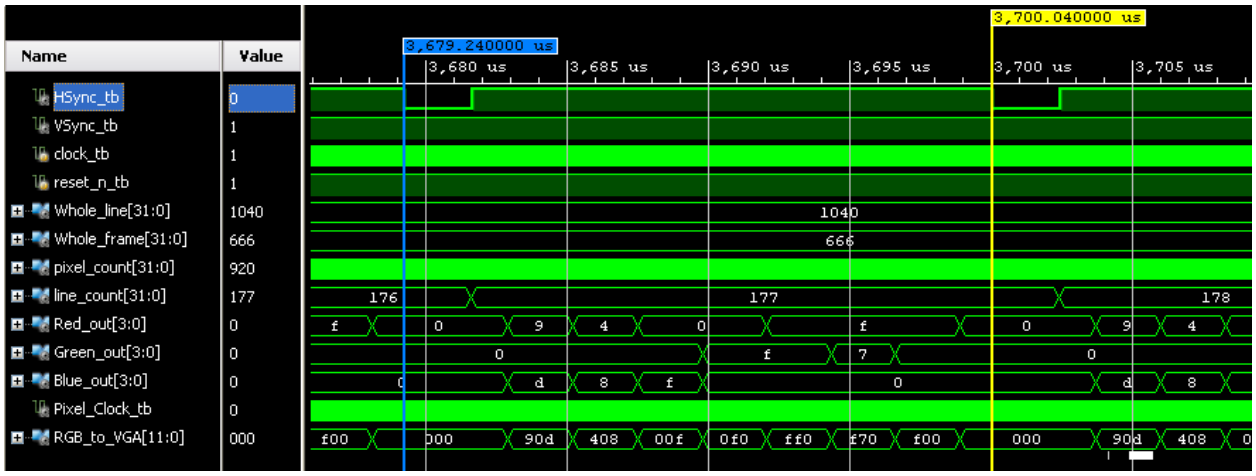
1. Simulation

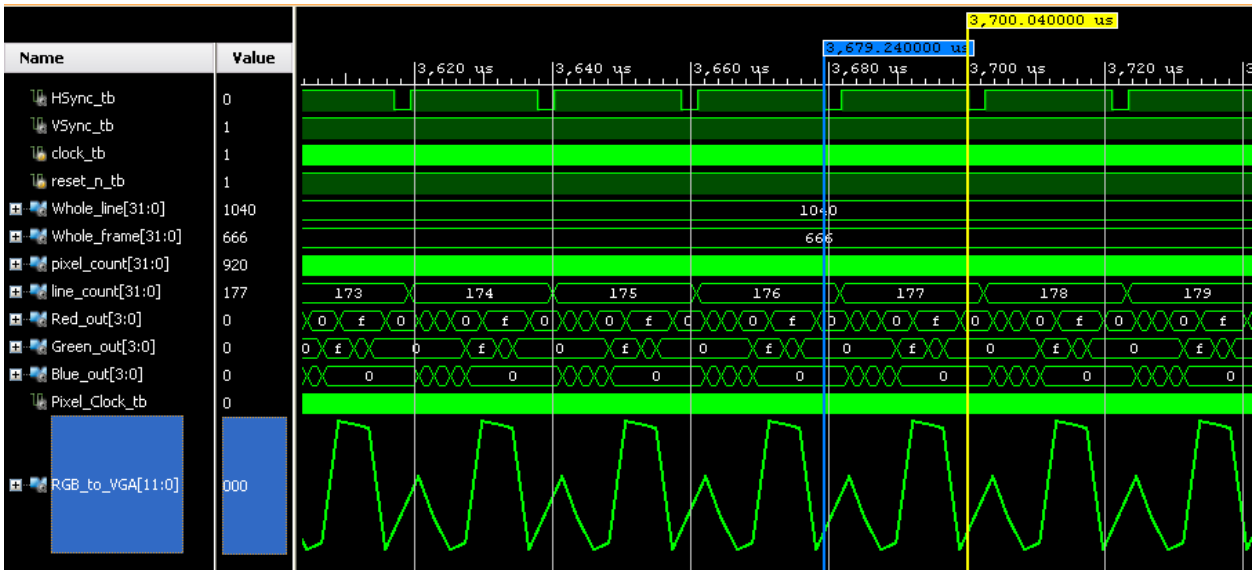
1.1. VSync



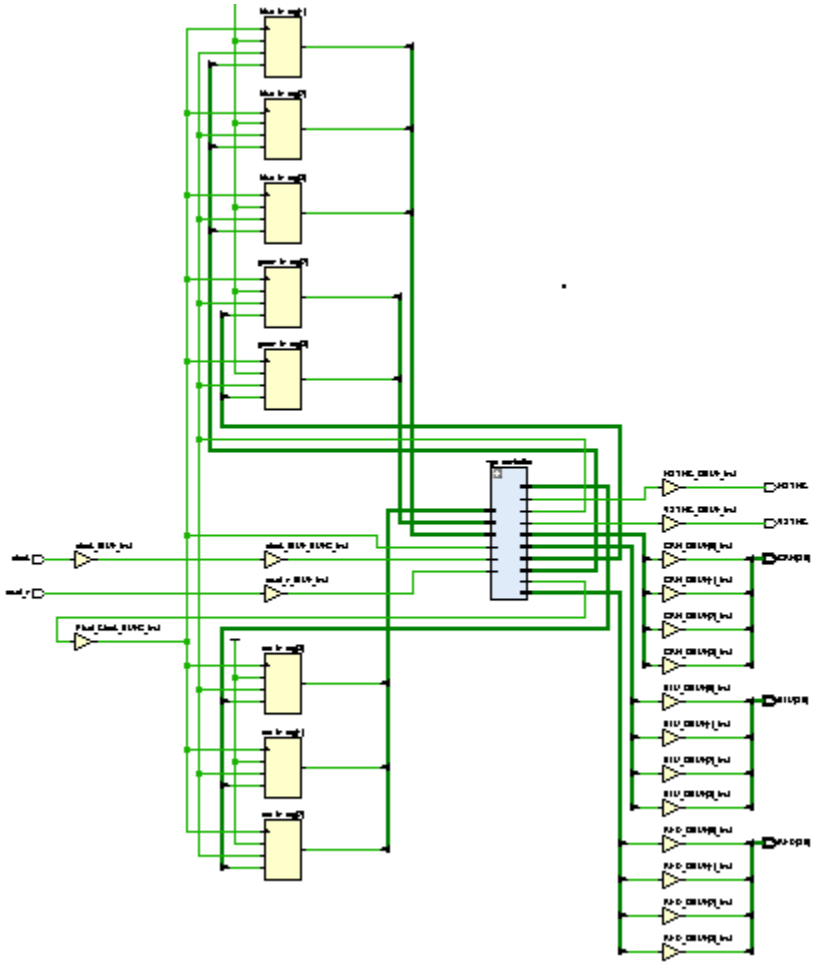
1.2 . HSync

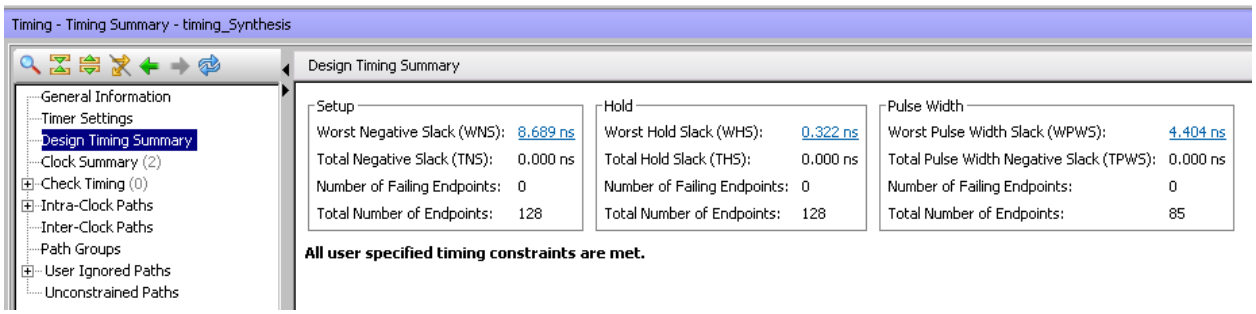


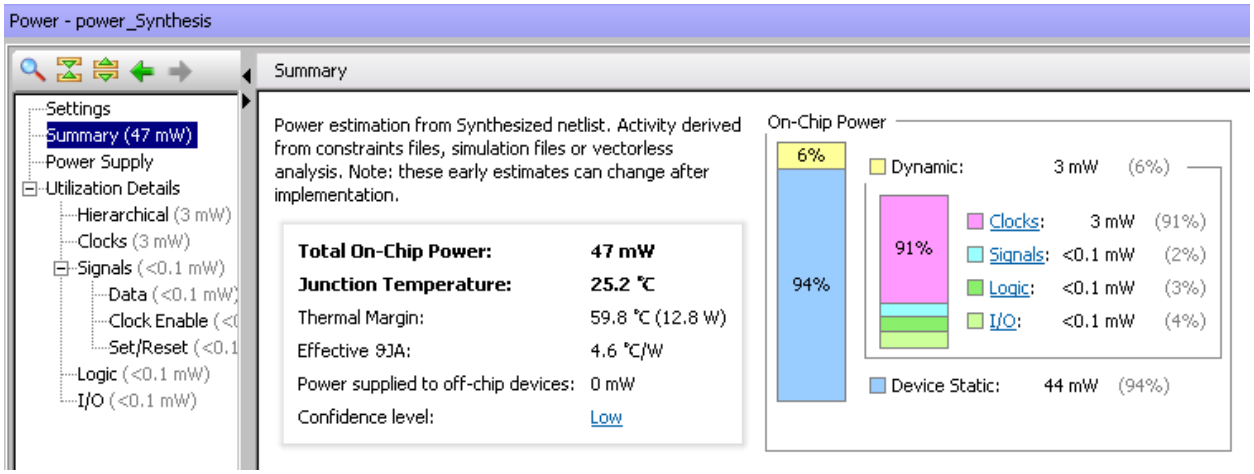
1.3. VGA RGB data as Analog

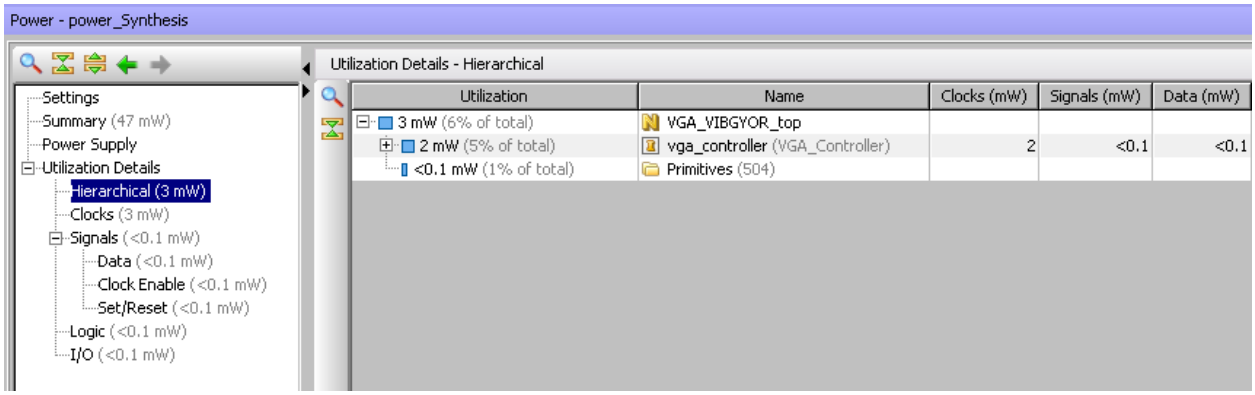


2. Synthesis

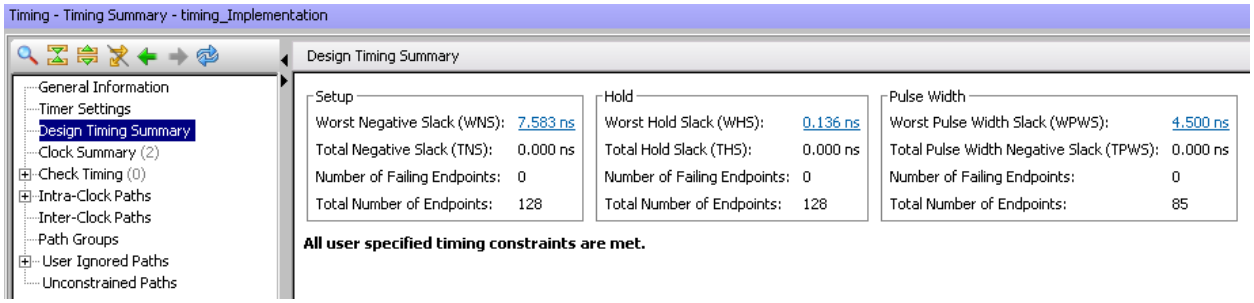


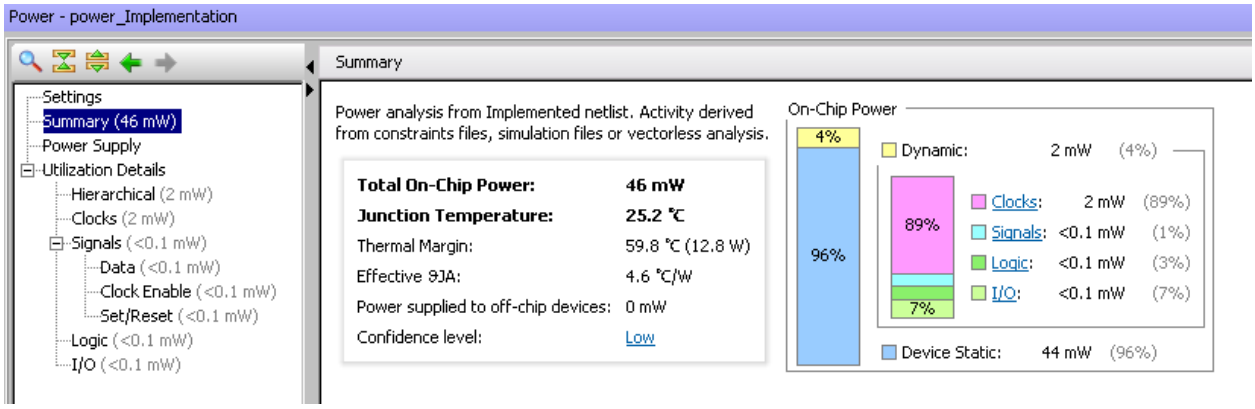

Timing - Timing Summary - timing_Synthesis
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Path Groups
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): 8.689 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 128
Hold
Worst Hold Slack (WHS): 0.322 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 128
Pulse Width
Worst Pulse Width Slack (WPWS): 4.404 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 85
All user specified timing constraints are met.

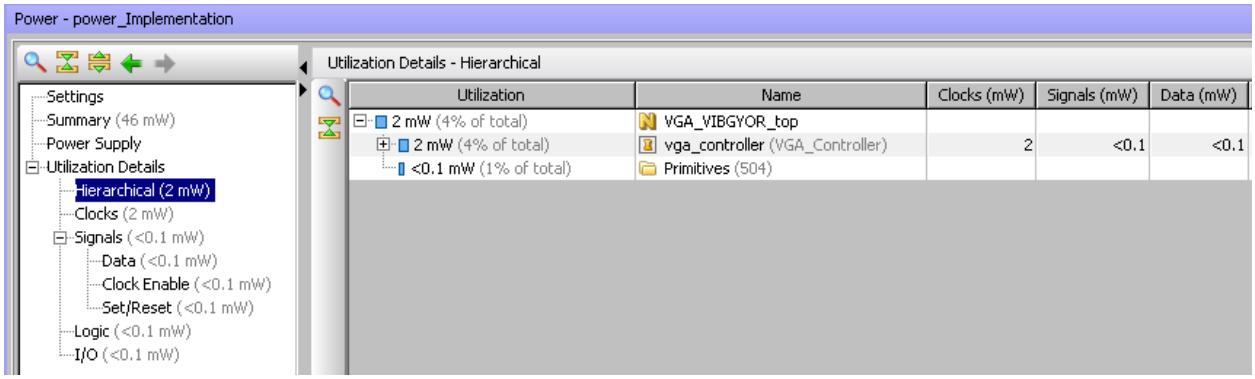

Power - power_Synthesis
Settings
Summary (47 mW)
Power Supply
Utilization Details
Hierarchical (3 mW)
Clocks (3 mW)
Signals (<0.1 mW)
Data (<0.1 mW)
Clock Enable (<0
Set/Reset (<0.1
Logic (<0.1 mW)
I/O (<0.1 mW)
Summary
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.
Total On-Chip Power: 47 mW
Junction Temperature: 25.2 °C
Thermal Margin: 59.8 °C (12.8 W)
Effective ϑJA: 4.6 °C/W
Power supplied to off-chip devices: 0 mW
Confidence level: Low
On-Chip Power
6%
94%
Dynamic: 3 mW (6%)
91%
Clocks: 3 mW (91%)
Signals: <0.1 mW (2%)
Logic: <0.1 mW (3%)
I/O: <0.1 mW (4%)
Device Static: 44 mW (94%)


Power - power_Synthesis
Settings
Summary (47 mW)
Power Supply
Utilization Details
Hierarchical (3 mW)
Clocks (3 mW)
Signals (<0.1 mW)
Data (<0.1 mW)
Clock Enable (<0.1 mW)
Set/Reset (<0.1 mW)
Logic (<0.1 mW)
I/O (<0.1 mW)
Utilization Details - Hierarchical
Utilization
Name
Clocks (mW)
Signals (mW)
Data (mW)
3 mW (6% of total)
VGA_VIBGYOR_top
2 mW (5% of total)
vga_controller (VGA_Controller)
2
<0.1
<0.1
<0.1 mW (1% of total)
Primitives (504)

3. Implementation







FLATRON