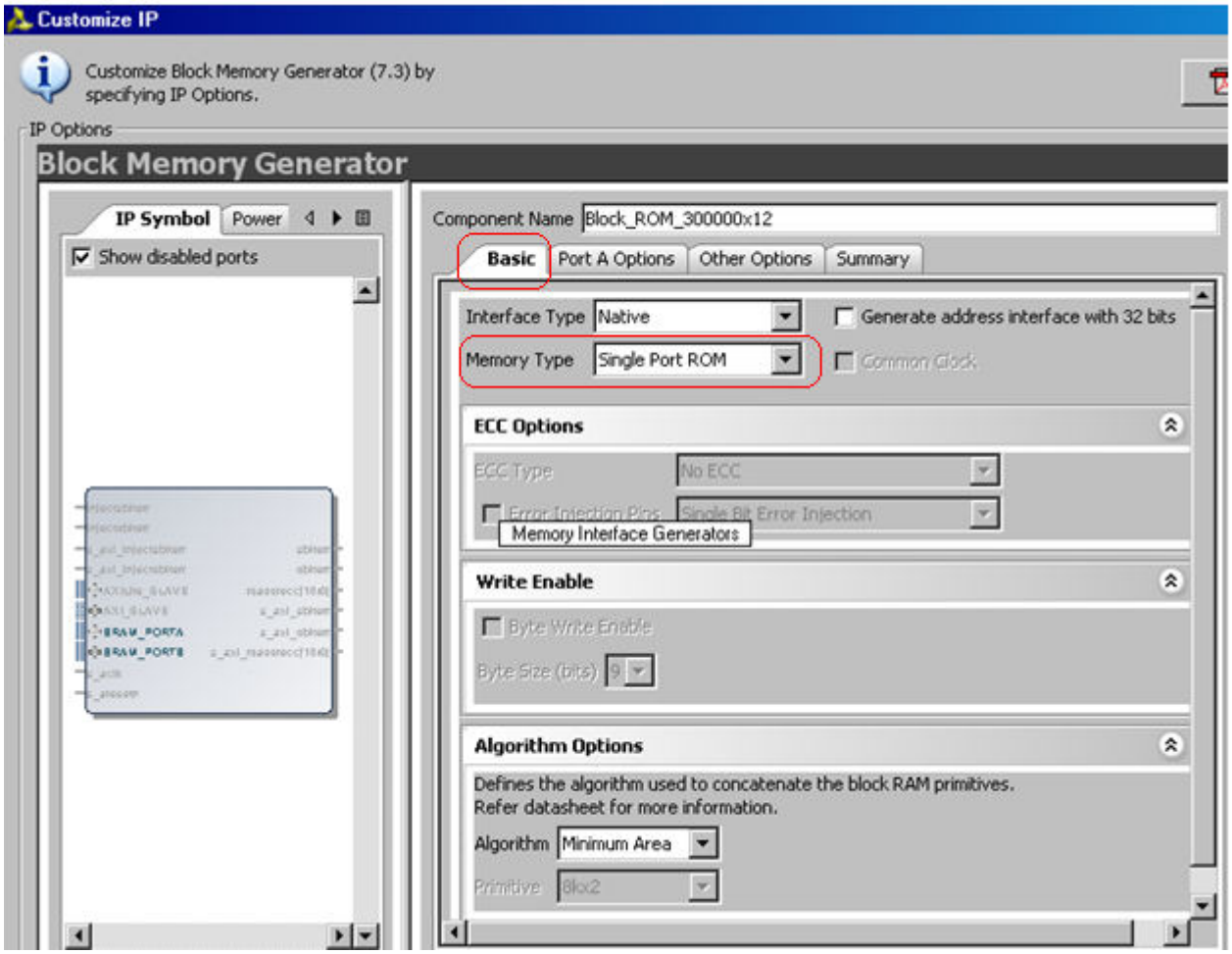
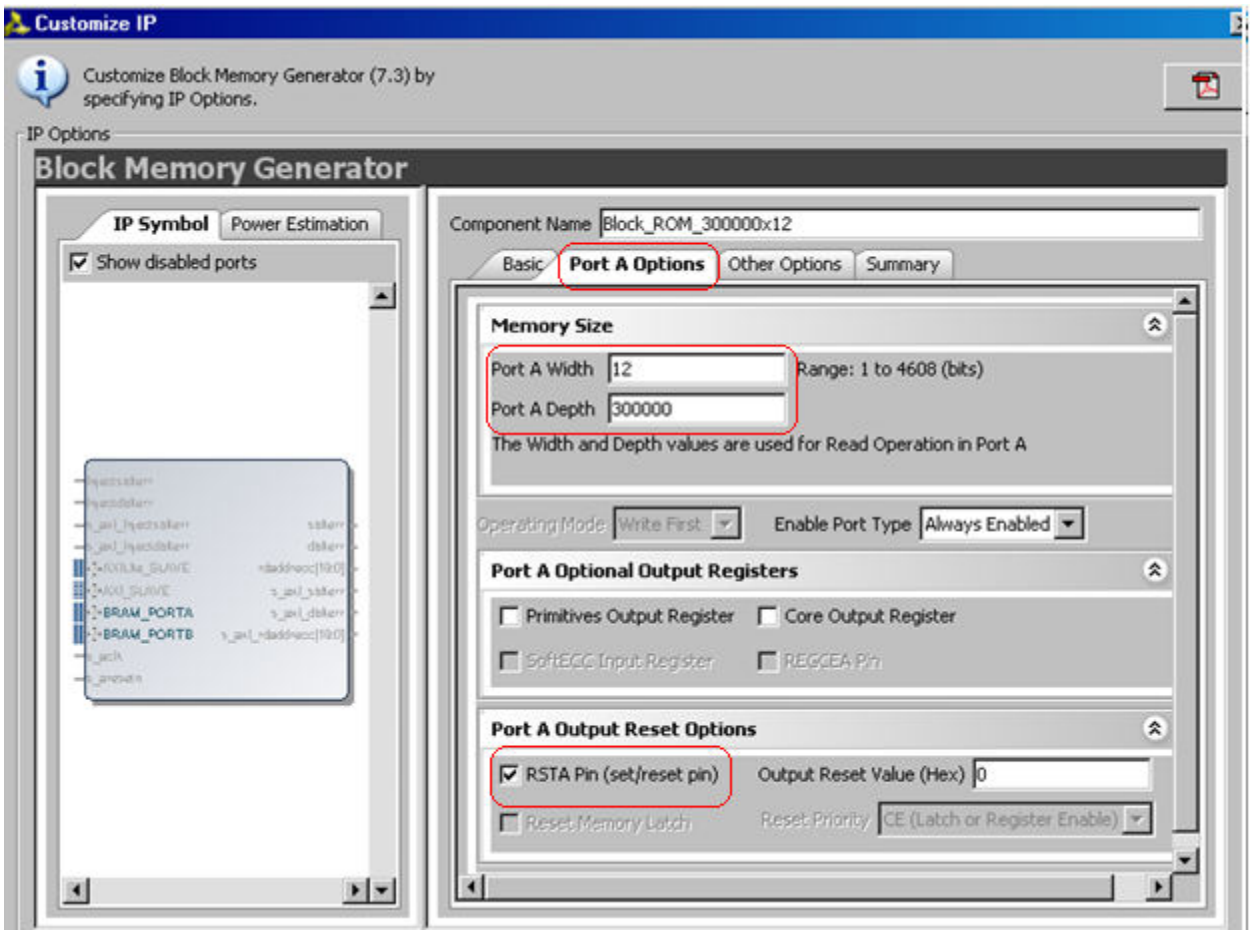
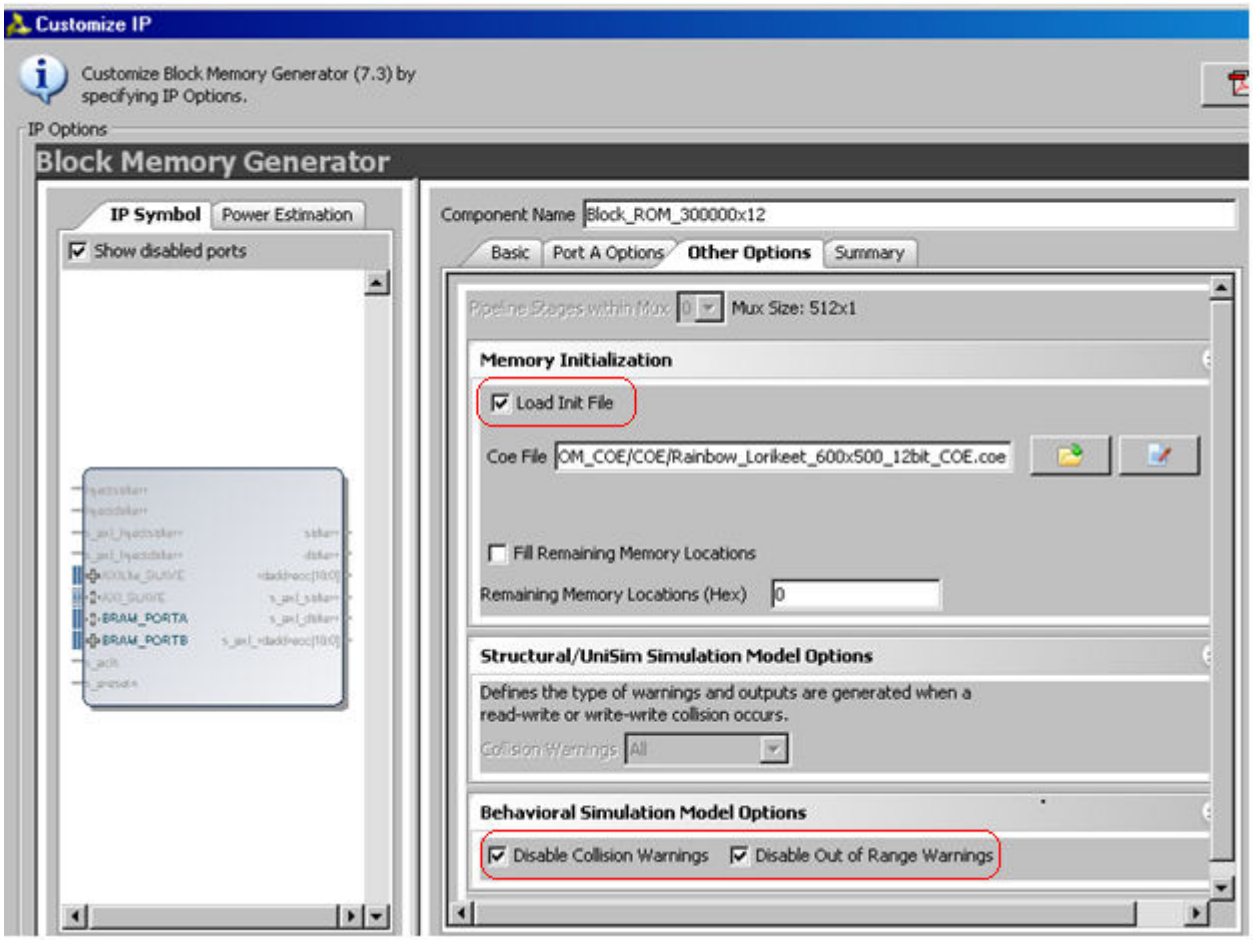
1. Block ROM Instantiation

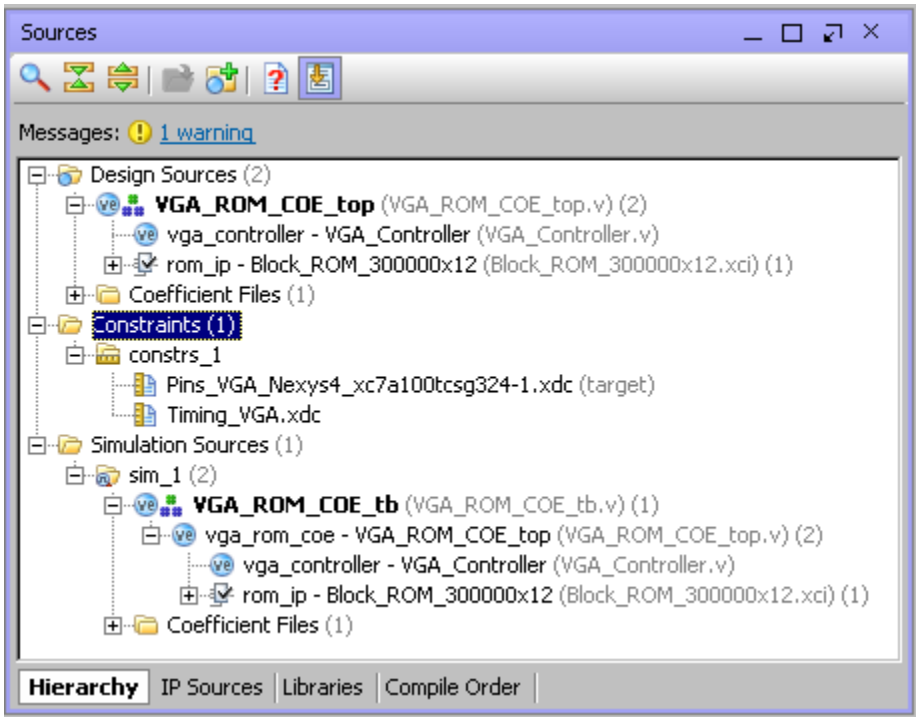
Vivado → Project Manager → IP Catalog →
Memories & Storage Elements →
RAMs & ROMs → Block Memory Generator




Customize IP
Customize Block Memory Generator (7.3) by specifying IP Options.
IP Options
Block Memory Generator
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
BRAM_PORTB
Component Name
Block_ROM_300000x12
Basic
Port A Options
Other Options
Summary
Memory Size
Port A Width
12
Range: 1 to 4608 (bits)
Port A Depth
300000
The Width and Depth values are used for Read Operation in Port A
Operating Mode
Write First
Enable Port Type
Always Enabled
Port A Optional Output Registers
Primitives Output Register
Core Output Register
SoftECC Input Register
REGCEA Pin
Port A Output Reset Options
RSTA Pin (set/reset pin)
Output Reset Value (Hex)
0
Reset Memory Latch
Reset Priority
CE (Latch or Register Enable)

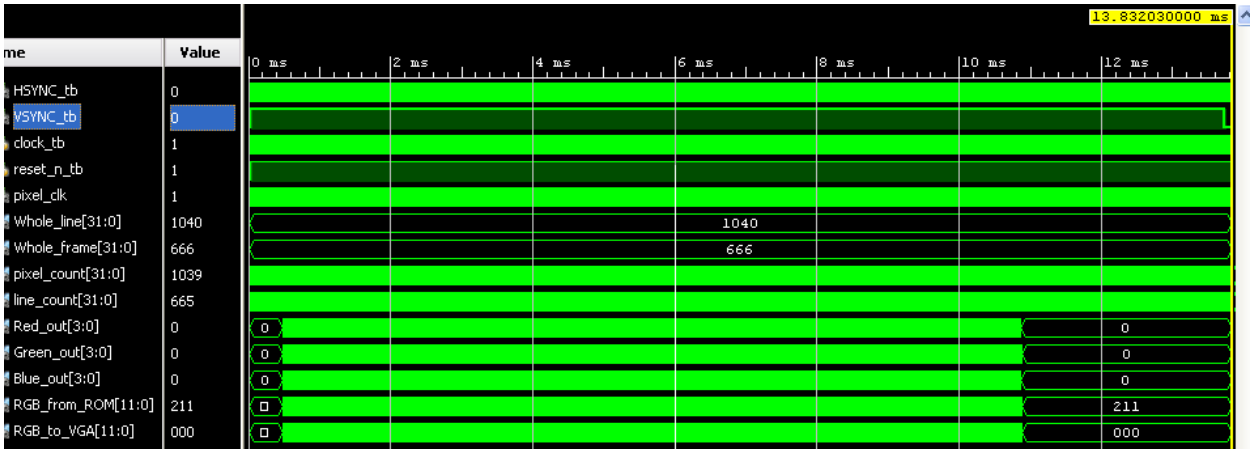

Customize IP
Customize Block Memory Generator (7.3) by specifying IP Options.
IP Options
Block Memory Generator
IP Symbol
Power Estimation
Show disabled ports
BRAM_PORTA
BRAM_PORTB
Component Name
Block_ROM_300000x12
Basic
Port A Options
Other Options
Summary
Pipeline Stages within Mux
Mux Size: 512x1
Memory Initialization
Load Init File
Coe File
OM_COE/COE/Rainbow_Lorikeet_600x500_12bit_COE.coe
Fill Remaining Memory Locations
Remaining Memory Locations (Hex)
0
Structural/UniSim Simulation Model Options
Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.
Collision Warnings
All
Behavioral Simulation Model Options
Disable Collision Warnings
Disable Out of Range Warnings

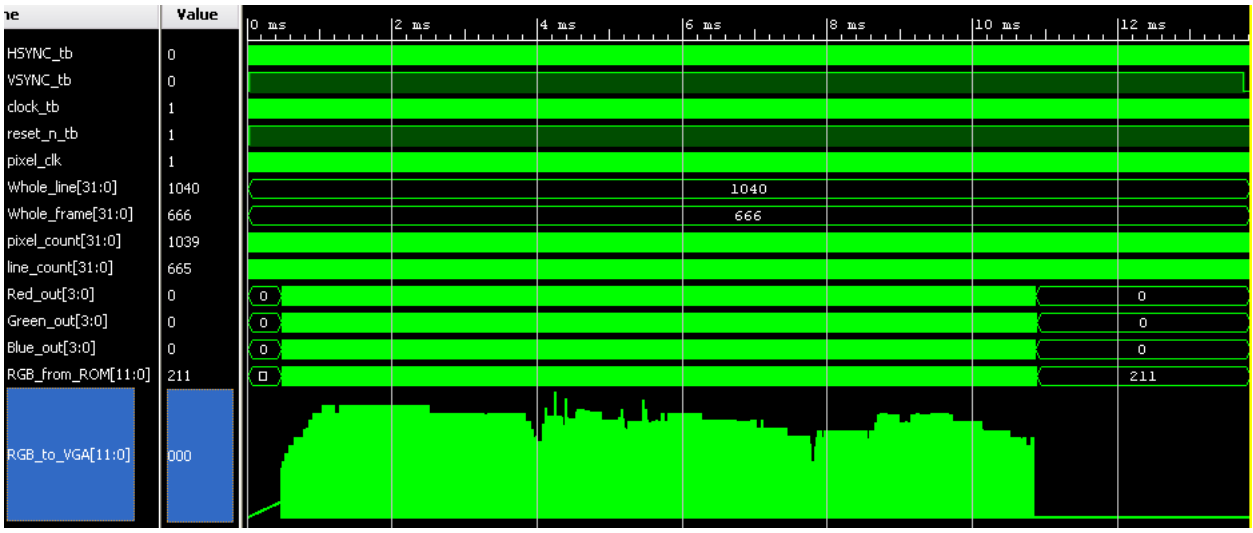
2. Project Hierarchy



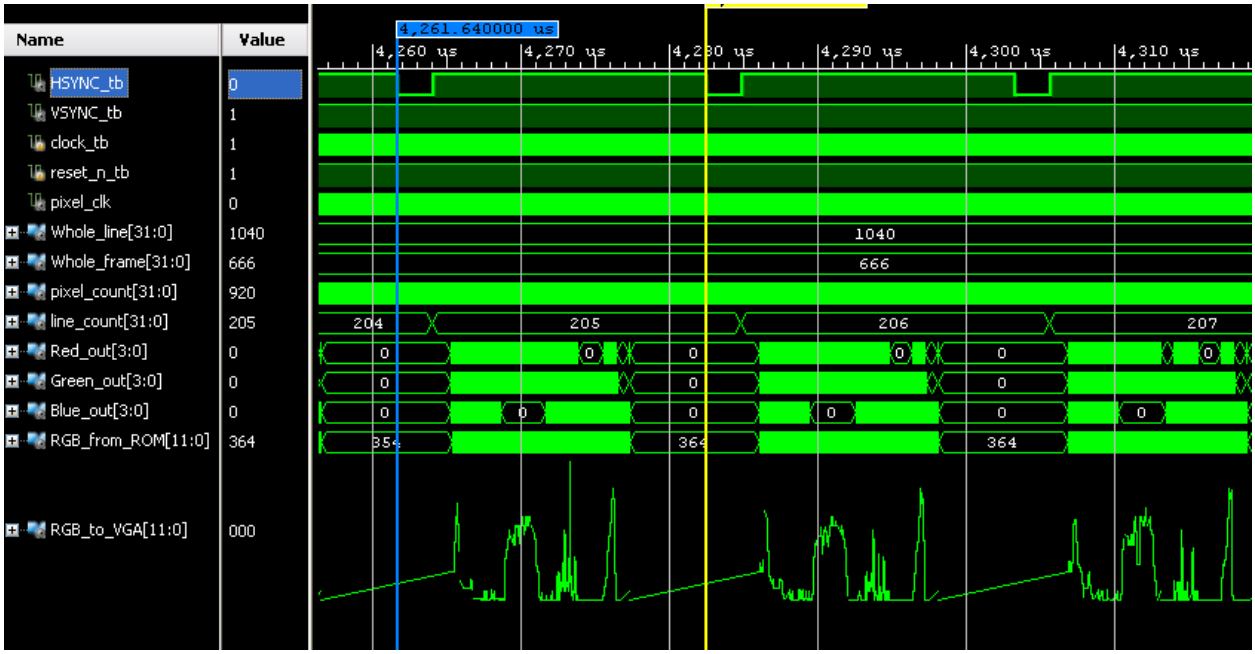
3. Simulation

3.1. Vsync

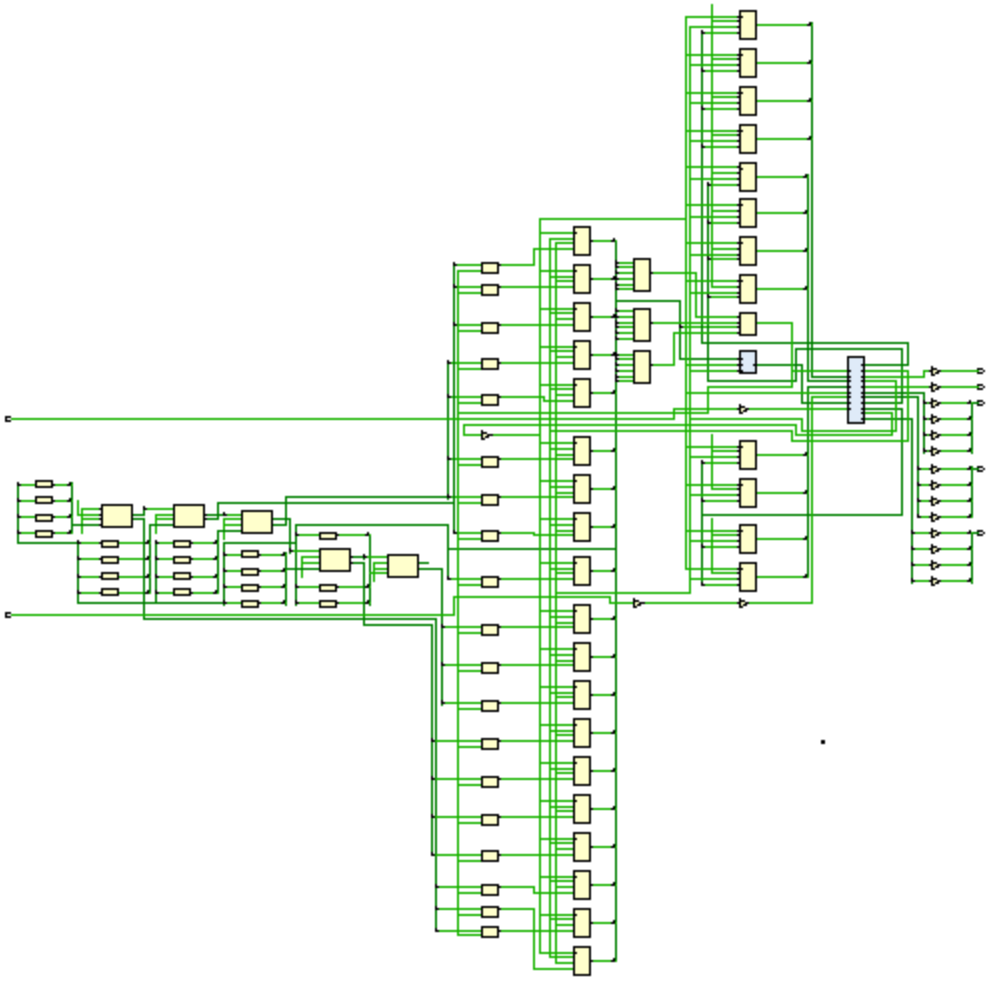




3.2. Hsync


Name
Value
HSYNC_tb
VSYNC_tb
clock_tb
reset_n_tb
pixel_clk
Whole_line[31:0]
Whole_frame[31:0]
pixel_count[31:0]
line_count[31:0]
Red_out[3:0]
Green_out[3:0]
Blue_out[3:0]
RGB_from_ROM[11:0]
RGB_to_VGA[11:0]
0
1
1
1
0
1040
666
920
205
0
0
0
364
000
4,261.640000 us
4,260 us
4,270 us
4,280 us
4,290 us
4,300 us
4,310 us
1040
666
204
205
206
207
364

4. Synthesis



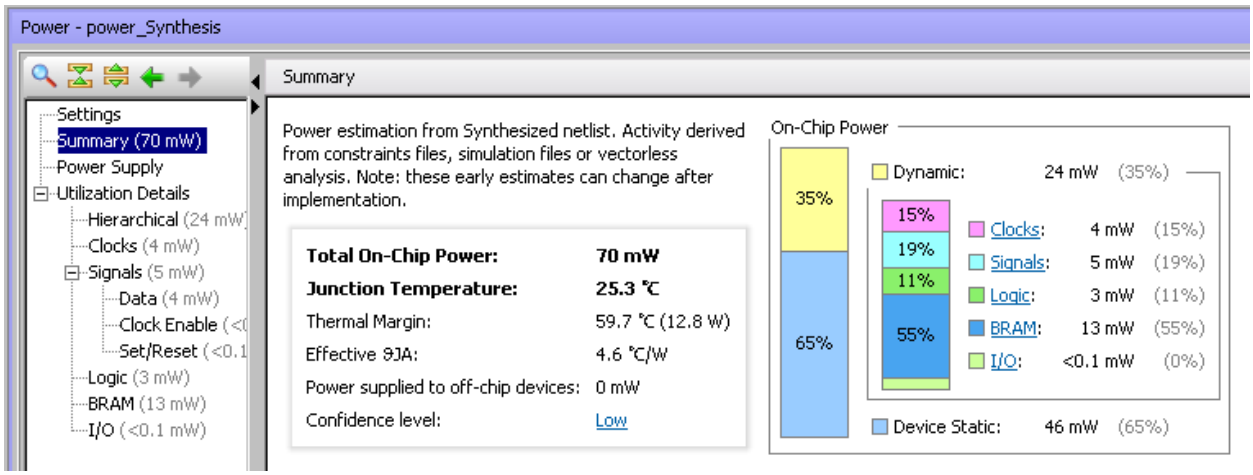
Timing - Timing Summary - timing_synthesis

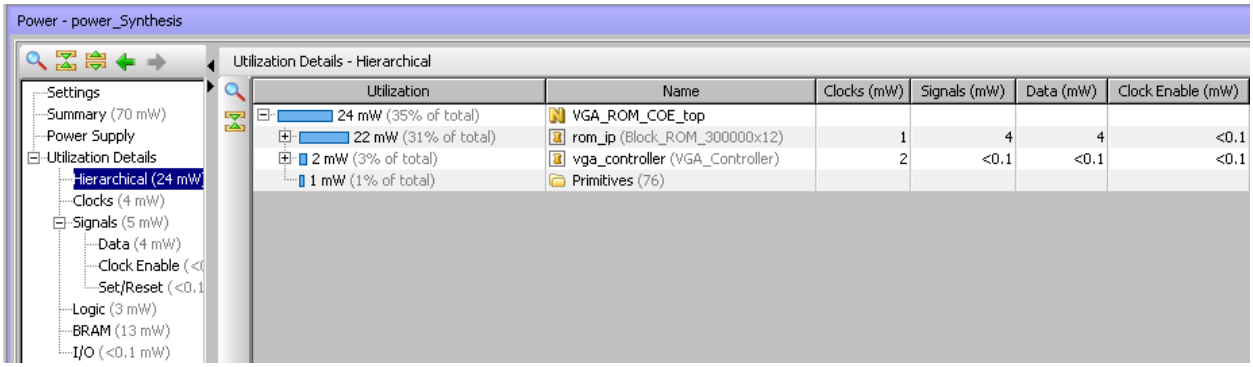
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (1)
Intra-Clock Paths
Inter-Clock Paths
Path Groups
User Ignored Paths
Unconstrained Paths

Design Timing Summary

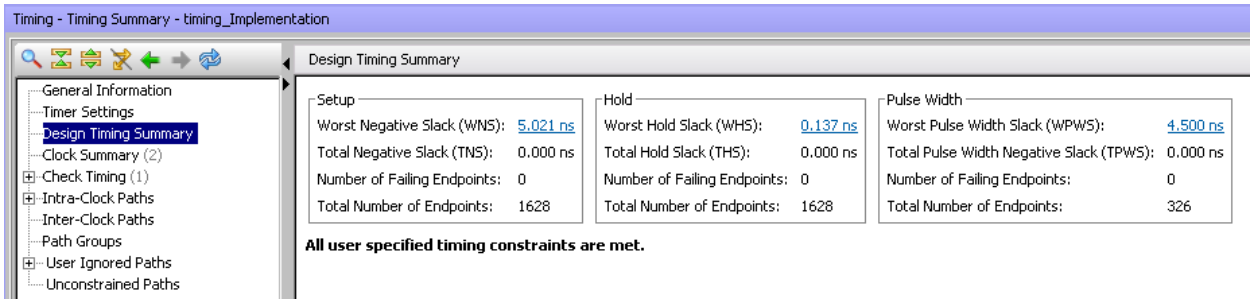
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.689 ns	Worst Hold Slack (WHS):	0.246 ns	Worst Pulse Width Slack (WPWS):	4.404 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1628	Total Number of Endpoints:	1628	Total Number of Endpoints:	326

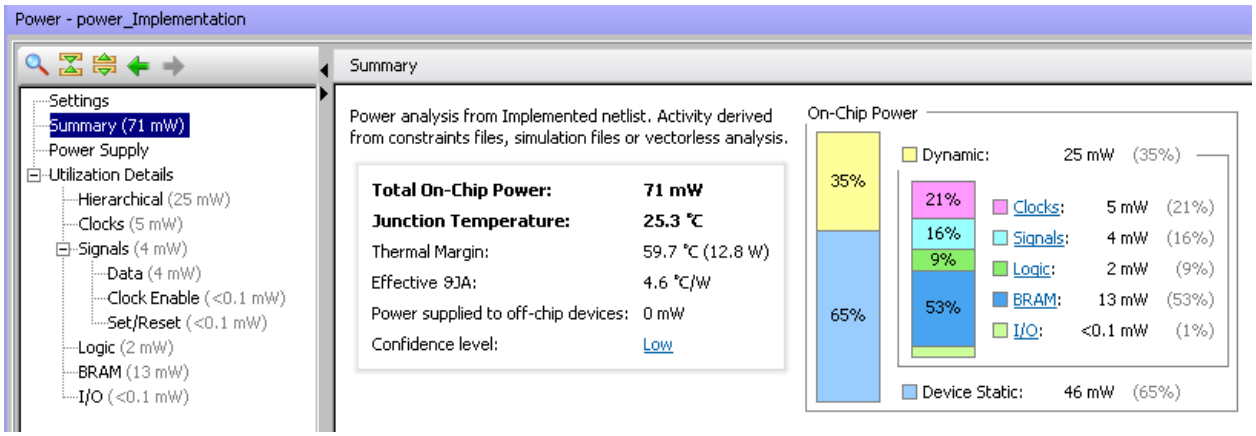
All user specified timing constraints are met.

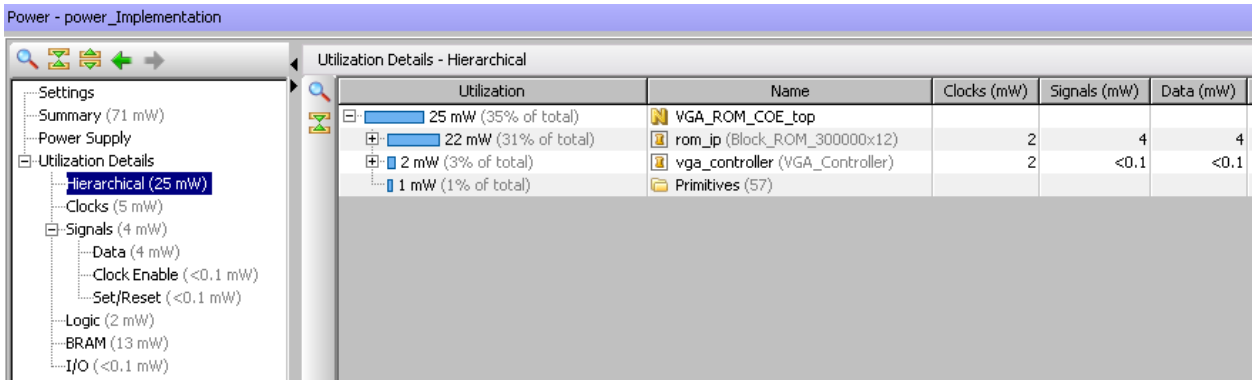

Power - power_Synthesis
Settings
Summary (70 mW)
Power Supply
Utilization Details
Hierarchical (24 mW)
Clocks (4 mW)
Signals (5 mW)
Data (4 mW)
Clock Enable (<0
Set/Reset (<0.1
Logic (3 mW)
BRAM (13 mW)
I/O (<0.1 mW)
Summary
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.
Total On-Chip Power: 70 mW
Junction Temperature: 25.3 °C
Thermal Margin: 59.7 °C (12.8 W)
Effective θJA: 4.6 °C/W
Power supplied to off-chip devices: 0 mW
Confidence level: Low
On-Chip Power
35%
65%
Dynamic: 24 mW (35%)
15%
19%
11%
55%
Clocks: 4 mW (15%)
Signals: 5 mW (19%)
Logic: 3 mW (11%)
BRAM: 13 mW (55%)
I/O: <0.1 mW (0%)
Device Static: 46 mW (65%)

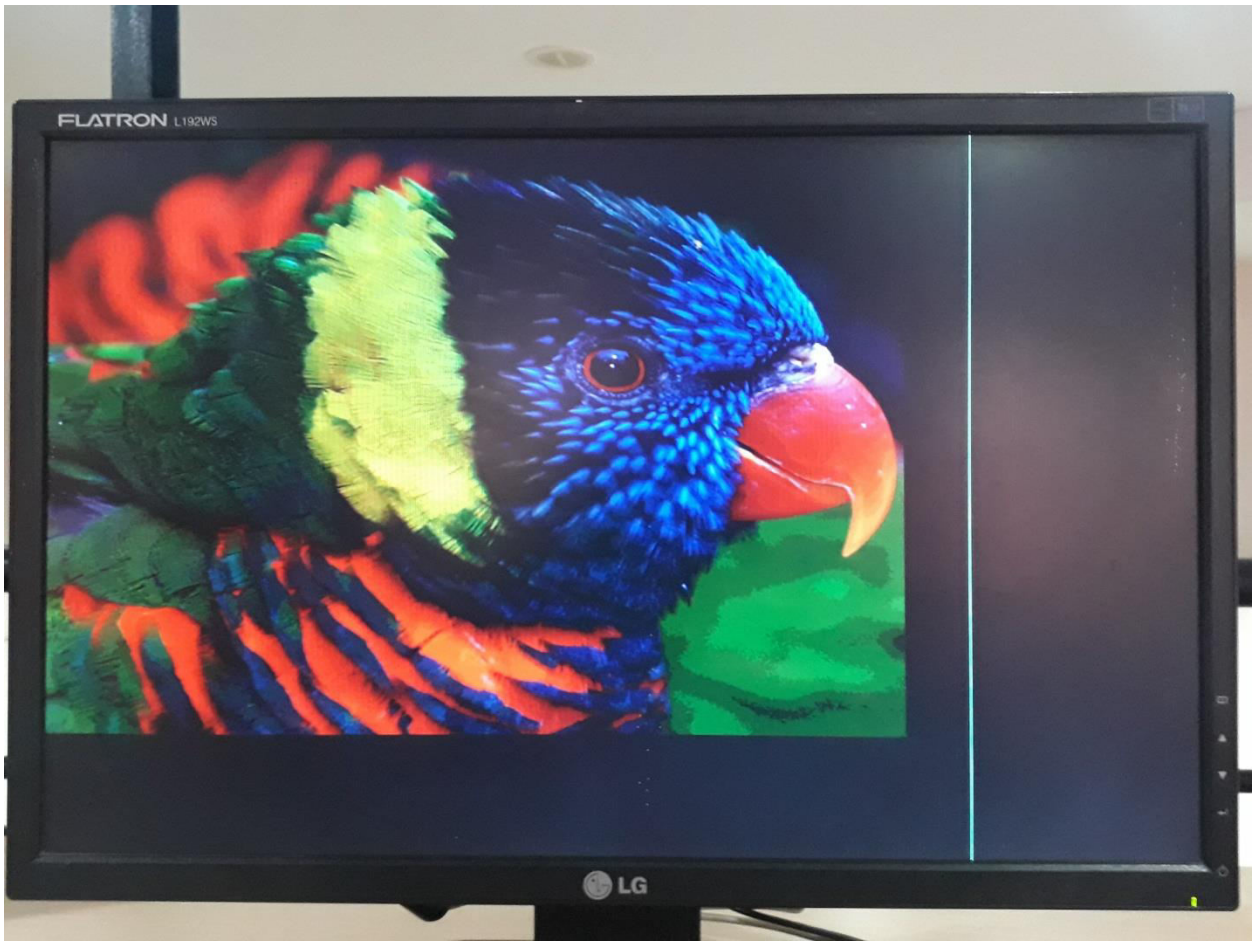

Power - power_Synthesis
Settings
Summary (70 mW)
Power Supply
Utilization Details
Hierarchical (24 mW)
Clocks (4 mW)
Signals (5 mW)
Data (4 mW)
Clock Enable (<0
Set/Reset (<0.1
Logic (3 mW)
BRAM (13 mW)
I/O (<0.1 mW)
Utilization Details - Hierarchical
Utilization
Name
Clocks (mW)
Signals (mW)
Data (mW)
Clock Enable (mW)
24 mW (35% of total)
VGA_ROM_COE_top
22 mW (31% of total)
rom_ip (Block_ROM_300000x12)
1
4
4
<0.1
2 mW (3% of total)
vga_controller (VGA_Controller)
2
<0.1
<0.1
<0.1
1 mW (1% of total)
Primitives (76)

5. Implementation








FLATRON L192WS
LG