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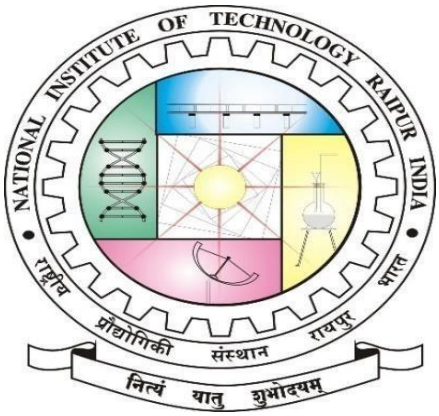

Department of Electronics and Communication Engineering

Summer training report

On

IMPLEMENTATION OF NOVEL FULL ADDER USING DIFFERENT TECHNOLOGY NODES

Internship undertaken under the supervision and guidance of :

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Current year of study : Fourth year

DECLARATION

I certify that

a) The work contained in this report is original and has been done by me under the guidance of my mentor/supervisor(s).

b) The work has not been submitted to any other Institute for any degree or diploma.

c) I have followed the guidelines provided by the Department in preparing the report.

d) Whenever I have used materials (data, theoretical analysis, figures, and text) from other sources, I have given due credit to them by citing them in the text of the report and giving their details in the reference.

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ABSTRACT

This training program aims to provide comprehensive instruction and hands-on experience in Digital design using software tools like Ltspice, Hspice, etc. The design of a 20-transistor novel full adder (NFA) with a new architecture employing CMOS transistors is presented in this work. The feature of the new topology is that the input carry of the full adder has to traverse through the single transistor, which enhances the speed of the full adder. Carry propagation is a critical factor in determining the speed of multi-bit adders like carry-choose adders, carry-save adders, and ripple carries adders, hence input carry is chosen above the other two inputs. The proposed NFA eliminates the complex XOR/XNOR functions for the generation of sum and output carry. The design also addresses the power factor, which is reduced by employing a NOR topology in the first stage of the complete adder and designing it using CMOS at 16nm,22nm,32nm, and low supply voltage. The circuit's different topology is designed so that the number of 'n' and 'p' type CMOSs is balanced. The proposed NFA is designed and extensively simulated at three technology nodes by testing its performance with various supply voltages like 0.6 V, 1 V, 1.2 V, and 1.5 V using the Ltspice tool

Keywords: Digital Design, Full adder, Carry propagate, Ltspice

ACKNOWLEDGMENT

Every project, big or small, succeeds in large part because of the efforts of a group of outstanding people who have always offered beneficial advice or given a hand. I am grateful for all of the people who have contributed to the success of our project by providing inspiration, support, and guidance. We are highly indebted to our guide Mr. Chitrakant Sahu Sir for his invaluable help and guidance during the project. We acknowledge his constant encouragement by giving his critiques of our work. We are grateful to him for having given us the support and confidence. Our special thanks go to Dr.Toshanlal Meenpal, Head of the Department of Electronics and Communication Engineering, NIT Raipur, for providing us with the best facilities in the Department. We'd like to express our gratitude to all of our teachers for providing a firm foundation for our studies and subsequent research. They have been tremendous sources of inspiration for us, and we sincerely appreciate it. We'd also like to express our gratitude to our friends, particularly my classmates, for all of the smart and thought-provoking talks that inspired us to think beyond the obvious. Last but not least, I'd like to express my gratitude to my parents for teaching me the value of hard work.

CONTENTS

a) History of CMOS

Before CMOS, there was NMOS. An NMOS gate consisted of a network of N-transistors between the output and VSS and a resistor between the output and VDD, but in NMOS the P-transistor was simply used as a resistor.

If the logic enabled current to flow to the ground, that would pull the output level down against the resistor. If the logic blocked the current, the resistor/transistor would pull the output up towards VDD.

There were two big problems with this approach. First, there are paths from VDD to VSS when the network of NMOS transistors allows current to pass, so a lot of leakage current.

The other issue was that the switching speed was limited due to the resistor. When the network of NMOS transistors blocked current, the output was only pulled up slowly due to the resistor.

The solution: CMOS. Replace the P-transistor pullup resistor/transistor with a complementary network of P-transistors

When the network of N-transistors allowed the current to pass, the network of P-transistors did not, so the output would be quickly pulled down to Vss. When the network of N-transistors blocked the current, the network of P-transistors would let it pass and the output would quickly be pulled up to VDD.

The C in CMOS stands for “complementary” since the networks of P and N transistors were complementary graphs in the mathematical sense. When one network had transistors in parallel, the other would have them in series (and vice-versa).

WHY CMOS?

The idea of MOSFETs was patented by J. E. Lilienfeld in the early 1930 s well before the invention of the bipolar transistor. Owing to fabrication limitations, however, MOS technologies became practical only much later, in the early 1960s, with the first several generations producing only n-type transistors.

It was in the mid-1960s that complementary MOS (CMOS) devices (i.e., with both n-type and p-type were introduced, initiating a revolution in the semiconductor industry.

CMOS technologies rapidly captured the digital market: CMOS gates dissipated power only during switching and required very few devices, two attributes in sharp contrast to their bipolar or GaAs counterparts.

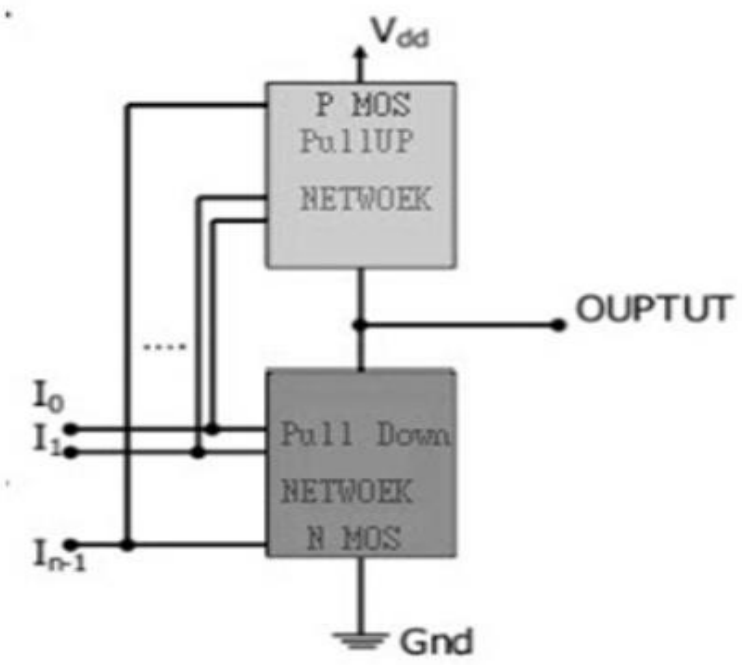
It was also soon discovered that the dimensions of MOS devices could be scaled down more easily than those of other types of transistors.

The next obvious step was to apply CMOS technology to analog design. The low cost of fabrication and the possibility of placing both analog and digital circuits on the same chip to improve the overall performance and/or reduce the cost of packaging made CMOS technology attractive.

However, MOSFETs were slower and noisier than bipolar transistors, finding limited application.

The principal force was device scaling because it continued to improve the speed of MOSFETs. The intrinsic speed of MOS transistors has increased by orders of magnitude in the past 60 years, exceeding that of bipolar devices even though the latter have also been scaled (but not as fast).

Another critical advantage of MOS devices over bipolar transistors is that the former can operate with lower supply voltages. In today’s technology, CMOS circuits run from supplies around 1 V and bipolar circuits around 2 V. The lower supplies have permitted a smaller power consumption for complex integrated circuits.



CMOS using Pull Up & Pull Down

fig:1

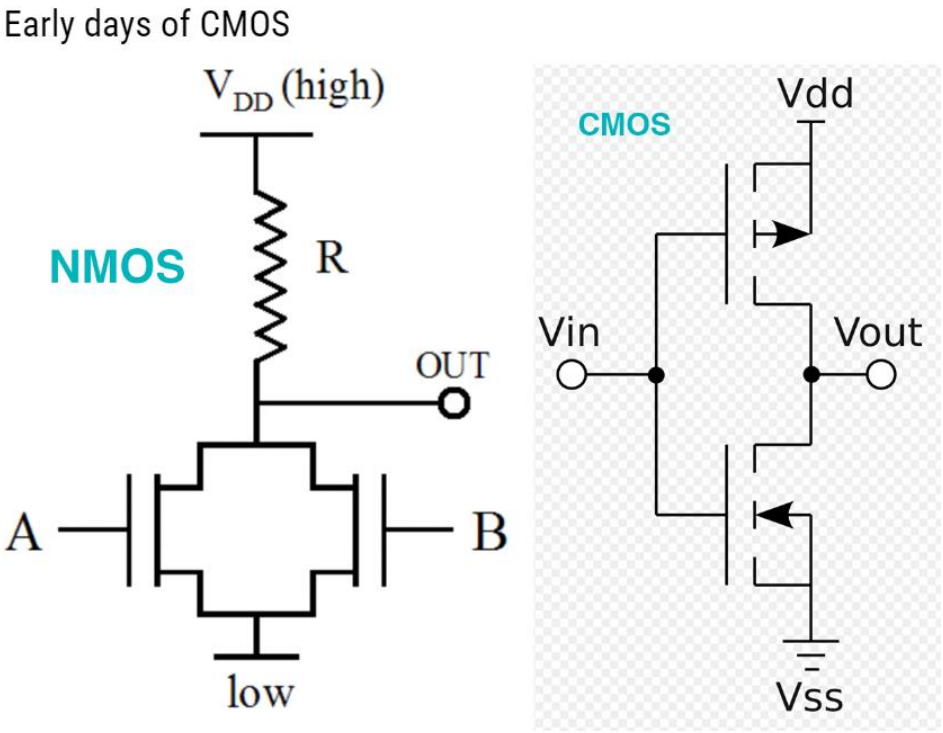


fig:2

B) CMOS working principle

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal that turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low-voltage power supply rail. Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail.

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern.

CMOS offers relatively high speed, low power dissipation, and high noise margins in both states and will operate over a wide range of source and input voltages (provided the source voltage is fixed).

C) CMOS SCALING

Currently, technology scaling has a threefold objective:

Reduce the gate delay by 30% (43% increase in frequency) Double the transistor density – Saving 50% of power (at 43% increase in frequency)

How is scaling achieved?

All the device dimensions (lateral and vertical) are reduced by 1/a– Concentration densities are increased by a– Device voltages are reduced by 1/a (not in all scaling methods) – Typically 1/a = 0.7 (30% reduction in the dimensions)

Table 1 shows the device scaling parameters:

Quantity	**Sensitivity**	**Constant field**	**Constant voltage**
Length	L	1/s	1/s
Gate oxide thickness	tox	1/s	1/s
Supply voltage	V	1/s	1
Threshold voltage	Vth	1/s	1
Doping density	Na, Nb	s	s^2
Width	W	1/s	1/s

Table 2 shows device scaling characteristics

Quantity	**sensitivity**	**Constant field**	**Constant voltage**
Area	WL	1/s^2	1/s^2
Oxide capacitance	CG	s.Cox	s.Cox
Drain current	Id	Id/s	s.Id
Power dissipation	p	P/s^2	s.P
Power density	p/Area	P/Area	S^3.(p/Area)

In VLSI, a technology node refers to a specific manufacturing process that governs the dimensions, transistor characteristics, and performance capabilities of integrated circuits. It encompasses parameters such as feature size, gate length, channel length, and interconnect density.

VLSI tech nodes are a measure of the smallest feature size in a semiconductor manufacturing process. They are typically expressed in nanometers (nm), and the smaller the number, the more advanced the process.

The first VLSI tech node was 10 micrometers (μm), which was introduced in the early 1970s. This was a major breakthrough, as it allowed for the integration of millions of transistors on a single chip.

Over the years, VLSI tech nodes have continued to shrink, with each new node offering significant improvements in performance, power efficiency, and density.

- The following is the list of important vlsi tech nodes

a) 10 μm (1970s): The first VLSI tech node. Used in early microprocessors and memory chips.

b) 3 μm (1980s): Introduced the use of polysilicon gates. Used in high-performance microprocessors and memory chips.

c) 1 μm (1990s): Introduced the use of copper interconnects. Used in high-performance microprocessors, memory chips, and graphics processors. metal gates. Used in high-performance microprocessors, memory chips, and graphics processors.

d) 22 nm (2010s): The current mainstream node. Used in a wide range of devices, including smartphones, tablets, laptops, and servers.

e) 14 nm (2010s): A leading-edge node used in high-performance microprocessors, memory chips, and graphics processors.

f) 7 nm (2010s): A leading-edge node used in high-performance microprocessors, memory chips, and graphics processors.

Advantages of Scaling :

The reduction in lateral dimensions of the MOSFET and interconnects size is known as 'scaling' of the geometric dimensions of the MOSFET.

The advantages of Scaling are as follows,

(1) Improved current driving capability improves the device characteristics.

(2) Due to small geometries the capacitance reduces.

(3) Improved interconnect technology reduces the RC delay.

(4) The multiple threshold devices due to scaling adjusts the active and stand by power trade-offs.

(5) The integration density improves due to single chip devices.

(6) Enhanced performance in terms of speed and power consumption.

(7) Cost of a chip decreases by twice.

Disadvantages of Scaling :

1) The power consumption per unit area increases as devices are scaled down. That means scaled devices run increasingly hot. This is a severe performance limitation for scaled devices.

2) The scaling leads to mistakes of having scale proportionally to zero dimension or to zero threshold voltages.

3) Since scaling reduces the carrier mobility, gain of the device reduces.

4) Due to reduction in conductor size, the current handling capacity of the device reduce. To solve this addition metal layers are necessary for more densely packed structure.

5) As the packing density per chip increases, due to higher power density, the device becomes very hot and needs forced cooling at the additional cost.

6) Higher fields also cause hot electron and oxide reliability problems.

e) Limitations Of CMOS

Following points summarize CMOS disadvantages over TTL and ECL:

1. Limited Speed: While CMOS can achieve high-speed operation, it may not match the extremely high speeds of technologies like ECL in certain applications.

2. The fabrication of CMOS process is more complex compared to some other logic families.

3. CMOS circuits are sensitive to variations in threshold voltage, which can be influenced by factors such as temperature and manufacturing process variations. This sensitivity may require additional design considerations.

4.A CMOS transistor typically has a lower breakdown voltage

SHORT CHANNEL EFFECTS

1) Drain Induced Barrier Lowering
2) Velocity saturation
3) Drain pinch through
4) Impact Ionization
5) Hot Electron Effect

1)Drain induced barrier lowering: When we apply a positive voltage to the drain of the short channel device, threshold voltage (Vt) will be reduced due to the depletion region under the drain region, and overall channel length will reduce, this is called Drain-induced barrier lowering (DIBL).it is also called as short channel effect in CMOS.

When we apply a positive voltage to the drain of a long-channel NMOS device, we observe no significant change in the value of Vt. But when we do the same for a short-channel NMOS device.

The physical origin of DIBL is the increase of the depletion layer due to a high value of VDS that reduces the equivalent channel length and consequently decreases the threshold voltage

2) velocity saturation: At the high lateral electric field elat that is equal to VDS/L, the velocity of the carrier ceases to increase linearly with the field strength is called Velocity saturation.

The velocity saturation results in lower Ids that which is expected at High VDS.

3)Impact ionization: Impact ionization is the process in a material by which one energetic charge carrier can lose energy by the creation of other charge carriers. In semiconductors, an electron (or hole) with enough kinetic energy can knock a bound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an electron hole pair.

4)Hot electron effect: When VDS is high, the electron near the gate will receive high kinetic energy, and some of these electrons might be trapped in gate oxide, which may damage the gate oxide or change Vt (threshold voltage). This is called a “Hot Electron Effect.” This leads to the deposition of negative charge on the gate which leads to an increase in threshold voltage by increasing flat band voltage. In addition, these hot carriers can rupture stable Si-H bonds creating fast interface states that degrade mosfet parameters such as gain.

a) Introduction to Ltspice

Ltspice is a free circuit simulator from the manufacturer Analog Devices that uses a mixture of Spice commands and circuit diagrams with a sizable library of passive and active components. The software also allows sub-circuits and Hierarchical circuits of any size, even from third-party sources to add components that are not currently available in the library. There is already a lot of support for the program and it always helps to have more if questions are answered vaguely online. Also, this tool is useful for testing out ideas that often use high current which requires plenty of safety factors when testing. This first post about this software will cover installation and getting started with drafting

a) Design of CMOS Inverter :

The term “CMOS” stands for “complementary-symmetry metal–oxide–semiconductor” which is pronounced as “ MOS”. CMOS is a type of MOSFET, where its fabrication process uses complementary & symmetrical P-type & N-type MOSFET pairs for logic functions. The main CMOS devices characteristics are consumption of low static power & high noise immunity. The inverter is accepted universally as the basic logic gate while performing a Boolean operation on a single i/p variable. A basic inverter circuit is used to accomplish a logic variable by complementing from A to A’.

CMOS INVERTER:

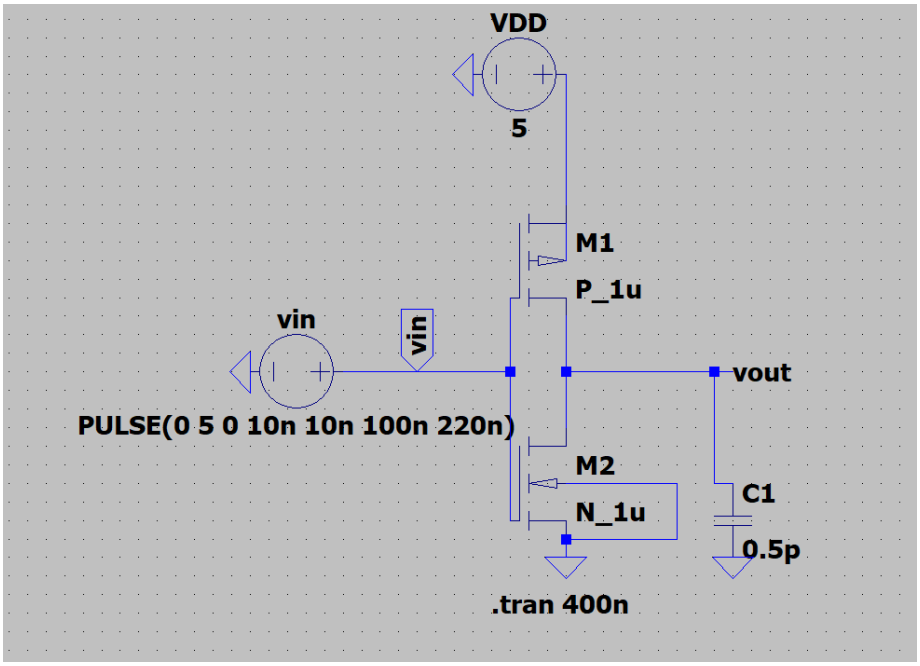


Fig:3

OUTPUT SIMULATIONS:

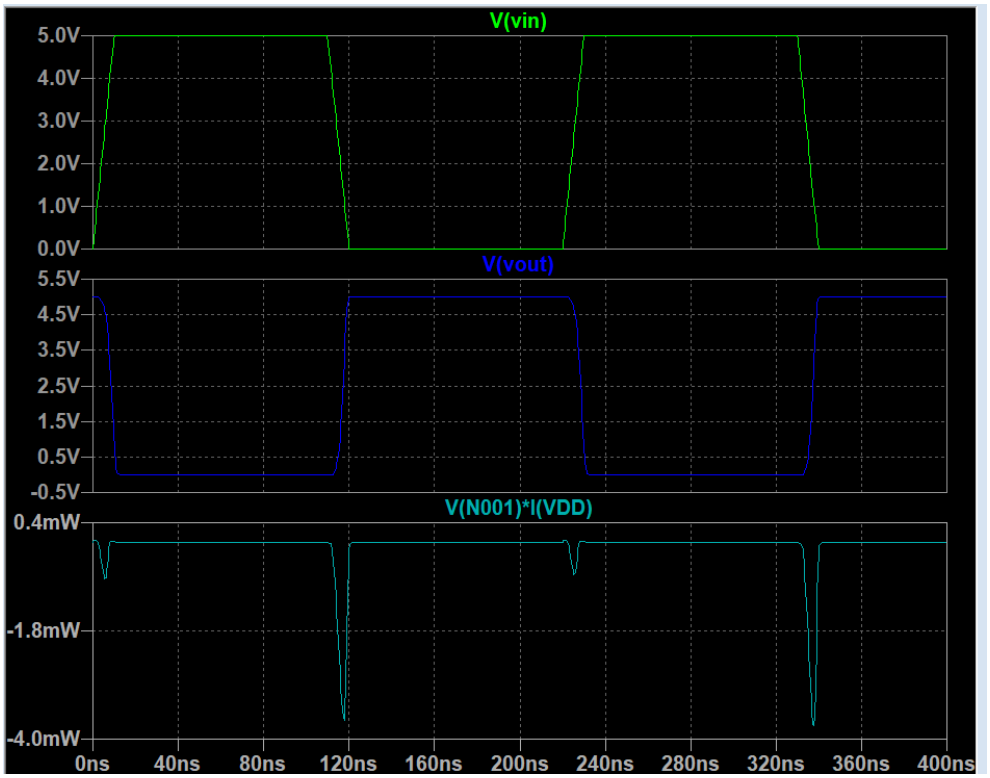


Fig:4

Long channel: This is the 1um technology node i,e channel length used for both the p and n type MOS are 1um.

Short channel CMOS inverter using 50n

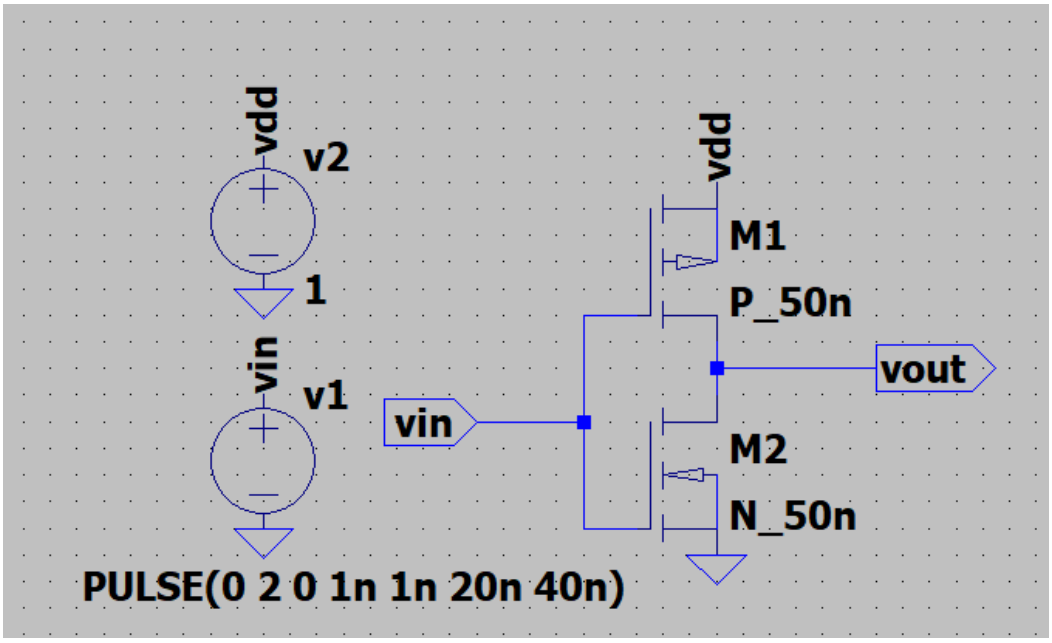


Fig:5

Output simulations :

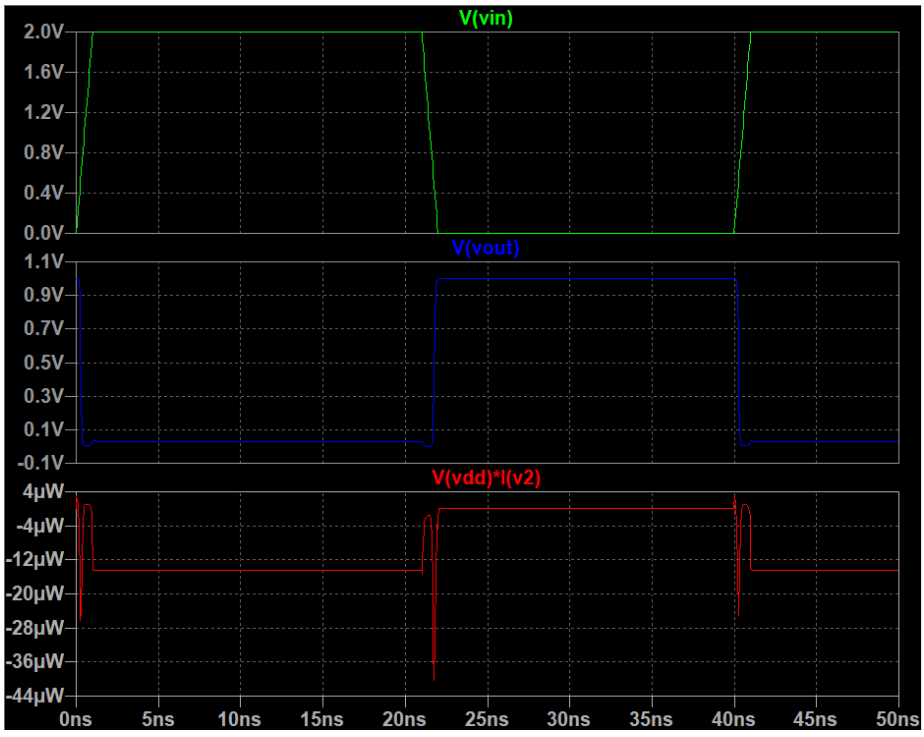


Fig:6

short channel: This is the 50n technology node i,e channel length used for both the p and n type MOS are 50n.

Design of NAND circuit:

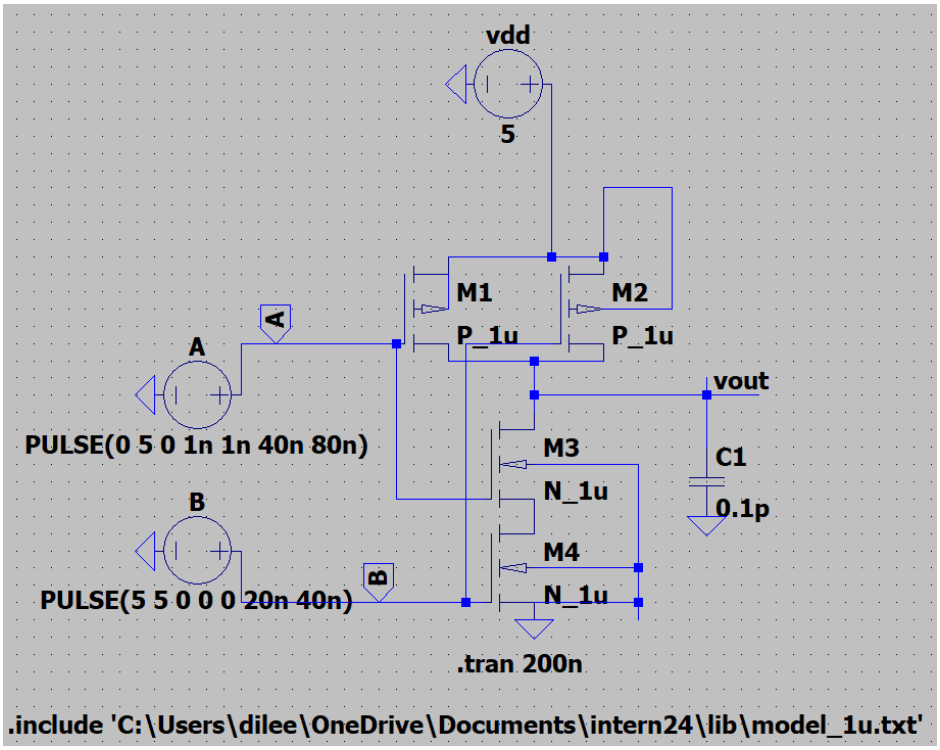


Fig:7

Output simulations:

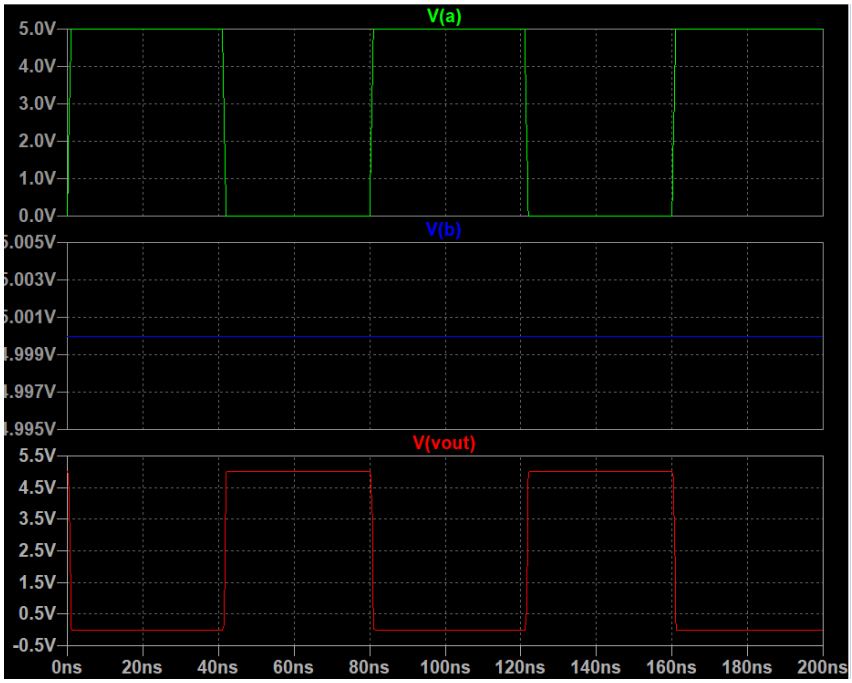


Fig:8

Full adder

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. The C-OUT is also known as the majority 1's detector, whose output goes high when more than one input is high. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. we use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit

.

Fig:9

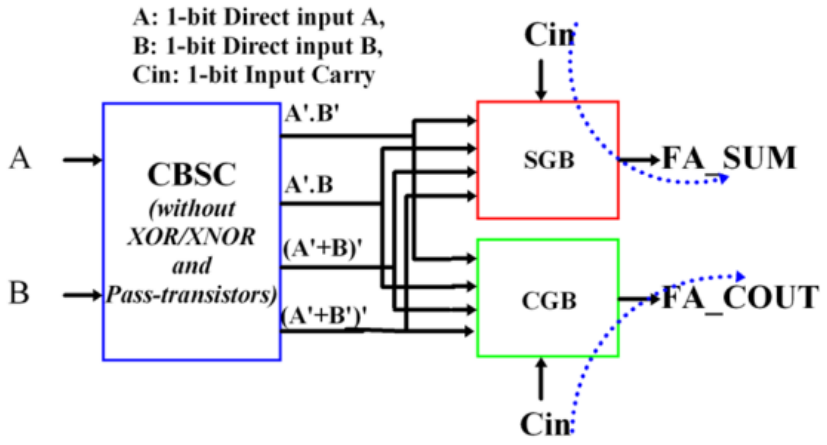
Table 3 shows Full Adder truth table:

inputs			outputs	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

b) Design of Novel Full Adder :

The proposed NFA design has three modules that do not use simple pass transistors and XOR/XNOR logic to obtain the FA SUM and FA COUT of a CMOS-based full adder circuit. The design uses CMOS which results in low power dissipation at lower technology nodes. The type of logic style, topology, and selective transmission gates improve the performance of a circuit. The proposed design also uses a mixed logic style to improve the performance. The below figure depicts a block diagram of the proposed NFA. The Common Block for Sum and Carry (CBSC) generates terms such as (A'.B'), (A'.B), (A'+B'), and (A'+B). These outputs are given to the Sum Generation Block (SGB) and Carry Generation Block (CGB). The propagation delay of carry is reduced by passing input carry (Cin) through a single transmission gate of each block as shown in below fig 10.

Fig:10



The direct inputs A and B of the proposed NFA are given to CBSC; therefore, this module's outputs do not rely on input carry. It produces four outputs W0, W1, W2, and W3. The expressions of the four outputs are given below.

W0=A'.B' , W1=A'.B ,W2=(A'+B)' and W3=(A'+B')'

The SGB of the proposed FA is designed using only two transmission gates (TG) to generate FA SUM. The expression of the sum generation block is FA_SUM = W0.Cin + W3 .Cin + W1.Cin' + W2.Cin'

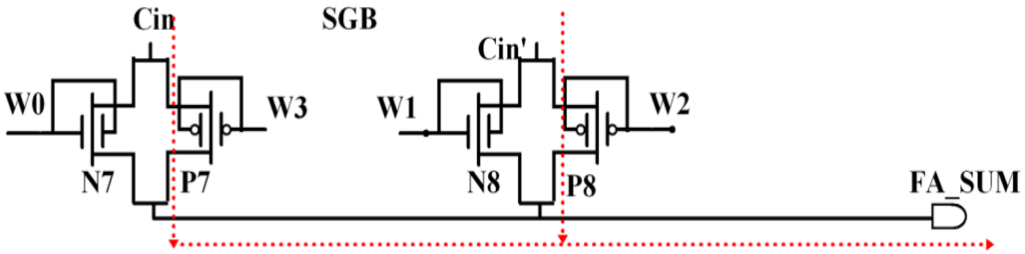


Fig: 11

The proposed CGB is better in terms of voltage swing and noise margin at lower supply voltages. Module III constructed with single TG, p-MOS connected to supply voltage, and n-MOS connected to ground. The expression of the carry generation block is FA_COUT = W1.Cin + W2.Cin + (A.B).

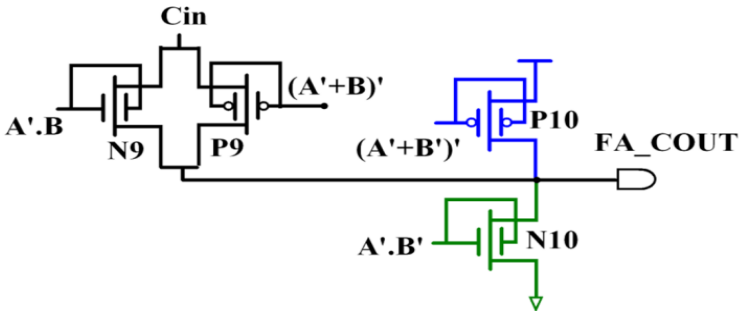


Fig 12:

This topology produces maximum voltage swing for FA COUT (FA OC). The inputs for p-MOS and n-MOS are taken from w3 and w4 of CBSC respectively. The FA OC is produced at a faster rate as input carry has to propagate through the signal transmission gate, which require less time for carry propagation.

Designed circuit of Novel Full Adder using 20 transistors

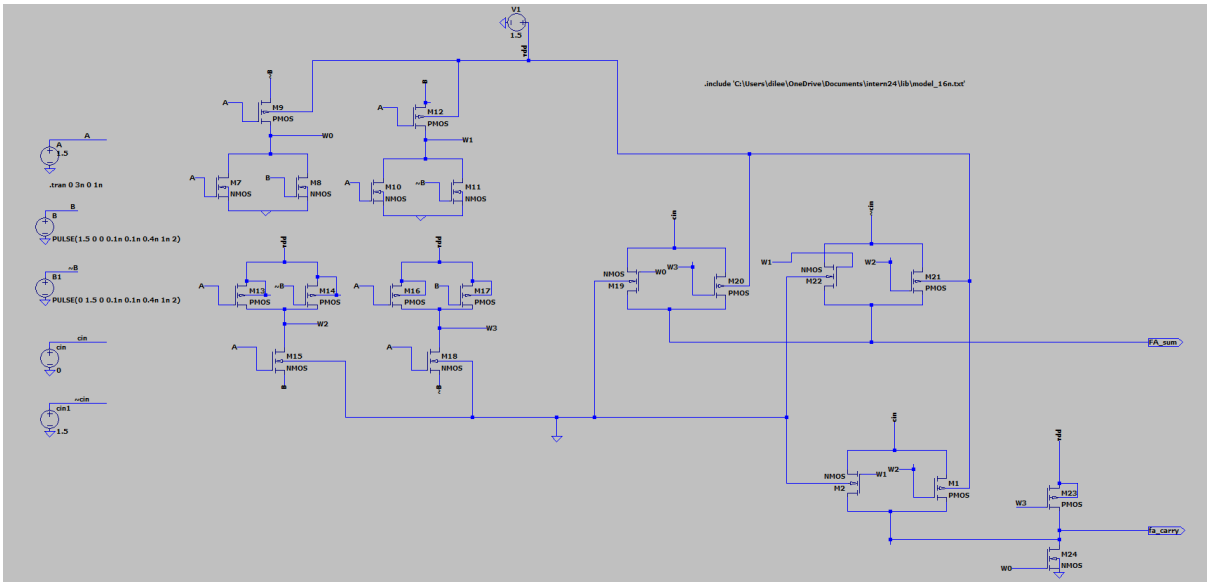


Fig ;13

Features of this Novel Full Adder

The complete circuit of NFA with three modules using 20 T is shown in above Fig. The CBSC is constructed and designed using 12 T. The design of SGB and CGB uses 4 T each. The main advantages of the proposed NFA are listed below,

– Pass-transistors are completely removed to improve the voltage swing.

– Complex XOR/XNOR modules are not used for the generation of the FA SUM and FA COUT of proposed NFA.

– The FA COUT is produced at faster rate as there exists single TG in the path from input carry.

– The design has an equal number of p and n-type transistors; 10 T of each type to maintain uniformity and high package density.

– It consumes less power due to the new architecture module I of the proposed NFA.

– It exhibits less propagation delay as 12 T module I relies only on the direct inputs but not on the input carry which is normally taken from previous FA in cascaded structure.

Output waveform:

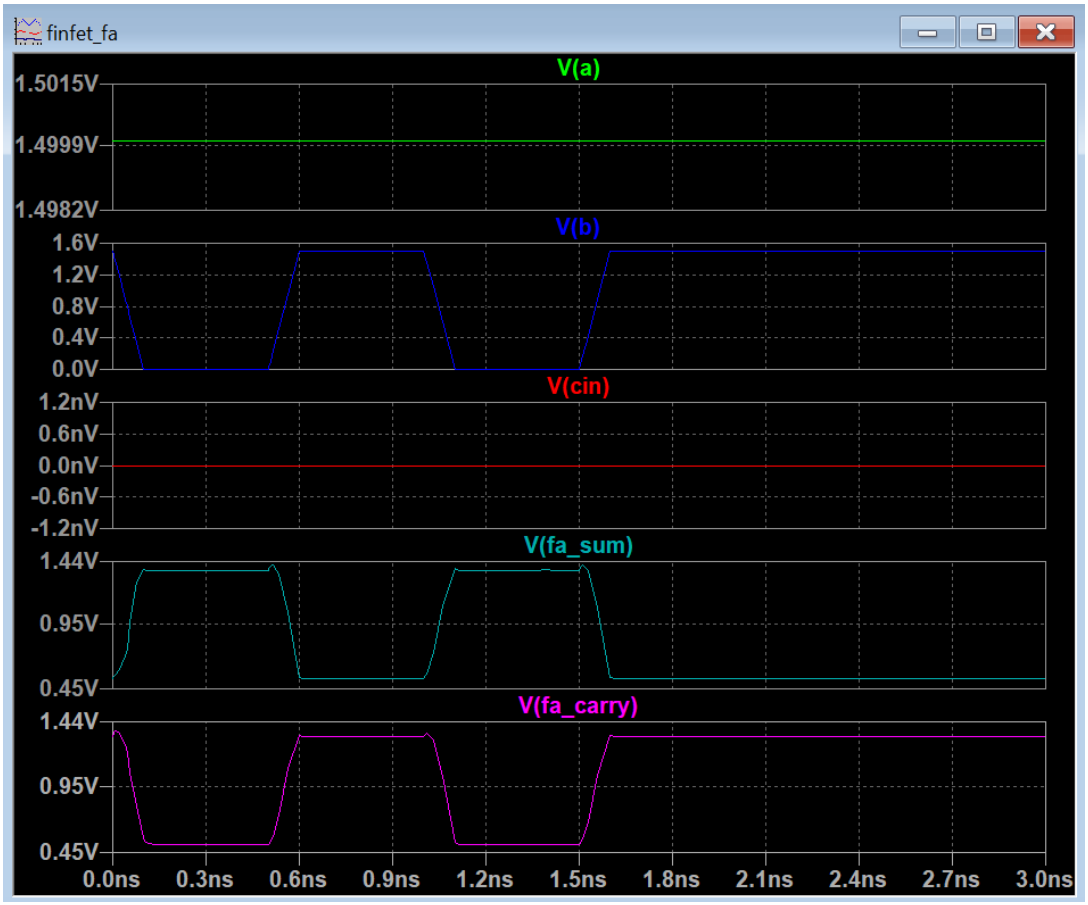


Fig: 14

Analysis and Results comparison

The Ltspice tool is used for the design, simulation, power and delay analysis . The model libraries of 22 nm High Performance-CMOS technology are collected from PTM model files .

Delay analysis:

At 1 GHz input frequency, the proposed 1-bit FA is simulated for transient and power analysis for 0.8 V, 1 V, 1.2 V, and 1.5 V. The full-swing transient response of the proposed NFA is shown in the output waveform. The time period of the input B is chosen as 1ns and for the remaining inputs given dc voltages for the transient analysis. For best result analysis and comparison, all the existing designs are simulated with same time periods. As the proposed design targets to reduce carry propagation time; therefore, the carry delay is minimized by 25-88% and the sum delay is 32-38 % minimized compared to a conventional Full adder.

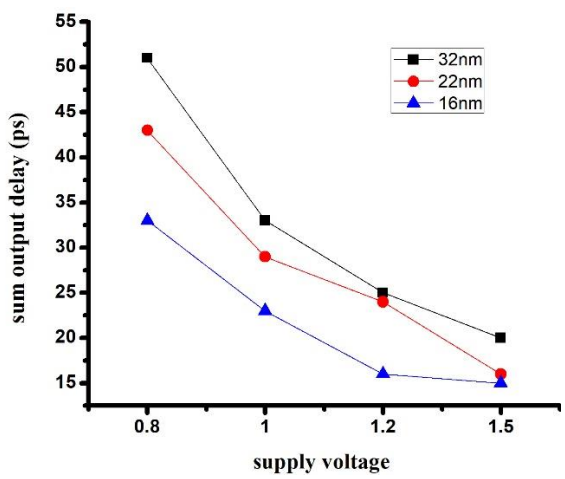


Fig:15

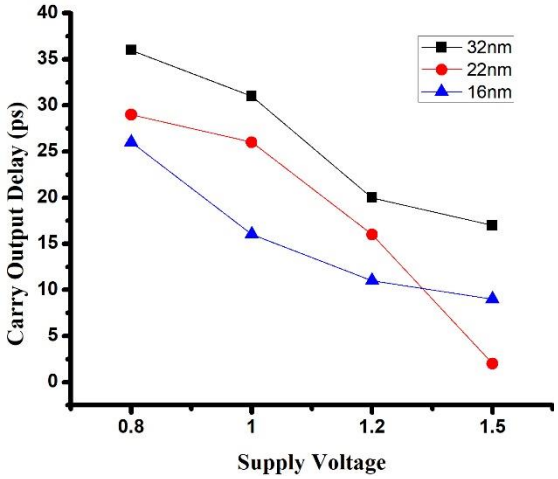


Fig :16

Power and PDP analysis:

Few of the previous FAs have not produced full swing output for certain low supply voltages due to threshold drop across pass-transistors; mainly at supply voltages 0.6 V and 1 V. The power comparison is carried out using the spice tool . The power is carried out for existing and proposed FAs by varying the supply volt ages; the proposed FA consumes 28-88% less power than existing designs. At the outset, the proposed FA is proved to be optimized as its PDP is reduced by

60-90% over existing designs. The PDP comparison results for both FA SUM and FA COUT outputs are shown in below fig 17 and fig 18.

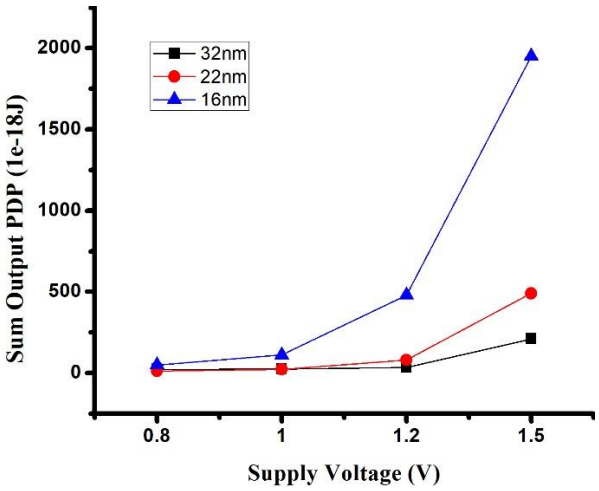


Fig:17

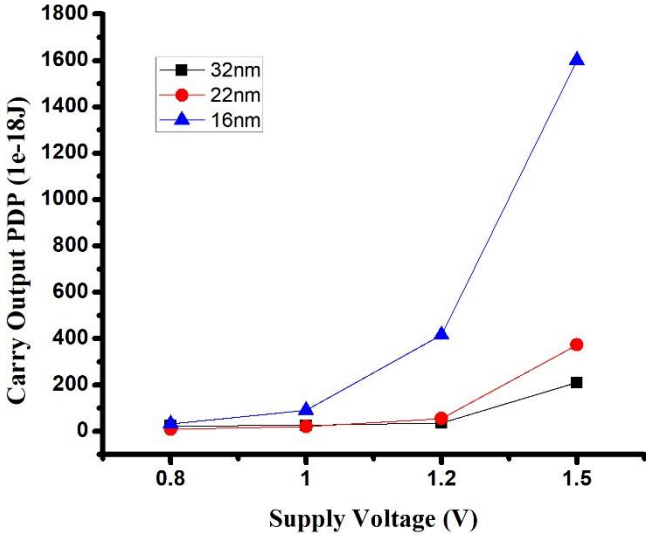


Fig:18

Conclusion:

The circuit design, and modelling of a novel full adder employing 20 T are presented in this project. The proposed work describes the design of a novel full adder using CMOSs without pass transistors. A new topology of hybrid full adder reduces the delay due to carry propagation from input to output node. The design process and functional verification of NFA is done at 22 nm technology using the `Ltspice tool. In terms of power dissipation and time, the suggested NFA outperforms previous designs; the reduction in power dissipation and delay is 28-88% and 2-13%, respectively.

Table 4 shows the sum and carry delay at three technology nodes:

Supply voltage(V)	Technology node 32nm		Technology node 22nm		Technology node 16nm	
	Sum Delay(ps)	**Carry delay(ps)**	**Sum Delay(ps)**	**Carry delay(ps)**	**Sum Delay(ps)**	**Carry delay(ps)**
1.5	20	17	16	2	14.7	9
1.2	25	20	23.6	16	16	11
1	33.4	31	28.6	25.6	23	16
0.8	50.8	36	43	29	33	26

APPENDIX:

The 22nm model file:

```
* PTM High Performance 22nm Metal Gate / High-K / Strained-Si
* nominal Vdd = 0.8V

.model  NMOS  nmos  level = 54

+version = 4.0          binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2            igcmod  = 1          igbmod  = 1          geomod  = 1
+diomod  = 1            rdsmod  = 0          rbodymod= 1          rgatemod= 1
+permod  = 1            acnqsmod= 0          trnqsmod= 0

+tnom    = 27           toxe    = 1.05e-009     toxp    = 8e-010        toxm    = 1.05e-009
+dtox    = 2.5e-010     epsrox  = 3.9           wint    = 5e-009        lint    = 2e-009
+ll      = 0            wl      = 0             lln     = 1             wln     = 1
+lw      = 0            ww      = 0             lwn     = 1             wwn     = 1
+lwl     = 0            wwl     = 0             xpart   = 0             toxref  = 1.05e-009
```

+xl = -9e-9

+vth0 = 0.50308 k1 = 0.4 k2 = 0 k3 = 0
+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2
+dvt2 = 0 dvt0w = 0 dvt1w = 0 dvt2w = 0
+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-011
+dvtp1 = 0.1 lpe0 = 0 lpeb = 0 xj = 7.2e-009
+ngate = 1e+023 ndep = 5.5e+018 nsd = 2e+020 phin = 0
+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0
+voff = -0.13 nfactor = 2.3 eta0 = 0.004 etab = 0
+vfb = -0.55 u0 = 0.04 ua = 6e-010 ub = 1.2e-018
+uc = 0 vsat = 250000 a0 = 1 ags = 0
+a1 = 0 a2 = 1 b0 = 0 b1 = 0
+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.02
+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = -0.005 drout = 0.5
+pvag = 1e-020 delta = 0.01 pscbe1 = 8.14e+008 pscbe2 = 1e-007
+fprout = 0.2 pdits = 0.01 pditsd = 0.23 pditsl = 2300000
+rsh = 5 rdsw = 145 rsw = 75 rdw = 75
+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0
+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005
+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002
+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
+eigbinv = 1.1 nigbinv = 3 aigc = 0.0213 bigc = 0.0025889
+cigc = 0.002 aigsd = 0.0213 bigsd = 0.0025889 cigsd = 0.002
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1
+xrcrg1 = 12 xrcrg2 = 5

+cgso = 6.5e-011 cgdo = 6.5e-011 cgbo = 2.56e-011 cgdl = 2.653e-010
+cgsl = 2.653e-010 ckappas = 0.03 ckappad = 0.03 acde = 1
+moin = 15 noff = 0.9 voffcv = 0.02

+kt1 = -0.11 kt11 = 0 kt2 = 0.022 ute = -1.5
+ua1 = 4.31e-009 ub1 = 7.61e-018 uc1 = -5.6e-011 prt = 0
+at = 33000

+fnoimod = 1 tnoimod = 0

+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1
+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 3e-010
+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001
+xtis = 3 xtid = 3

+dmcg = 0 dmci = 0 dmdg = 0 dmcgt = 0
+dwj = 0 xgw = 0 xgl = 0

+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15
+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

.model PMOS pmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0
+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1
+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1
+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 1.1e-009 toxp = 8e-010 toxm = 1.1e-009
+dtox = 3e-010 epsrox = 3.9 wint = 5e-009 lint = 2e-009
+ll = 0 wl = 0 lln = 1 wln = 1
+lw = 0 ww = 0 lwn = 1 wwn = 1
+lwl = 0 wwl = 0 xpart = 0 toxref = 1.1e-009
+xl = -9e-9

+vth0 = -0.4606 k1 = 0.4 k2 = -0.01 k3 = 0
+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2
+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0
+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-011
+dvtp1 = 0.05 lpe0 = 0 lpeb = 0 xj = 7.2e-009
+ngate = 1e+023 ndep = 4.4e+018 nsd = 2e+020 phin = 0
+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0
+voff = -0.126 nfactor = 2.1 eta0 = 0.0038 etab = 0
+vfb = 0.55 u0 = 0.0095 ua = 2e-009 ub = 5e-019
+uc = 0 vsat = 210000 a0 = 1 ags = 1e-020
+a1 = 0 a2 = 1 b0 = 0 b1 = 0
+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.12
+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = 3.4e-008 drout = 0.56
+pvag = 1e-020 delta = 0.01 pscbe1 = 8.14e+008 pscbe2 = 9.58e-007
+fprout = 0.2 pdits = 0.08 pditsd = 0.23 pditsl = 2300000
+rsh = 5 rdsw = 145 rsw = 72.5 rdw = 72.5
+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0
+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005
+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002
+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
+eigbinv = 1.1 nigbinv = 3 aigc = 0.0213 bigc = 0.0025889
+cigc = 0.002 aigsd = 0.0213 bigsd = 0.0025889 cigsd = 0.002
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 6.5e-011 cgdo = 6.5e-011 cgbo = 2.56e-011 cgdl = 2.653e-010
+cgsl = 2.653e-010 ckappas = 0.03 ckappad = 0.03 acde = 1
+moin = 15 noff = 0.9 voffcv = 0.02

+kt1 = -0.11 kt11 = 0 kt2 = 0.022 ute = -1.5
+ua1 = 4.31e-009 ub1 = 7.61e-018 uc1 = -5.6e-011 prt = 0
+at = 33000

+fnoimod = 1 tnoimod = 0

+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1
+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1
+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1
+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1
+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1
+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 3e-010
+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5
+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1
+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001
+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001
+xtis = 3 xtid = 3

+dmcg = 0 dmci = 0 dmdg = 0 dmcgt = 0
+dwj = 0 xgw = 0 xgl = 0

+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15
+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

The 50n model file

```
* Short channel models from CMOS Circuit Design, Layout, and Simulation,
* 50nm BSIM4 models VDD=1V, see CMOSedu.com
*
.model  N_50n  nmos  level = 54
+binunit = 1          paramchk= 1          mobmod  = 0
+capmod  = 2          igcmod  = 1          igbmod  = 1          geomod  = 0
+diomod  = 1          rdsmod  = 0          rbodymod= 1          rgatemod= 1
+permod  = 1          acnqsmod= 0          trnqsmod= 0
+tnom    = 27         toxe    = 1.4e-009   toxp    = 7e-010     toxm    = 1.4e-009
+epsrox  = 3.9        wint    = 5e-009     lint    = 1.2e-008
+ll      = 0          wl      = 0          lln     = 1          wln     = 1
+lw      = 0          ww      = 0          lwn     = 1          wwn     = 1
+lwl     = 0          wwl     = 0          xpart   = 0          toxref  = 1.4e-009
+vth0    = 0.22       k1      = 0.35       k2      = 0.05       k3      = 0
+k3b     = 0          w0      = 2.5e-006   dvt0    = 2.8        dvt1    = 0.52
+dvt2    = -0.032     dvt0w   = 0          dvt1w   = 0          dvt2w   = 0
+dsub    = 2          minv    = 0.05       voffl   = 0          dvtp0   = 1e-007
+dvtp1   = 0.05       lpe0    = 5.75e-008  lpeb    = 2.3e-010   xj      = 2e-008
+ngate   = 5e+020     ndep    = 2.8e+018   nsd     = 1e+020     phin    = 0
+cdsc    = 0.0002     cdscb   = 0          cdscd   = 0          cit     = 0
+voff    = -0.15      nfactor = 1.2        eta0    = 0.15       etab    = 0
+vfb     = -0.55      u0      = 0.032      ua      = 1.6e-010   ub      = 1.1e-017
+uc      = -3e-011    vsat    = 1.1e+005   a0      = 2          ags     = 1e-020
+a1      = 0          a2      = 1          b0      = -1e-020    b1      = 0
+keta    = 0.04       dwg     = 0          dwb     = 0          pclm    = 0.18
+pdiblc1 = 0.028      pdiblc2 = 0.022      pdiblcb = -0.005     drout   = 0.45
+pvag    = 1e-020     delta   = 0.01       pscbe1  = 8.14e+008  pscbe2  = 1e-007
+fprout  = 0.2        pdits   = 0.2        pditsd  = 0.23       pditsl  = 2.3e+006
+rsh     = 3          rdsw    = 150        rsw     = 150        rdw     = 150
+rdswmin = 0          rdwmin  = 0          rswmin  = 0          prwg    = 0
+prwb    = 6.8e-011   wr      = 1          alpha0  = 0.074      alpha1  = 0.005
```

```
+beta0   = 30          agidl   = 0.0002       bgidl   = 2.1e+009     cgidl   = 0.0002
+egidl   = 0.8
+aigbacc = 0.012       bigbacc = 0.0028       cigbacc = 0.002
+nigbacc = 1           aigbinv = 0.014        bigbinv = 0.004        cigbinv = 0.004
+eigbinv = 1.1         nigbinv = 3            aigc    = 0.017        bigc    = 0.0028
+cigc    = 0.002       aigsd   = 0.017        bigsd   = 0.0028       cigsd   = 0.002
+nigc    = 1           poxedge = 1            pigcd   = 1            ntox    = 1
+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 6.238e-010  cgdo    = 6.238e-010   cgbo    = 2.56e-011    cgdl    = 2.495e-10
+cgsl    = 2.495e-10   ckappas = 0.02         ckappad = 0.02         acde    = 1
+moin    = 15          noff    = 0.9          voffcv  = 0.02
+kt1     = -0.21       kt1l    = 0.0          kt2     = -0.042       ute     = -1.5
+ua1     = 1e-009      ub1     = -3.5e-019    uc1     = 0            prt     = 0
+at      = 53000
+fnoimod = 1           tnoimod = 0
+jss     = 0.0001      jsws    = 1e-011       jswgs   = 1e-010       njs     = 1
+ijthsfwd= 0.01        ijthsrev= 0.001        bvs     = 10           xjbvs   = 1
+jsd     = 0.0001      jswd    = 1e-011       jswgd   = 1e-010       njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001        bvd     = 10           xjbvd   = 1
+pbs     = 1           cjs     = 0.0005       mjs     = 0.5          pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33         pbswgs  = 1            cjswgs  = 5e-010
+mjswgs  = 0.33        pbd     = 1            cjd     = 0.0005       mjd     = 0.5
+pbswd   = 1           cjswd   = 5e-010       mjswd   = 0.33         pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33         tpb     = 0.005        tcj     = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001        tpbswg  = 0.005        tcjswg  = 0.001
+xtis    = 3           xtid    = 3
+dmcg    = 0e-006      dmci    = 0e-006       dmdg    = 0e-006       dmcgt   = 0e-007
+dwj     = 0e-008      xgw     = 0e-007       xgl     = 0e-008
+rshg    = 0.4         gbmin   = 1e-010       rbpb    = 5            rbpd    = 15
+rbps    = 15          rbdb    = 15           rbsb    = 15           ngcon   = 1
*
.model  P_50n  pmos  level = 54
```

+binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 0

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 1.4e-009 toxp = 7e-010 toxm = 1.4e-009

+epsrox = 3.9 wint = 5e-009 lint = 1.2e-008

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 1.4e-009

+vth0 = -0.22 k1 = 0.39 k2 = 0.05 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 3.9 dvt1 = 0.635

+dvtp1 = 0.05 lpe0 = 5.75e-008 lpeb = 2.3e-010 xj = 2e-008 +dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.7 minv = 0.05 voffl = 0 dvtp0 = 0.5e-008

+ngate = 5e+020 ndep = 2.8e+018 nsd = 1e+020 phin = 0

+cdsc = 0.000258 cdscb = 0 cdscd = 6.1e-008 cit = 0

+voff = -0.15 nfactor = 2 eta0 = 0.15 etab = 0

+vfb = 0.55 u0 = 0.0095 ua = 1.6e-009 ub = 8e-018

+uc = 4.6e-013 vsat = 90000 a0 = 1.2 ags = 1e-020

+a1 = 0 a2 = 1 b0 = -1e-020 b1 = 0

+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.55

+pdiblc1 = 0.03 pdiblc2 = 0.0055 pdiblcb = 3.4e-008 drout = 0.56

+pvag = 1e-020 delta = 0.014 pscbe1 = 8.14e+008 pscbe2 = 9.58e-007

+fprout = 0.2 pdits = 0.2 pditsd = 0.23 pditsl = 2.3e+006

+rsh = 3 rdsw = 250 rsw = 160 rdw = 160

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 3.22e-008

+prwb = 6.8e-011 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8

+aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.69 bigc = 0.0012

+cigc = 0.0008 aigsd = 0.0087 bigsd = 0.0012 cigsd = 0.0008

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7.43e-010 cgdo = 7.43e-010 cgbo = 2.56e-011 cgdl = 1e-014

+cgsl = 1e-014 ckappas = 0.5 ckappad = 0.5 acde = 1

+moin = 15 noff = 0.9 voffcv = 0.02

+kt1 = -0.19 kt11 = 0 kt2 = -0.052 ute = -1.5

+ua1 = -1e-009 ub1 = 2e-018 uc1 = 0 prt = 0

+at = 33000

+fnoimod = 1 tnoimod = 0

+jss = 0.0001 jsws = 1e-011 jswgs = 1e-010 njs = 1

+ijthsfwd= 0.01 ijthsrev= 0.001 bvs = 10 xjbvs = 1

+jsd = 0.0001 jswd = 1e-011 jswgd = 1e-010 njd = 1

+ijthdfwd= 0.01 ijthdrev= 0.001 bvd = 10 xjbvd = 1

+pbs = 1 cjs = 0.0005 mjs = 0.5 pbsws = 1

+cjsws = 5e-010 mjsws = 0.33 pbswgs = 1 cjswgs = 5e-010

+mjswgs = 0.33 pbd = 1 cjd = 0.0005 mjd = 0.5

+pbswd = 1 cjswd = 5e-010 mjswd = 0.33 pbswgd = 1

+cjswgd = 5e-010 mjswgd = 0.33 tpb = 0.005 tcj = 0.001

+tpbsw = 0.005 tcjsw = 0.001 tpbswg = 0.005 tcjswg = 0.001

+xtis = 3 xtid = 3

+dmcg = 0e-006 dmci = 0e-006 dmdg = 0e-006 dmcgt = 0e-007

+dwj = 0e-008 xgw = 0e-007 xgl = 0e-008

+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15

+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

The 1u model file

.MODEL N_1u NMOS LEVEL = 3

+ TOX = 200E-10 NSUB = 1E17 GAMMA = 0.5

+ PHI = 0.7 VTO = 0.8 DELTA = 3.0

+ UO = 650 ETA = 3.0E-6 THETA = 0.1

+ KP = 120E-6 VMAX = 1E5 KAPPA = 0.3

```
+ RSH    = 0          NFS    = 1E12        TPG    = 1
+ XJ     = 500E-9     LD     = 100E-9
+ CGDO   = 200E-12    CGSO   = 200E-12     CGBO   = 1E-10
+ CJ     = 400E-6     PB     = 1           MJ     = 0.5
+ CJSW   = 300E-12    MJSW   = 0.5
*
.MODEL P_1u PMOS LEVEL  = 3
+ TOX    = 200E-10    NSUB   = 1E17        GAMMA  = 0.6
+ PHI    = 0.7        VTO    = -0.9        DELTA  = 0.1
+ UO     = 250        ETA    = 0           THETA  = 0.1
+ KP     = 40E-6      VMAX   = 5E4         KAPPA  = 1
+ RSH    = 0          NFS    = 1E12        TPG    = -1
+ XJ     = 500E-9     LD     = 100E-9
+ CGDO   = 200E-12    CGSO   = 200E-12     CGBO   = 1E-10
+ CJ     = 400E-6     PB     = 1           MJ     = 0.5
+ CJSW   = 300E-12    MJSW   = 0.5
```

References:

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