

EC 2.101 - Digital Systems and Microcontrollers

Practice Sheet 3 (Lec 1 – Lec 17)

Q1. Design a combinatorial circuit for 4-bit

a. Binary-to-Gray converter

<i>Binary</i>				<i>Gray</i>			
<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>	<i>W</i>	<i>X</i>	<i>Y</i>	<i>Z</i>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

As given in the question, Gray code is an encoding of binary numbers such that adjacent numbers only differ by one bit. Gray code has extensive applications in error correcting codes, solutions to the Tower of Hanoi problem, etc.

- The bit combinations for 4-bit binary code and its equivalent bit combinations of gray code are listed above.
- The four bits of binary numbers are designated as A, B, C, and D, and gray code bits are designated as W, X, Y, and Z.

- For transformation of binary numbers to gray, A, B, C, and D are considered as inputs and W, X, Y, and Z are considered as outputs.

	C'D'	C'D	CD	CD'
A'B'				
A'B				
AB	1	1	1	1
AB'	1	1	1	1

Figure 1: K-map for W

	C'D'	C'D	CD	CD'
A'B'				
A'B	1	1	1	1
AB				
AB'	1	1	1	1

Figure 2: K-map for X

	C'D'	C'D	CD	CD'
A'B'			1	1
A'B	1	1		
AB	1	1		
AB'			1	1

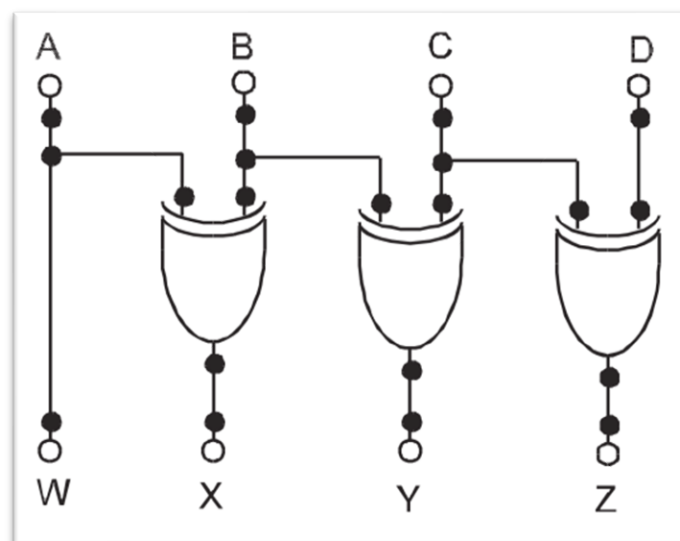
Figure 3: K-map for Y

	C'D'	C'D	CD	CD'
A'B'		1		1
A'B		1		1
AB		1		1
AB'		1		1

Figure 3: K-map for Z

From the K-maps, the Boolean expressions are determined to be as follows:

- $W = A$
- $X = A'B + AB' = A \oplus B$
- $Y = BC' + B'C = B \oplus C$
- $Z = C'D + CD' = C \oplus D$



b. Gray-to-Binary converter

- Using the same conversion table as in 1.a., the Karnaugh maps are formed below.
- Here the inputs are considered as W, X, Y, and Z, whereas, outputs are A, B, C, and D.

	Y'Z'	Y'Z	YZ	YZ'
W'X'				
W'X				
WX	1	1	1	1
WX'	1	1	1	1

Figure 5.16(a) Karnaugh map for A.

	Y'Z'	Y'Z	YZ	YZ'
W'X'				
W'X	1	1	1	1
WX				
WX'	1	1	1	1

Figure 5.16(b) Karnaugh map for B.

	Y'Z'	Y'Z	YZ	YZ'
W'X'			1	1
W'X	1	1		
WX			1	1
WX'	1	1		

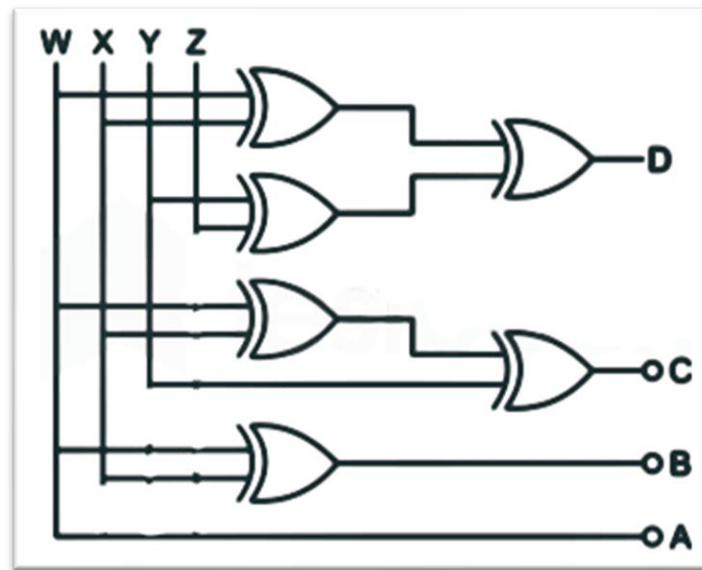
Figure 5.16(c) Karnaugh map for C.

	Y'Z'	Y'Z	YZ	YZ'
W'X'		1		1
W'X	1		1	
WX		1		1
WX'	1		1	

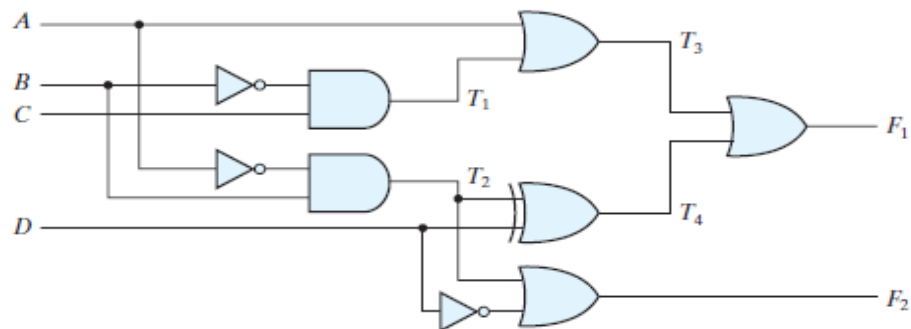
Figure 5.16(d) Karnaugh map for D.

The Boolean expressions will be as follows:

- $A = W$
- $B = W'X + WX' = W \oplus X$
- $$\begin{aligned}
 C &= W'X'Y + W'XY' + WXY + WX'Y' \\
 &= W'(X'Y + XY') + W(XY + X'Y') \\
 &= W'(X \oplus Y) + W(X \oplus Y)' \\
 &= W \oplus X \oplus Y = B \oplus Y
 \end{aligned}$$
- $$\begin{aligned}
 D &= W'X'Y'Z + W'X'YZ' + W'XY'Z' + W'XYZ + WXY'Z + WXYZ' + \\
 &\quad WX'Y'Z' + WX'YZ \\
 &= W'X'(Y'Z + YZ') + W'X(Y'Z' + YZ) + WX(Y'Z + YZ') + WX'(Y' + YZ) \\
 &= W'X'(Y \oplus Z) + W'X(Y \oplus Z)' + WX(Y \oplus Z) + WX'(Y \oplus Z)' \\
 &= (W'X + WX')(Y \oplus Z)' + (W'X' + WX)(Y \oplus Z) \\
 &= (W \oplus X)(Y \oplus Z)' + (W \oplus X)'(Y \oplus Z) \\
 &= W \oplus X \oplus Y \oplus Z = C \oplus Z
 \end{aligned}$$



Q2. Obtain the Simplified Boolean Expressions for the following outputs



a.

$$T1 = B'C$$

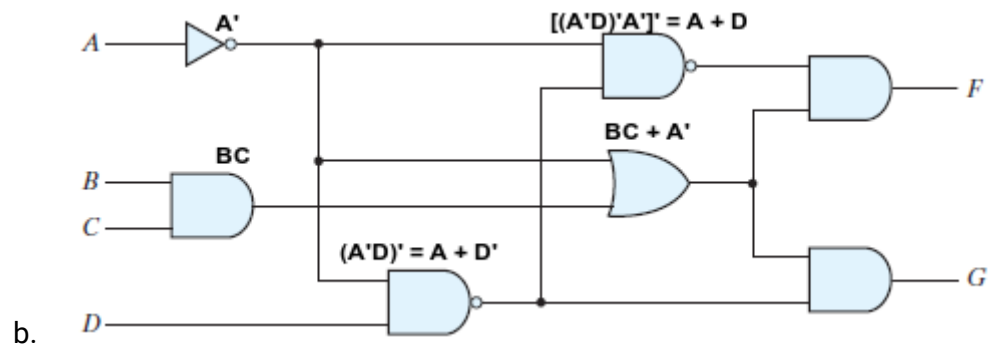
$$T2 = A'B$$

$$\begin{aligned} T3 &= A + T1 \\ &= A + B'C \end{aligned}$$

$$\begin{aligned} T4 &= D \oplus T2 \\ &= D \oplus (A'B) \\ &= A'BD' + D(A + B') \quad [A + A'BD' = A + BD'] \\ &= A'BD' + AD + B'D \quad [A + AD = A] \end{aligned}$$

$$F1 = A + B'C + BD' + B'D \quad (\text{or}) \quad F1 = A + CD' + BD' + B'D$$

$$F2 = T2 + D' = A'B + D'$$



$$\begin{aligned}
 F &= (A + D)(A' + BC) \\
 &= A'D + ABC + BCD \\
 &= A'D + ABC
 \end{aligned}$$

$$\begin{aligned}
 G &= (A + D')(A' + BC) \\
 &= A'D' + ABC + BCD' \\
 &= A'D' + ABC
 \end{aligned}$$

Q3. Given 4-bit input message, design a circuit that generates:

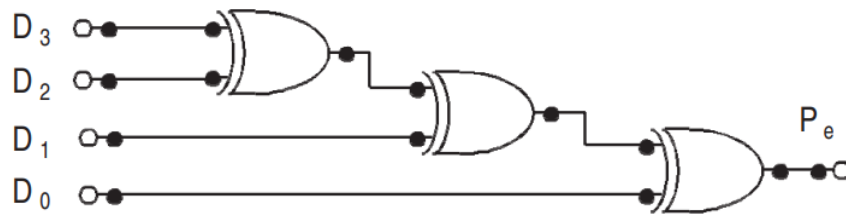
a. Even parity bit

Four bit Message $D_3D_2D_1D_0$	Even Parity (P_e)	Odd Parity (P_o)
0000	0	1
0001	1	0
0010	1	0
0011	0	1
0100	1	0
0101	0	1
0110	0	1
0111	1	0
1000	1	0
1001	0	1
1010	0	1
1011	1	0
1100	0	1
1101	1	0
1110	1	0
1111	0	1

Parity bits are one of the methods used to ensure that the data has been transmitted correctly. A few other ways include start bits, stop bits, etc. There are two types of parity. Even parity and Odd parity. In even parity, the transmitted data is ensured to contain an even number of 1s in it. So, if the number of 1s in the message are odd, the parity bit becomes 1, hence making the total number of 1s even. Alternatively, if the number of 1s is already even, the parity bit will be zero. The same rules apply for odd parity, except that the total number of 1s will always be odd. You can check that these rules hold in the truth table.

Since the message bit combination is designated as $D_3D_2D_1D_0$, and from the definition of XOR it is clear that even parity is given by

$$P_e = D_3 \oplus D_2 \oplus D_1 \oplus D_0 \text{ (Can be determined by kmaps as well)}$$



b. Odd parity bit

From the previous table, it is clear that odd parity bit is given by

$$\begin{aligned} P_o &= P_e' \\ &= (D_3 \oplus D_2 \oplus D_1 \oplus D_0)' \end{aligned}$$

(Can be determined by kmaps as well)

