EC-2014-2

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1 Question

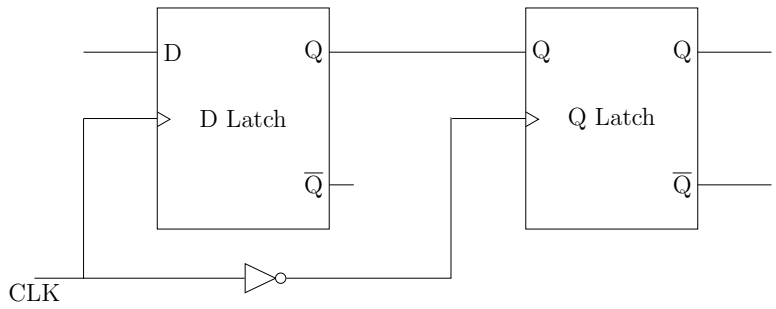

Figure 1: Question Diagram

Current option is

(a) JK flip-flop

(b) SR flip-flop

(c) D flip-flop

(d) Master-slave arrangement

2 Answer

The correct option is d)Master-slave arrangement

2.1 Master-Slave D flip flop

The basic D-type flip flop can be improved further by adding a second SR flip flop to its output that is activated on the complementary clock signal to produce a "Master-Slave D-type flip flop".On the leading edge of the clock signal(LOW-to-HIGH)the first stage, the "master" latches the input condition at D,while the output stage is deactivated.

On the trailing edge of the clock signal (HIGH-to-LOW), the second"slave" stage is now activated, latching on to the output from the first master circuit. Then the output stage appears to be triggered on the negative edge of the clock pulse." Master-Slave D-type flip flop" can be constructed by the cascading together of two latches with opposite clock phases as shown.

2.2 Transition Table

Present State		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

2.3 State Diagram

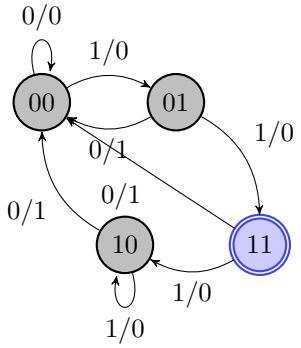

Figure 2: State Diagram

We can see from above that on the leading edge of the clock pulse the master flip-flop will be loading data from the data D input, therefore the master is "ON". With the trailing edge of the clock pulse, the slave flip-flop is loading data,i.e.the slave is "ON".Then there will always be one flip-flop"ON" and the other "OFF" but never both the master and slave "ON" at the same time.Therefore, the output Q acquires the value of D,only when one complete pulse,ie,0-1- is applied to clock input.