assignment 11

solution to gate EC 2014-2,question 9

dilip

IIIT RAICHUR

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Question Figure

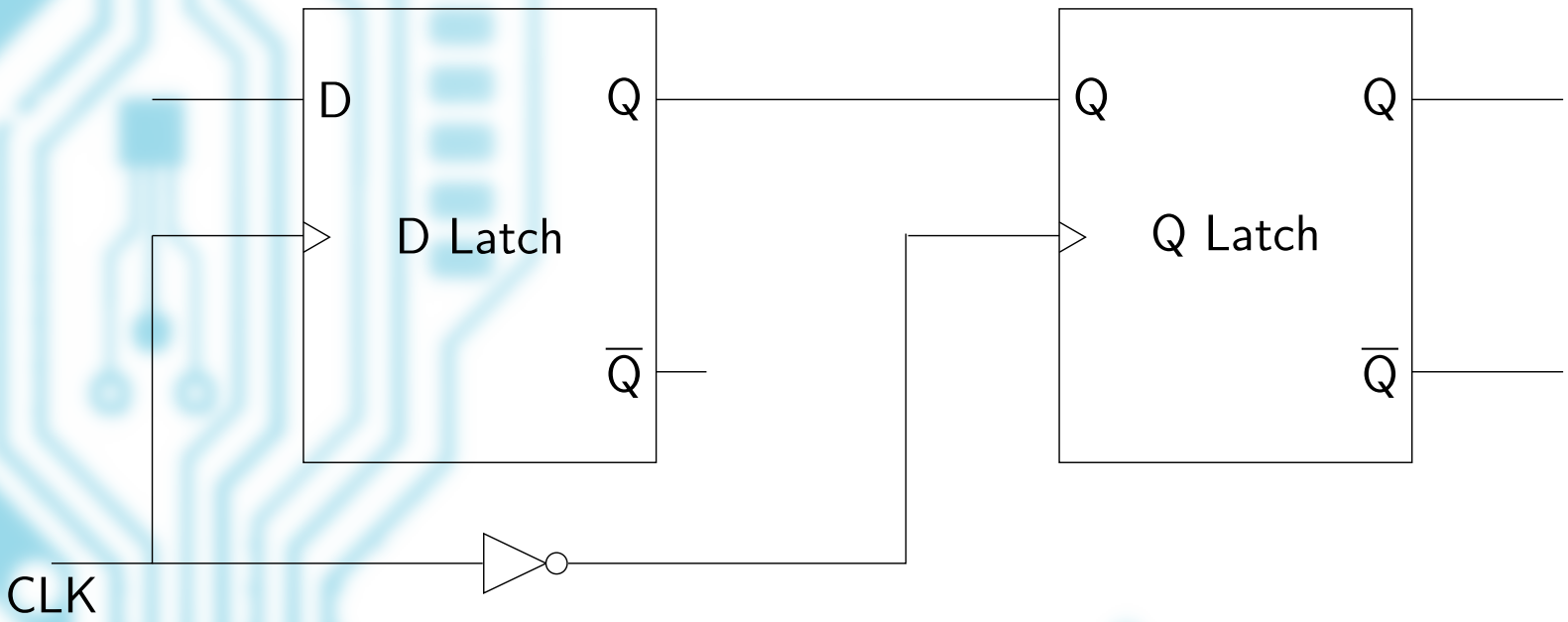

Figure: Question Diagram

Question Text

Current option is

(a) JK flip-flop

(b) SR flip-flop

(c) D flip-flop

(d) Master-slave arrangement

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Answer

The correct option is d)Master-slave arrangement.

The basic D-type flip flop can be improved further by adding a second SR flip flop to its output that is activated on the complementary clock signal to produce a "Master-Slave D-type flip flop".On the leading edge of the clock signal(LOW-to-HIGH)the first stage, the "master" latches the input condition at D,while the output stage is deactivated.
On the trailing edge of the clock signal (HIGH-to-LOW), the second "slave" stage is now activated, latching on to the output from the first master circuit.Then the output stage appears to be triggered on the negative edge of the clock pulse."Master-Slave D-type flip flop" can be constructed by the cascading together of two latches with opposite clock phases as shown.

Transition Table

Present State		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

State Diagram

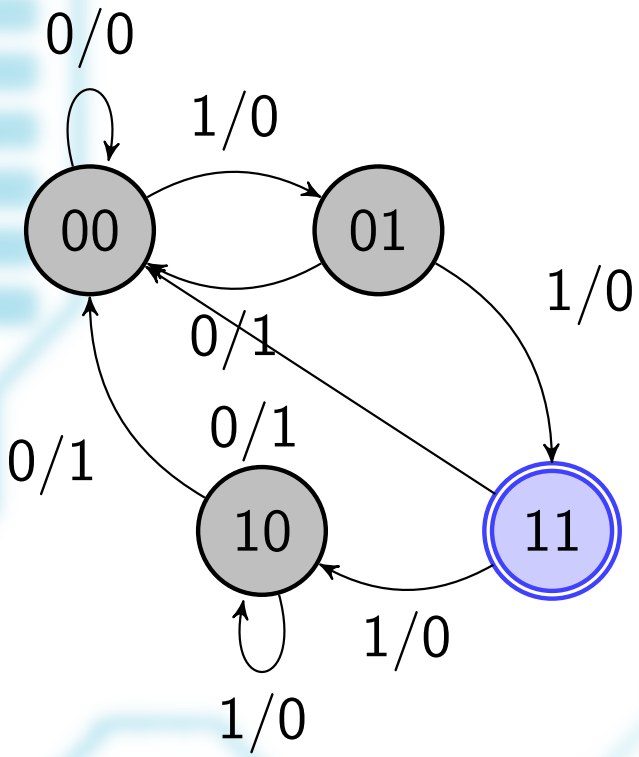

Figure: State Diagram

Timing Diagrams

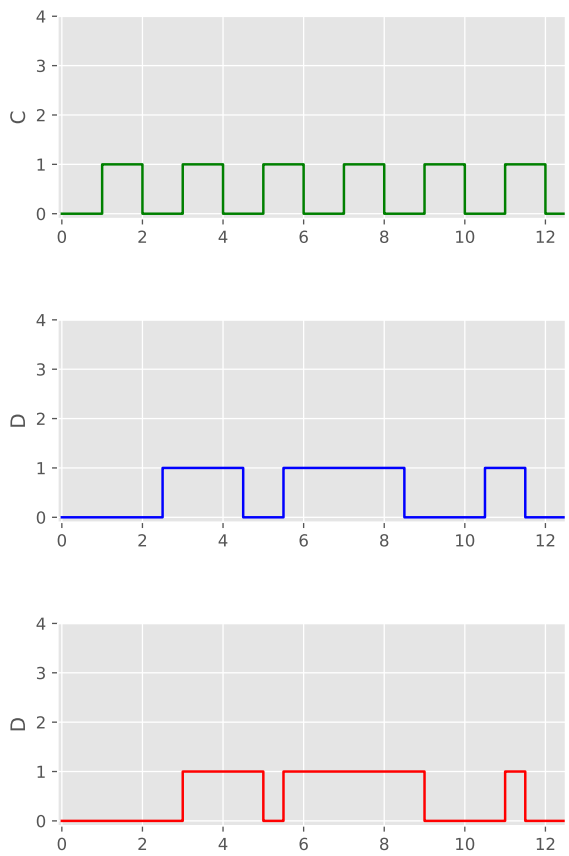

Figure: Timing diagram