Tribhuvan University Institute of Science and Technology 2078

Bachelor Level / second-semester / Science Full Marks: 60 + 20 + 20

Computer Science and Information Technology (CSC162) Pass Marks: 24 + 8 + 8

Microprocessor Time: 3 Hours

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Group A

Attempts any TWO questions

Explain instruction cycle, machine cycle and T-states. Draw timing diagram of IN instruction with brief description.

Draw block diagram of 80286 microprocessor and explain its main four functional subunits. Differentiate between Real Address Mode and Protected Virtual address mode.

Explain LXI and CMP instruction. Write an assembly language program for 8-bit microprocessor to divide 8 bit data stored in memory location 8050 by 8 bit data stored in 8051 and store the quotient in 8052 and remainder in 8053.

Group B

Attempts any EIGHT questions

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	What are the different modes of parallel communication? Construct a control word for 8255 PPI for following configuration:
	Port A and Port C _{upper} – mode 0
4	Port B and Port C _{lower} – mode 0
	Port A and Port C _{upper} as input port
	Port B and Port C _{lower} as output port
5	Differentiate between interrupt based I/O and DMA based I/O. Explain based DMA operation in brief
6	Differentiate between PUSH and POP instruction with example illustrating the use of these instruction.
7	Write an assembly language program for 16 bit microprocessor to reverse the string "This is Microprocessor"
8	What is the use of AD_7 – AD_0 in 8085 microprocessor? Explain address demultiplexing process in 8085 microprocessor with suitable diagram.
9	What is mean by addressing mode? Explain all the addressing mode available in 8085 microprocessor.
10	Explain Register Organization in 80386 microprocessor.

Draw a logic diagram snowing generation of memory and I/O read/write control signals in 8085 microprocessor

Write short notes on (Any two):

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- a. Program Counter
- b. Von-Neumann Architecture
- c. Interrupt Masking