Introduction to 8255A PPI (Programmable Peripheral Interface)

8255A is widely used programmable parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile and economical (when multiple I/O ports are required), but somewhat complex. It is an important general purpose I/O device that can be used with almost any microprocessor.

The 8255A has 24 input output pins that can be grouped primarily in two 8 bits parallel ports: A and B, with the remaining 8 bits as port C. The 8 bits of port C can be used as individual bits or be grouped in two four bits ports: C_{upper} (C_U) and C_{lower} (C_L) as in figure (a). The functions of these ports are defined by writing a control word in the control registers.

Block Diagram

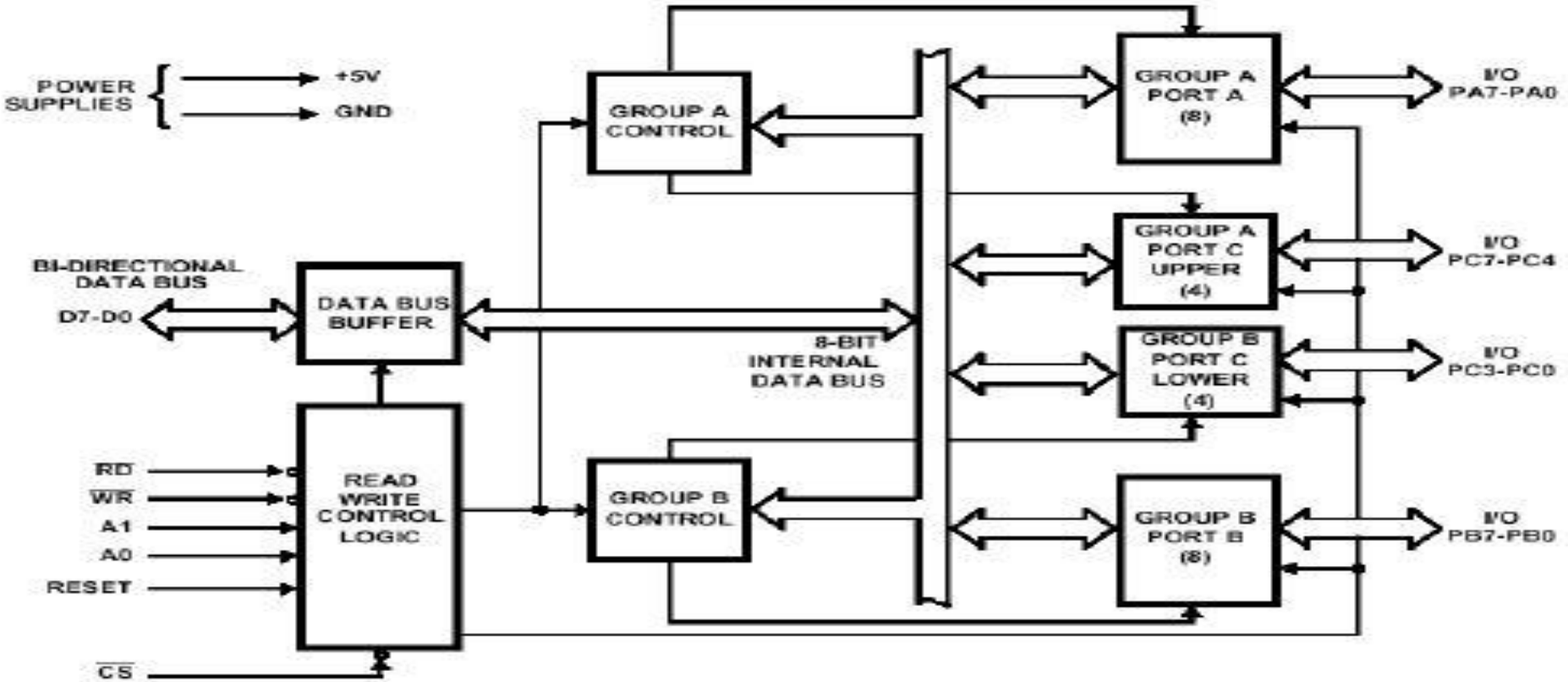

Fig (a): Internal Block Diagram of 8255A PPI

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A "low" on this input pin enables the communication between the 8255 and the CPU.

(RD) Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the 8255.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL REGISTER

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255. Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B.

Modes of Operation

The 8255A is primarily operated in two modes: I/O (input-output) mode and the BSR (Bit-Set-Reset) mode. The I/O mode is further grouped into Mode 0 (Simple I/O interfacing), Mode 1 (Interfacing with handshake signals) and Mode 2 (Bidirectional I/O interfacing).

Figure (b) shows all the functions of 8255A, classifying according to two modes: the Bit Set-Reset (BSR) mode and Input Output (I/O) mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: mode 0, mode 1 and mode 2. In mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A and ports B use bits from port C as handshake signals. In the handshake mode, two types of data transfer can be implemented: status check and interrupt. In mode 2, port A can be set up

for bidirectional data transfer using handshake signal from port C, and port B can be set up either in mode 0 or mode 1.

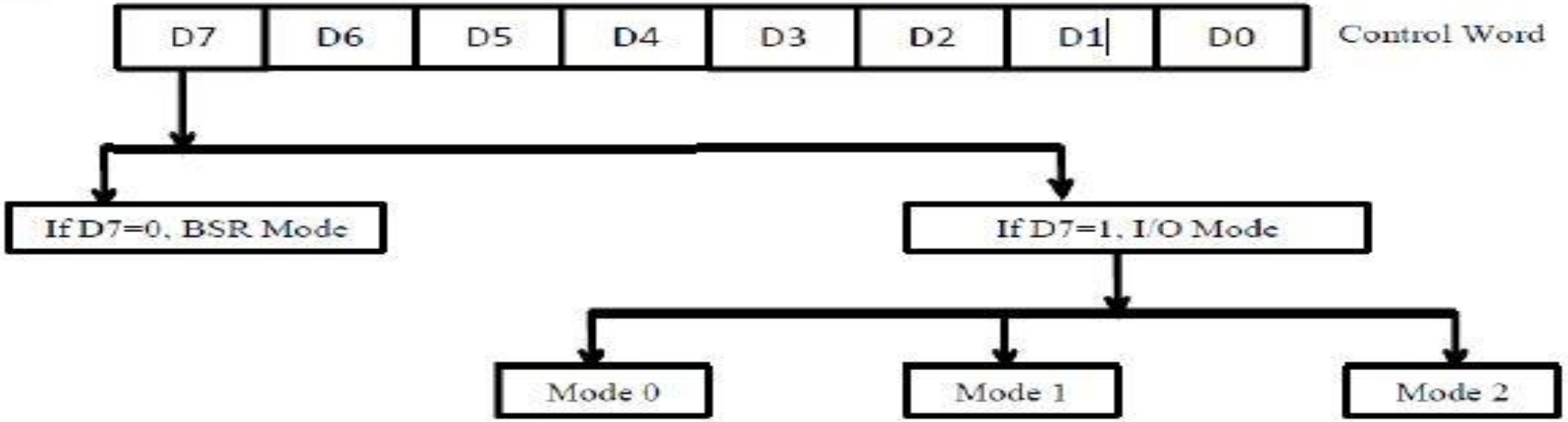

Fig (b): Control word specifying various modes

When D7=0, BSR mode
→ For port C
→ No effect on I/O mode and functions of port A and B
→ Individual bits of port C can be used for applications such as ON/OFF switch

When D7=1, I/O mode

i) Mode 0
   → Simple I/O interfacing for port A, B and C

ii) Mode 1
   → Interfacing with handshake signals for port A and B
   → Port C bits are used for handshake

iii) Mode 2
   → Bidirectional I/O interfacing for port A
   → Port B: either in mode 0 or mode 1
   → Port C bits used for handshake

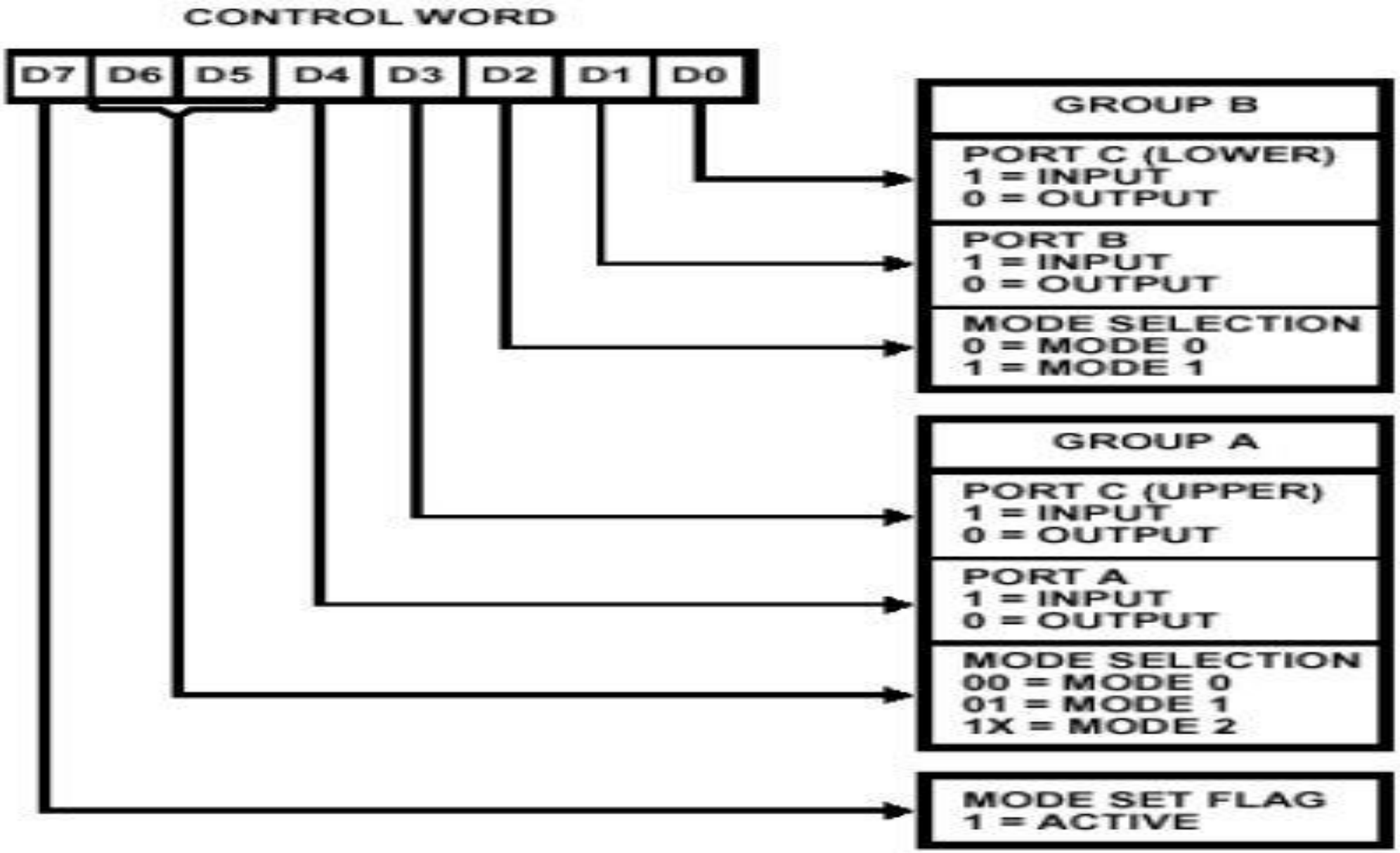

Fig: I/O Mode Definition Control Word Format

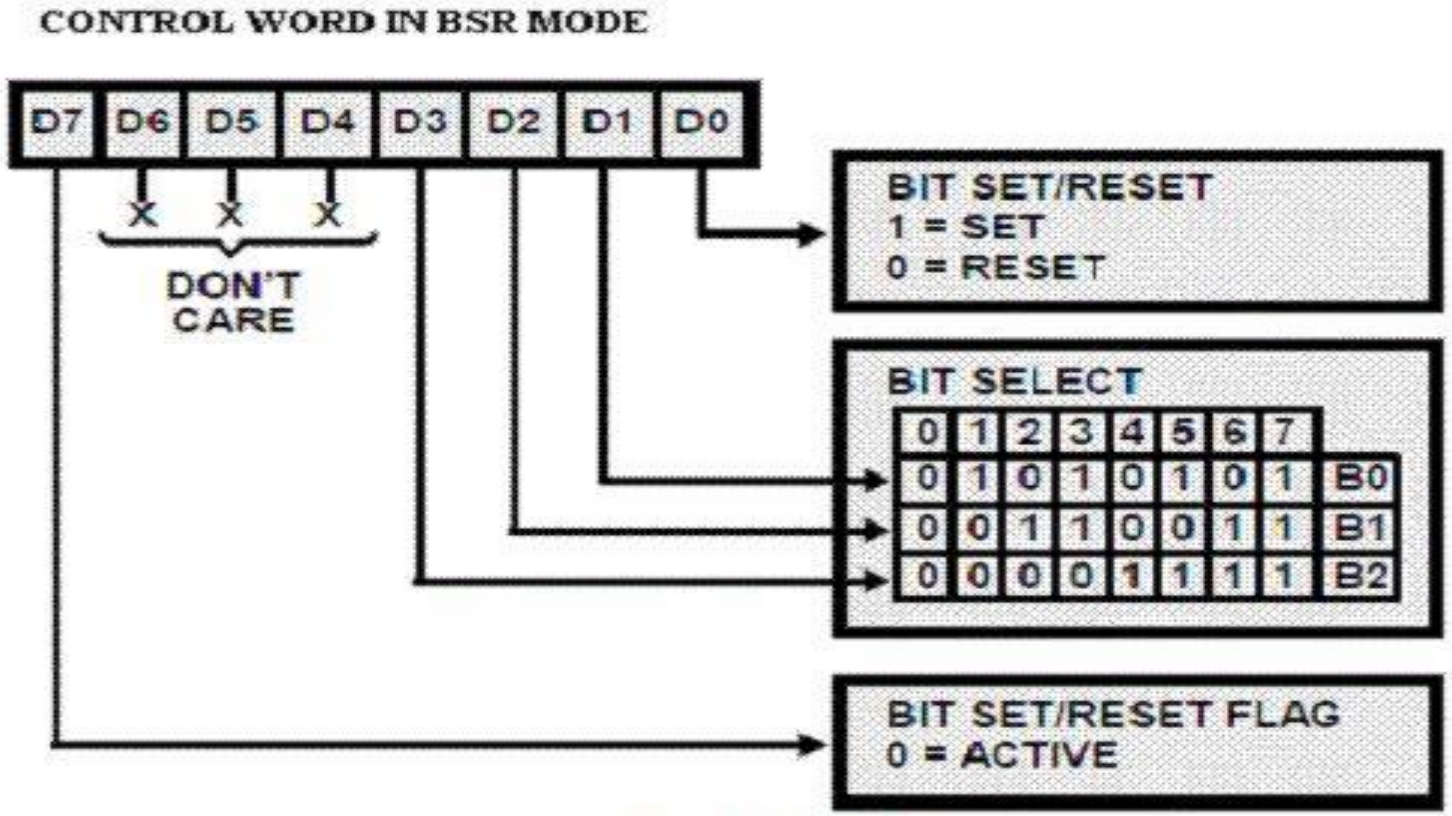

Fig: BSR Mode

- The content of control register is called control word specifying an input output functions for each port.
- The register can be accessed to write a control word when A_0 and A_1 are at logic 1. The register is not accessible for read operation.
- Bit D_7 of the control register specifies either I/O functions or Bit Set-Reset function as classified in figure (b).
- If bit D_7=1, bit D_6-D_0 determine I/O function in various modes as shown in figure (b).
- If bit D_7=0, port C operates in Bit Set-Reset mode.
- The BSR control word does not affect the function of port A and port B.

PROGRAMMABLE DMA CONTROLLER - INTEL 8257

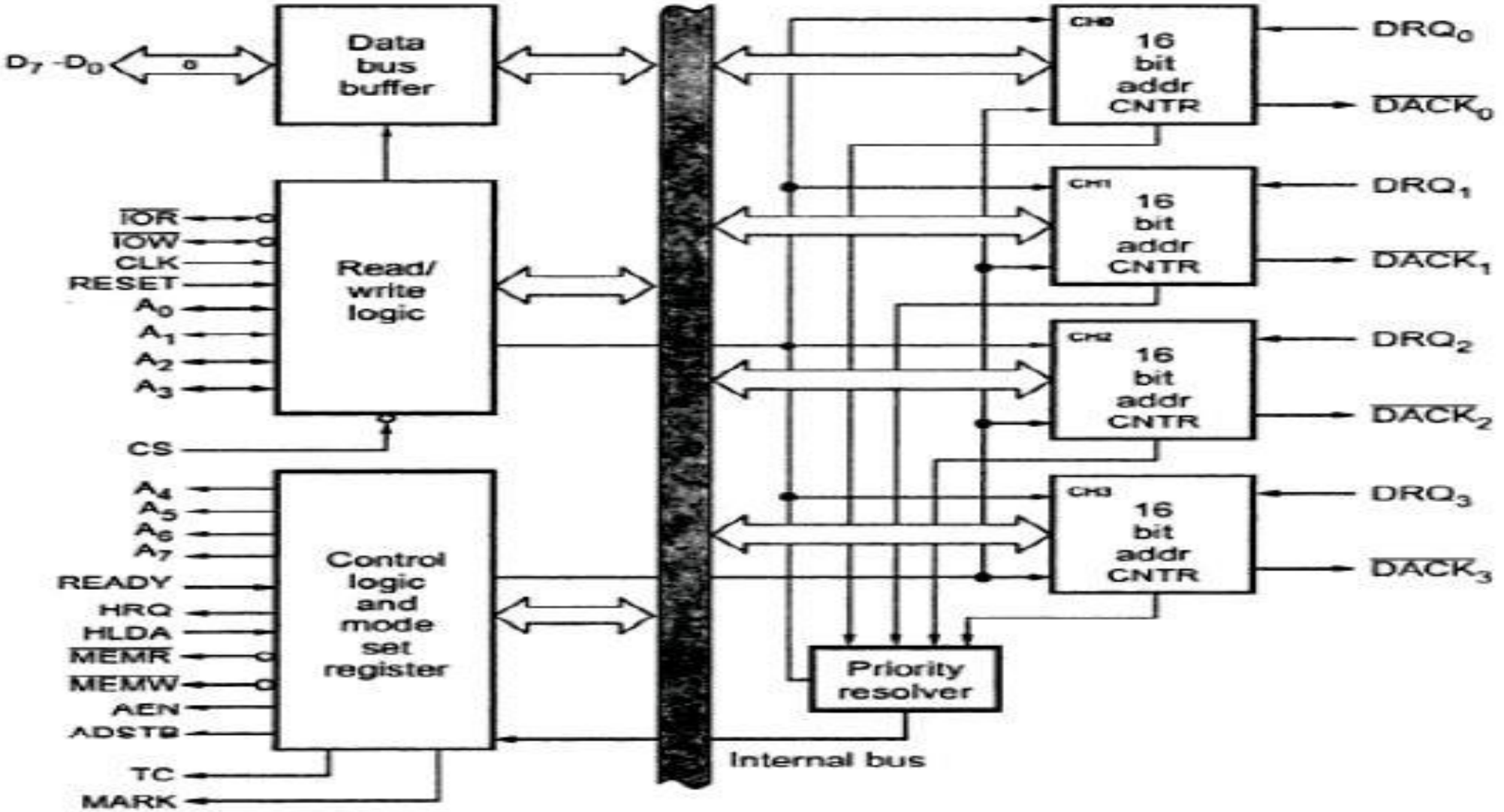

Fig: Functional block diagram of DMA Controller

It is a device to transfer the data directly between IO device and memory without through the CPU. So it performs a high-speed data transfer between memory and I/O device.

The features of 8257 is,

- The 8257 has four channels and so it can be used to provide DMA to four I/O devices.
- Each channel can be independently programmable to transfer up to 64kb of data by DMA.
- Each channel can be independently perform read transfer, write transfer and verify transfer.

The functional blocks of 8257 as shown in the above figure are data bus buffer, read/write logic, control logic, priority resolver and four numbers of DMA channels.

Operation of 8257 DMA Controller

- Each channel of 8257 has two programmable 16-bit registers named as address register and count register.
- Address register is used to store the starting address of memory location for DMA data transfer.
- The address in the address register is automatically incremented after every read/write/verify transfer.
- The count register is used to count the number of byte or word transferred by DMA.
- In read transfer the data is transferred from memory to I/O device.
- In write transfer the data is transferred from I/O device to memory.
- Verification operations generate the DMA addresses without generating the DMA memory and I/O control signals.
- The 8257 has two eight bit registers called mode set register and status register.

Introduction to 8251A PCI (Programmable Communication Interface)

- The 8251A is a programmable serial communication interface chip designed for synchronous and asynchronous serial data communication.
- It supports the serial transmission of data.
- It is packed in a 28 pin DIP.
- It is also called USART (Universal Synchronous Asynchronous Receiver Transmitter).

Block Diagram:

The functional block diagram of 8251A consists of five sections. They are:

- Read/Write control logic
- Transmitter
- Receiver
- Data bus buffer
- Modem control.

The functional block diagram is shown in fig:

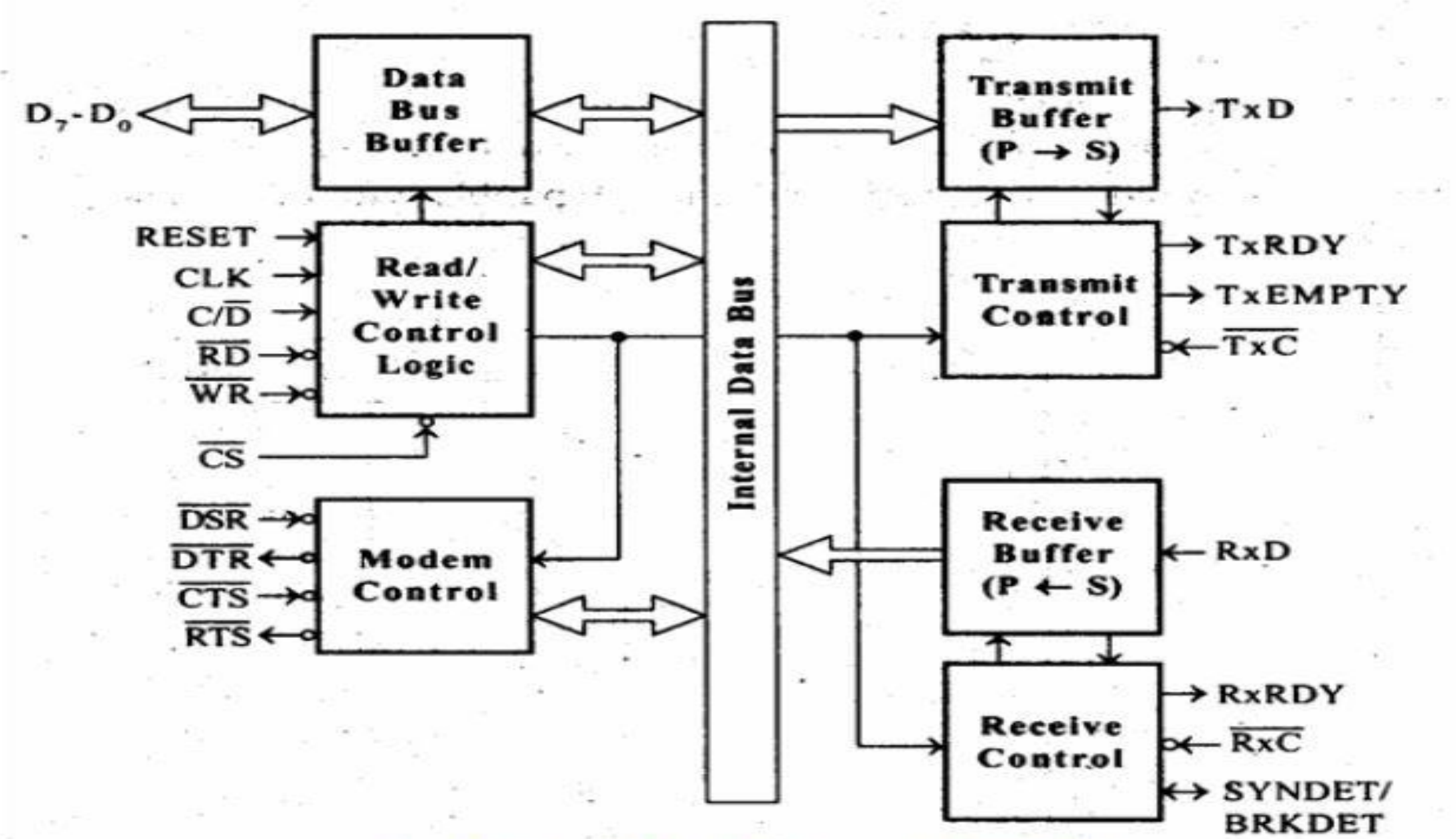

Fig: Functional block diagram of 8251A PCI

Read/Write control logic:

- The Read/Write Control logic interfaces the 8251A with CPU, determines the functions of the 8251A according to the control word written into its control register.
- It monitors the data flow.
- This section has three registers and they are control register, status register and data buffer.
- The eight parallel lines, D7-D0, connect to the system data bus so that data words and control/status words can be transferred to and from the device.
- The chip select (CS) input is connected to an address decoder so the device is enabled when addressed.
- The signals RD, WR, CS and C/D are used for read/write operations with these three registers.
- It has two internal addresses, a control address which is selected when C/D is high (1), and a data address which is selected when C/D input is low (0).
- When the RESET is high, it forces 8251A into the idle mode.
- The CLK (clock input) is necessary for 8251A for communication with CPU and this clock does not control either the serial transmission or the reception rate.

Transmitter section:

- The transmitter section accepts parallel data from CPU and converts them into serial data.
- The transmitter section is double buffered, i.e., it has a ***buffer register*** to hold an 8-bit parallel data and another register called ***output register*** to convert the parallel data into serial bits.
- When output register is empty, the data is transferred from buffer to output register. Now the processor can again load another data in buffer register.
- If buffer register is empty, then TxRDY goes high.
- If output register is empty then TxEMPTY goes high.
- The clock signal, TxC controls the rate at which the bits are transmitted by the USART.
- The clock frequency can be 1, 16 or 64 times the baud rate.

Receiver Section:

- The receiver section accepts serial data and convert them into parallel data
- The receiver section is double buffered, i.e., it has an *input register* to receive serial data and convert to parallel, and a *buffer register* to hold the parallel data.
- When the RxD line goes low, the control logic assumes it as a START bit, waits for half a bit time and samples the line again.
- If the line is still low, then the input register accepts the following bits, forms a character and loads it into the buffer register.
- The CPU reads the parallel data from the buffer register.
- When the input register loads a parallel data to buffer register, the RxRDY line goes high.
- The clock signal RxC controls the rate at which bits are received by the USART.
- During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.
- During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

MODEM Control:

- The MODEM control unit allows to interface a MODEM to 8251A and to establish data communication through MODEM over telephone lines.
- This unit takes care of handshake signals for MODEM interface.

Programmable Interrupt Controller: The 8259A

The 8259A is a programmable interrupt-managing device, specifically designed for use with the interrupt signals (INTR/INT) of the 8085 MP.

The 8259A block diagram includes control logic, registers for interrupt requests, priority resolver, cascade logic, and data bus. The registers manage interrupt requests; the priority resolver determines their priority. The cascade logic is used to connect additional 8259A devices.

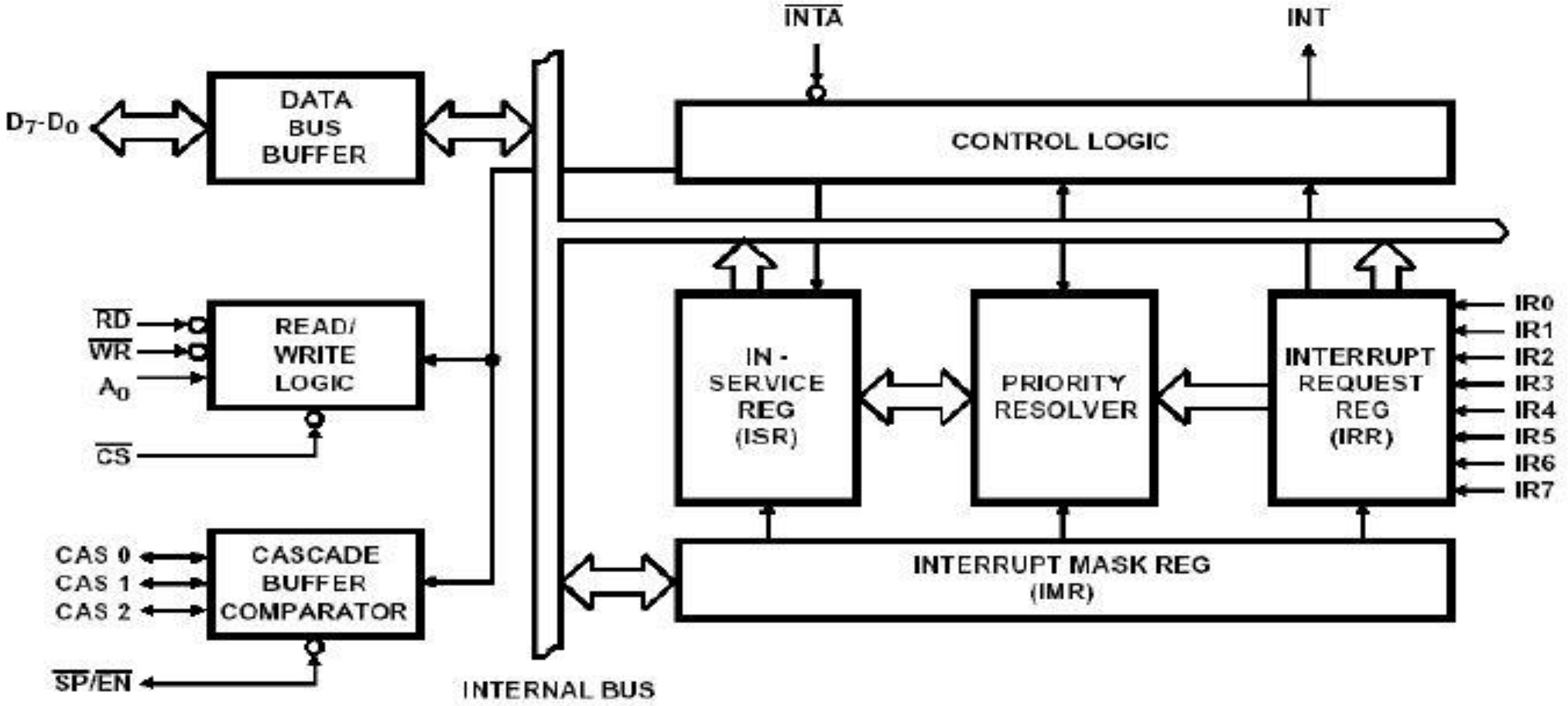

Fig: Block Diagram of 8259A PIC

The internal block diagram of the 8259 includes eight block

I. Control Logic
II. Read/Write Logic
III. Data Bus Buffer
IV. Three Registers IRR, ISR, and IMR
V. Priority Resolver and
VI. Cascade Buffer

Read/Write Logic

When the address line A0 is at logic 0, the controller is selected to write a command or read a status.

Control Logic

- This block has two pins INT (interrupt) as an output, $\overline{\text{INTA}}$(Interrupt Acknowledge) as an input.
- The INT is connected to the interrupt pin of the μP. Whenever a valid interrupt is asserted, this signal goes high. The $\overline{\text{INTA}}$ is the Interrupt Acknowledge signal from the μP.

Interrupt Registers and Priority Resolver

- The Interrupt Request Register (IRR) has eight input lines (IR0-IR7) for interrupts. When these lines go high, the requests are stored in the register

- The In-Service Register (ISR) stores all the levels that are currently being serviced, and the Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked
- The Priority Resolver (PR) examines these three registers and determines whether INT should be sent to the µP

Cascade Buffer/Comparator

- This block is used to expand the number of interrupt levels by cascading two or more 8259s

Interrupt Operation

To implement interrupts, the Interrupt Enable flip-flop in the µP should be enabled by writing the EI instruction, and the 8259 requires two types of control words; Initialization Command Words (ICWs) and Operational Command Words (OCWs)

ICWs:

ICWs are used to set up the proper conditions and specify RST vector addresses.

OCWs:

OCWs are used to perform functions such as masking interrupts, setting up status-read operations, etc.

The following steps take place during the operation of 8259A:

i) One or more interrupt request lines go high requesting the service.
ii) The 8259A resolves the priorities and sends an INT signal to the MP.
iii) The MP acknowledges the interrupt by sending INTA(bar).

iv) After the INTA(bar) has been received, the op-code for the call instruction (CDH) is placed on the data bus.
v) Because of the CALL instruction, the MP sends two more INTA(bar) signals.
vi) At the first INTA(bar), the 8259A places the low-order 8-bit address on the data bus and at the second INTA(bar), it places the high-order 8-bit address of the interrupt vector. This completes the 3-byte CALL instruction.
vii) The program sequence of the MP is transferred to the memory location specified by the CALL instruction.

Priority modes

i) Fully Nested mode
→ IR0 has the highest priority and the following IR1, IR2, IR3..... etc. have the decreasing priorities.
ii) Automatic rotation mode
→ First priority changes to the last after its service.
iii) Specific rotation mode
→ This is user selectable or programmable, which means priority can be selected by programming.

Features

i) It manages 8 interrupt requests.
ii) It can vector an interrupt request anywhere in the memory map through program control without additional hardware for restart instructions. However, all 8 requests are spaced at the interval of either 4 locations or 8 locations.
iii) It can solve 8 levels of interrupt priorities in a variety of modes.
iv) With cascading additional 8259A devices, the priority scheme can be expanded to 64 levels.
v) The 8259A has the abilities such as reading the status and changing the interrupt mode during a program execution.
vi) It can mask each interrupt request individually.
vii) It can be set up to work with either the 8085 MP mode or the 8086/8088 MP mode.