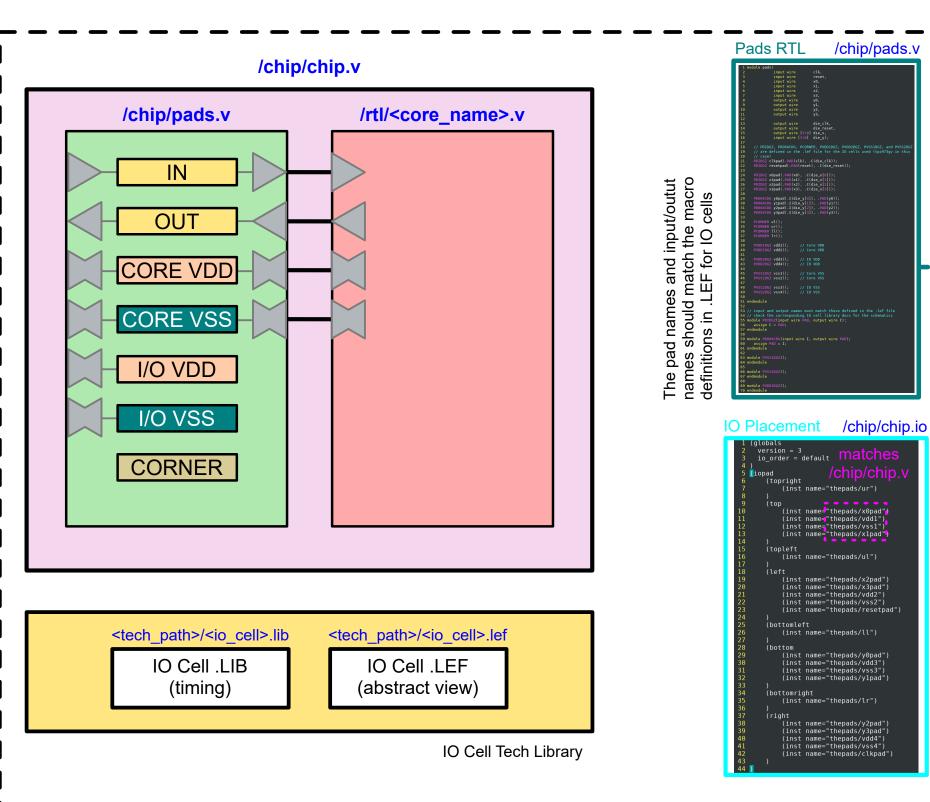


Padframe implemenation



/chip/chip.v

die_clk;
die_reset
die_x;
die_y;

wire wire wire [3:0] wire [3:0]

pads thepads(.clk(clk),

.x0(x0) .x1(x1) .x2(x2) .x3(x3)

mavg thecore(.x(die_x), .y(die_y), .reset(die_reset) .clk(die_clk));

Core RTL /rtl/<core_name>.v

always @(posedge clk or posedge reset) bo if (reset) begin

reg [3:0] tap0, tap1, tap2;
reg [3:0] newtap0, newtap1,

tap0 <- 4 b0, tap1 <= 4'b0; tap2 <= 4'b0; end else begin

always @(*) begin newtap0 = x; newtap1 = tap0; newtap2 = tap1; sum0 = tap0 + x; sum1 = sum0 + tap0

tap1 <= newtap1 tap2 <= newtap2

sum1 = sum0 + tap1; sum2 = sum1 + tap2 + 6'h2; sum2scaled = sum2[5:2];

.,3(,3), .y0(y0), .y1(y1), .y2(y2), .y3(y3), .die_clk(die_clk),