Digital design flow with Cadence Tools

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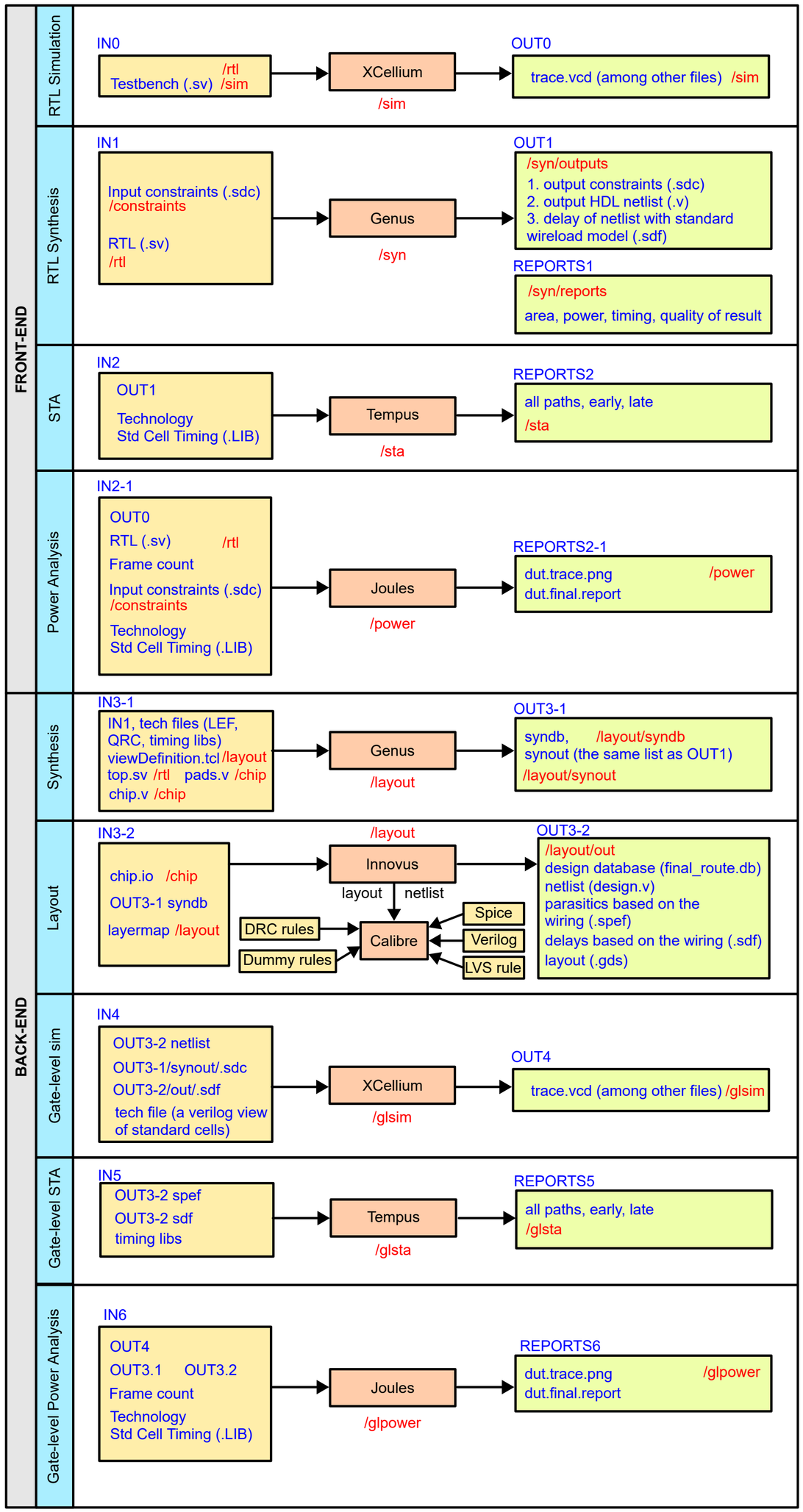
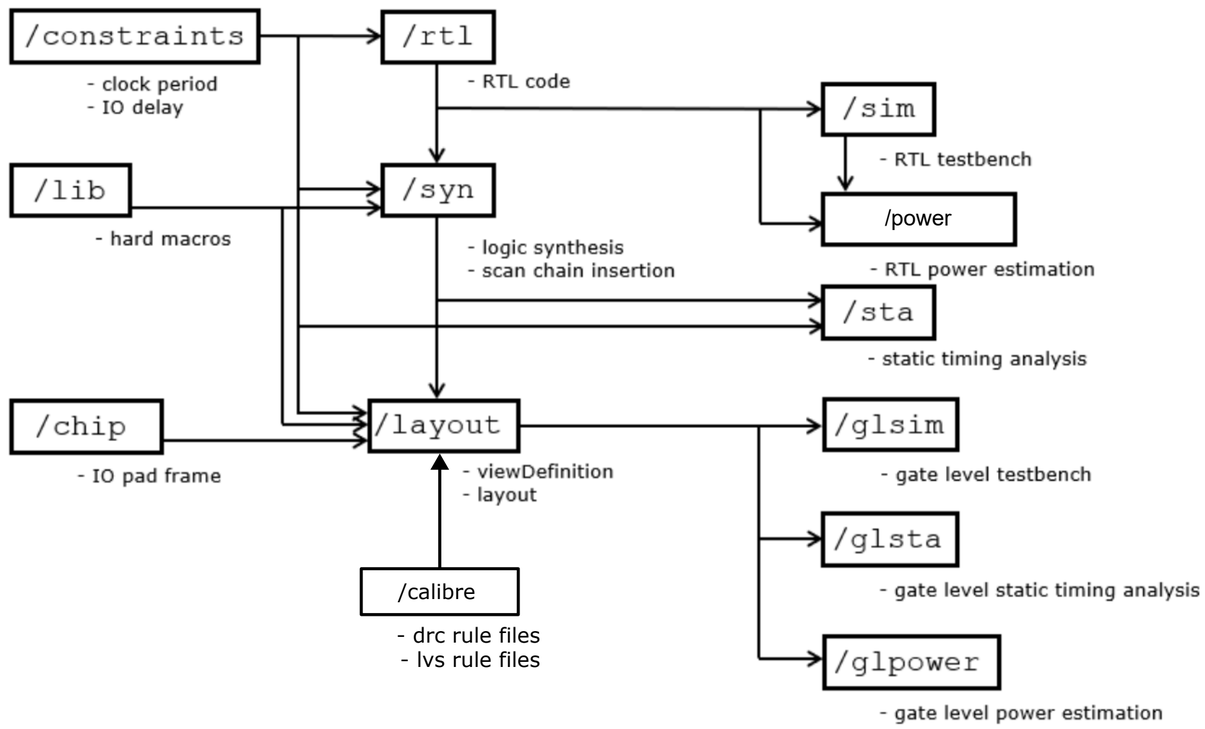
directory file





- `/rtl` contains the register-transfer level code of the design.
- `/sim` contains the testbench of the design, and possible test-vectors. The design is simulated with **Xcelium**, and the `Makefile` must be properly configured with (System)Verilog file names.
- `/constraints` contains the input/output delay constraints and the synthesis clock period of the design in an `.sdc` file. The input/output delay constraints can be adjusted by editing this SDC file.
- `/syn` contains the logic synthesis and test vector generation scripts, used by **Genus** and **Modus** respectively. The `Makefile` must be properly configured with synthesis configuration parameters including the technology library. In addition, the synthesis script can be tweaked to modify the optimization level, introduce hard macro's, etc.
- `/power` contains the RTL power estimation script, which uses the RTL VCD files as well as the RTL source code. The `Makefile` must be properly configured with power estimation parameters, including the number of frames to use (1 to 1000 or twice the number of clock cycles in the VCD, whatever is smaller). **Joules** estimates power as a graph and a data file.
- `/lib` allocates the behavioral (verilog), timing (lib) and layout (lef) views of any hard macros used in the design. In our case, .lib and .lef files are located separately to ensure consistency among multiple designs.
- `/sta` performs static timing analysis using **Tempus**. The STA script needs tuning according to the design parameters.
- `/chip` defines the block pin allocation or the padframe of the chip, depending on whether you do a block-level design or a full-chip design.
- `/layout` creates the final layout using **Genus** and **Innovus**. The `Makefile` defines relevant design parameters including the libraries to use. The synthesis and layout scripts need manual tuning to enable the use of hard macros and other custom steps.
- `/glsim` performs gate-level simulation using the final netlist produced from the design. This final netlist uses delay information (SDF) computed from the layout data.
- `/glsta` performs gate-level STA using the final netlist produced from the design using **Tempus**. The STA uses parasitic information (SPEF) produced from the layout data.
- `/glpower` performs gate-level power esimation using the final netlist produced from the design, and the VCD computed during gate-level simulation.

Source: Prof. Schaumont's ECE574-F24 course at WPI
URL: https://schaumont.dyn.wpi.edu/ece574f24/10fclayout.html