INDIAN INSTITUTE OF TECHNOLOGY PATNA

EC3102: VLSI DESIGN

GROUP PROJECT

Design & Analysis of Precharge Circuits for SRAM using only NMOS and only PMOS

Team Details:
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Objective:

The objective of this project is to design and analyze SRAM precharge circuits using only NMOS transistors and only PMOS transistors for four different circuit topologies labeled (a), (b), (c), and (d). The following metrics were obtained from simulation for each design:

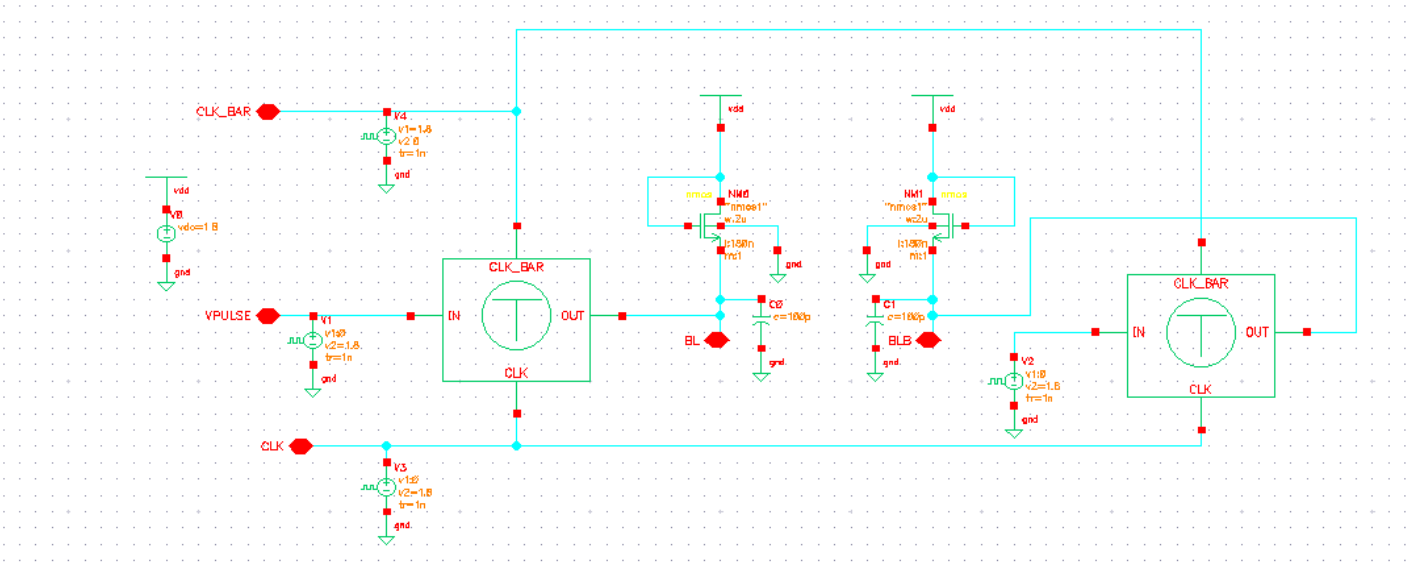
1. Transient Analysis Waveform
2. Propagation delay
3. Average static power
4. Average dynamic power

All circuits were simulated under identical bias, load(100pF), and stimulus conditions, enabling direct comparison of performance results.

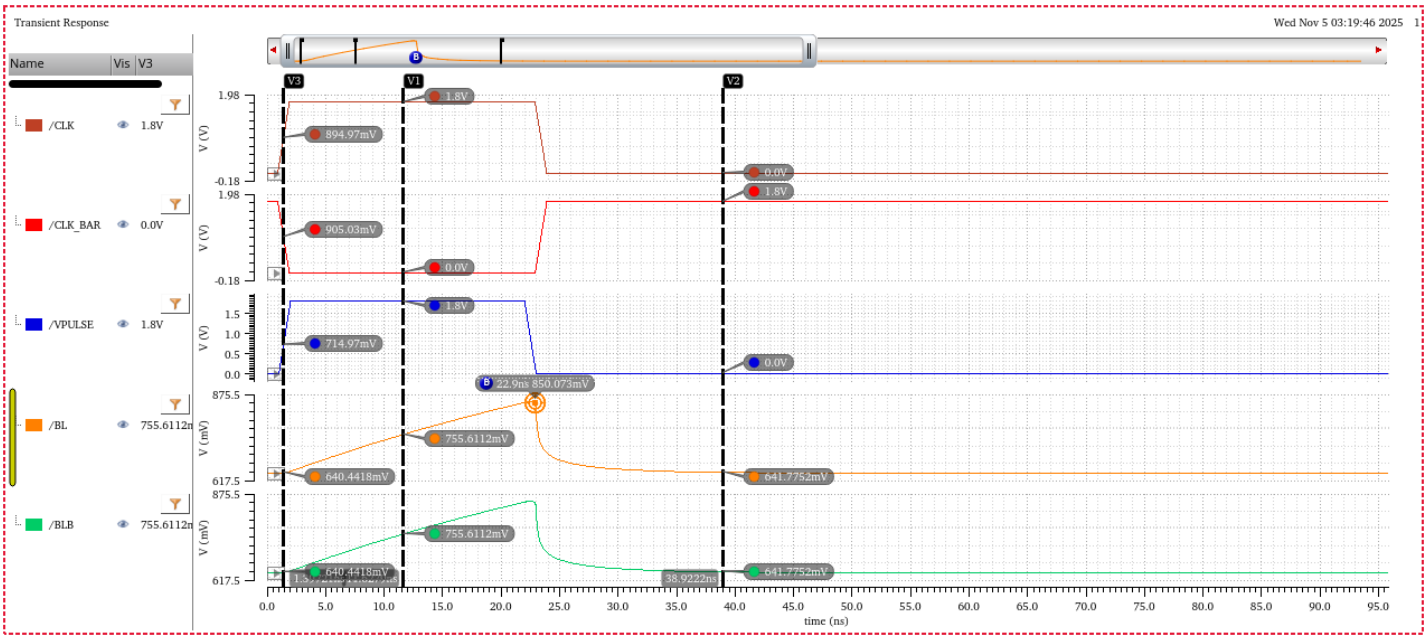
Software and Technology Node Used: Cadence Virtuoso, gpdk 180 node

CIRCUIT DIAGRAMS, SIMULATION RESULTS & CALCULATIONS:

1. Circuit (a) – NMOS only

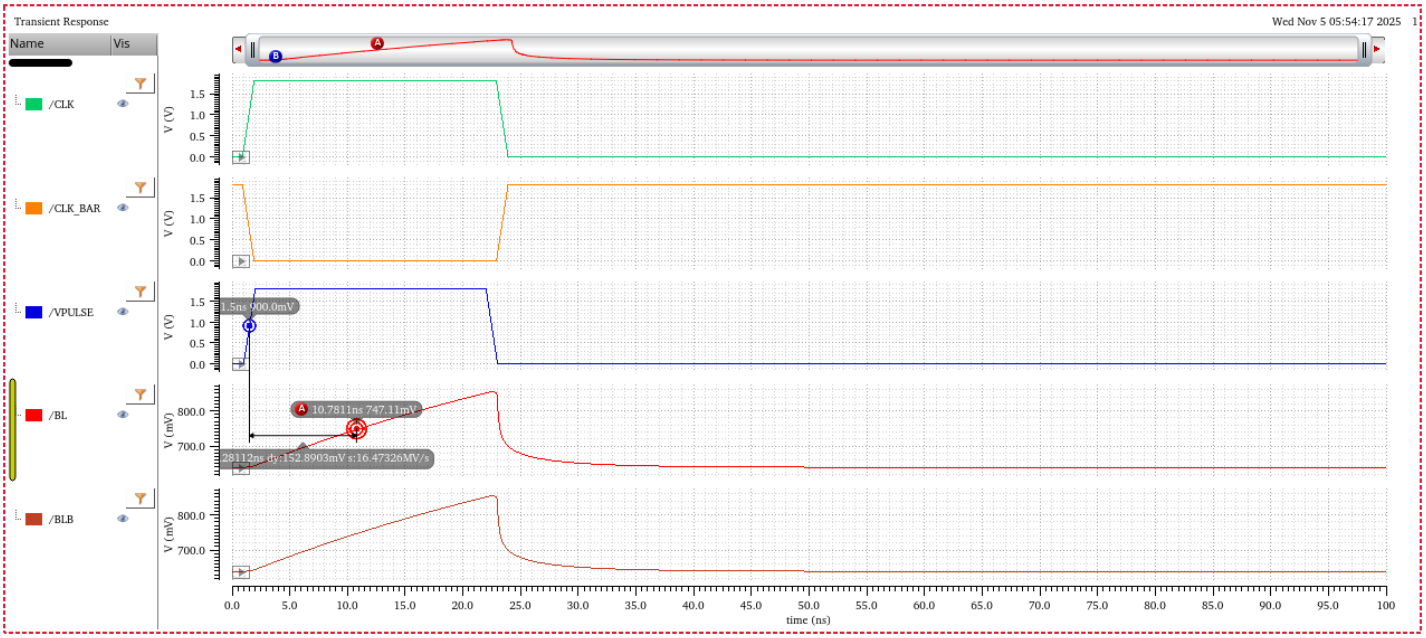


TRANSIENT ANALYSIS:

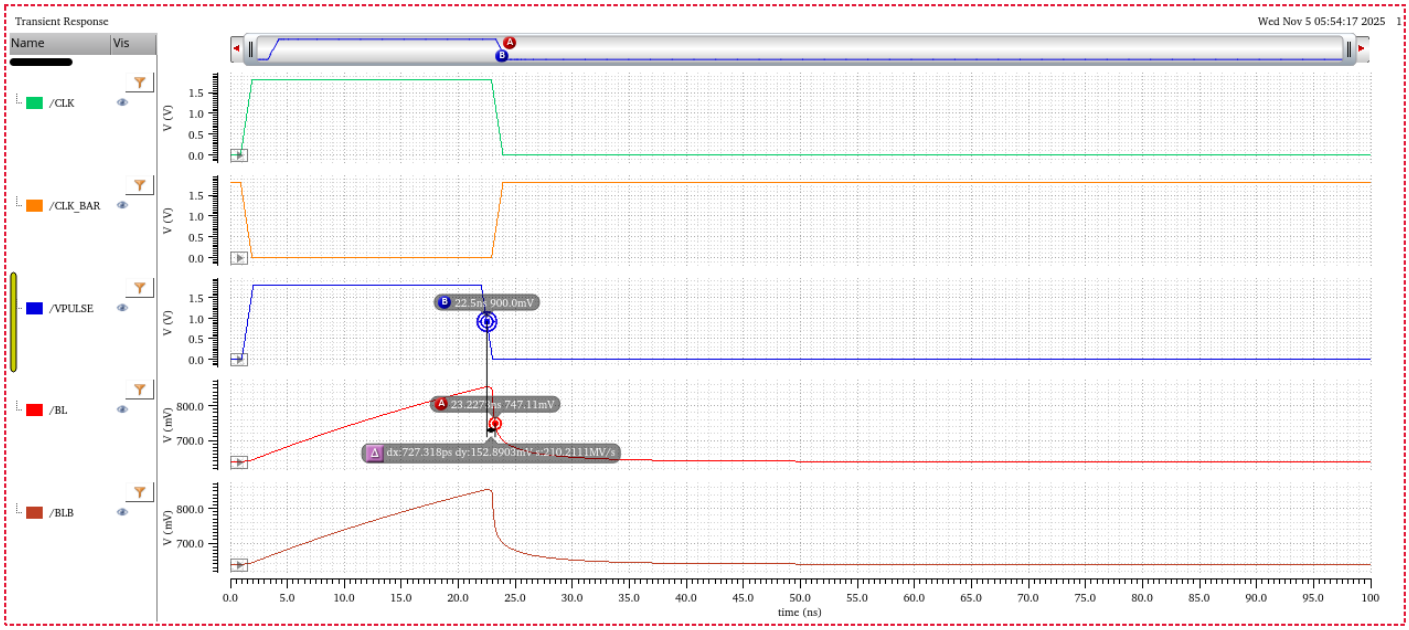


TIME DELAY CALCULATION:

A) T_PLH

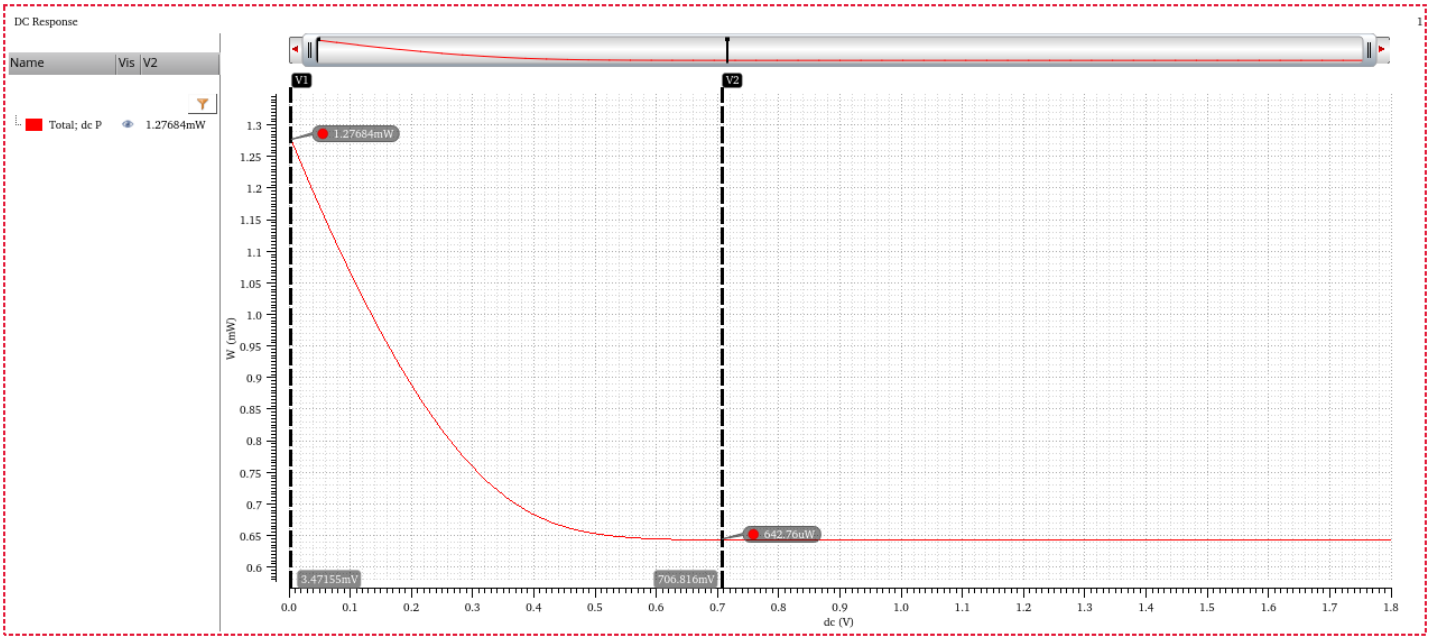


B)T_PHL



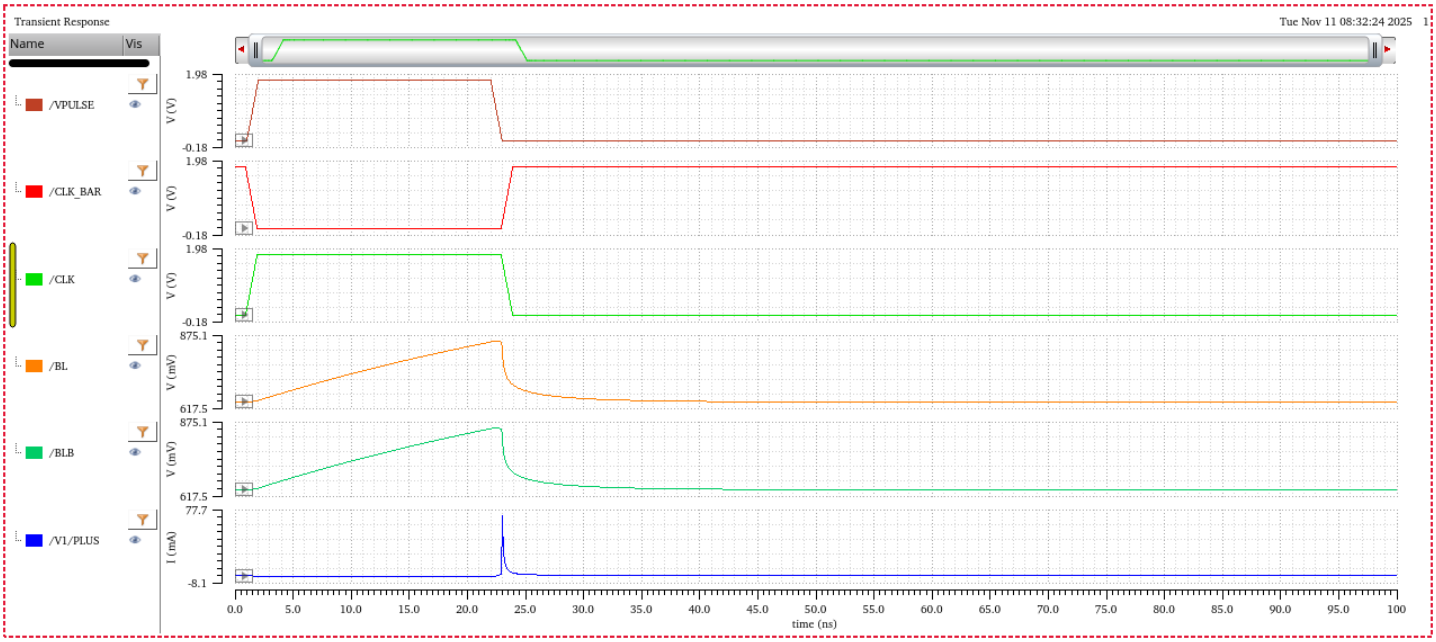
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (9281.1 ps + 727.318 ps)/2 = 5001.209 fs = 5.001209 ns

STATIC POWER ANALYSIS:



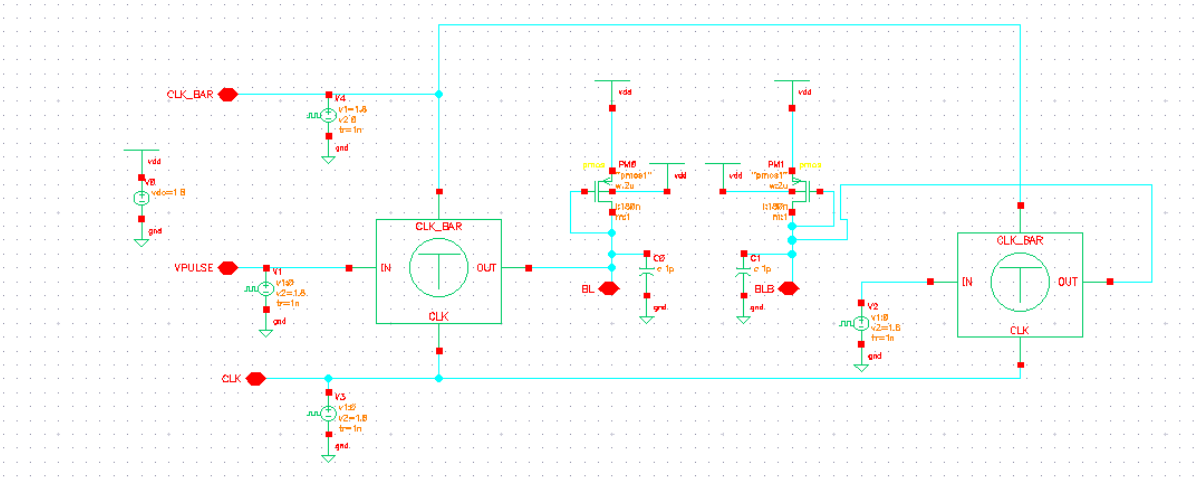
Average static power: 0.9598 mW

DYNAMIC POWER ANALYSIS:

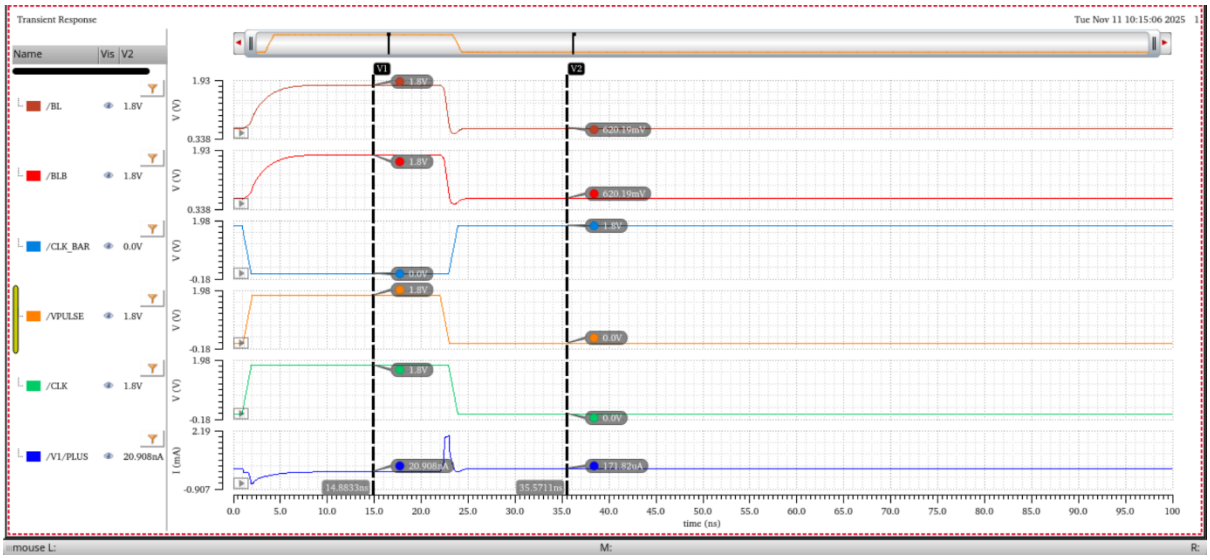


Average dynamic power: 322.7 uW

2. Circuit (a) – PMOS only

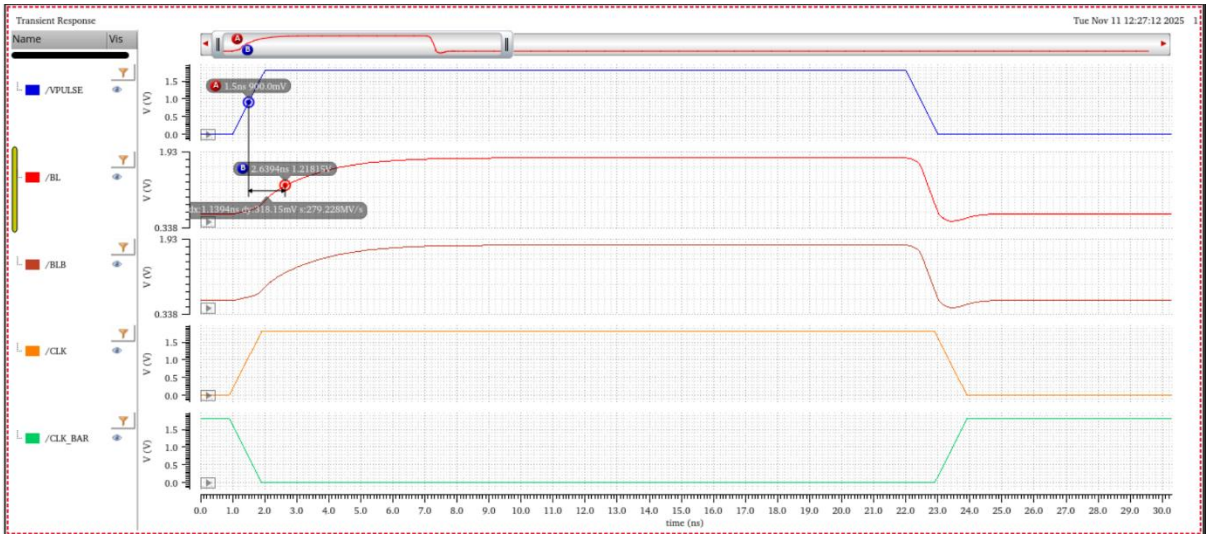


TRANSIENT ANALYSIS:

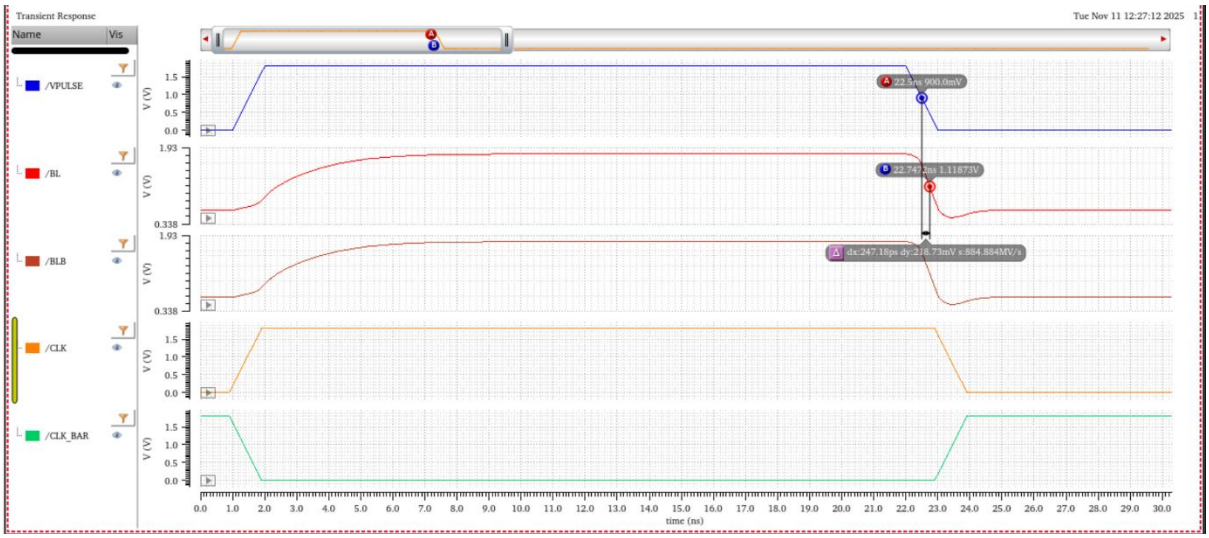


TIME DELAY CALCULATION:

A) T_PLH

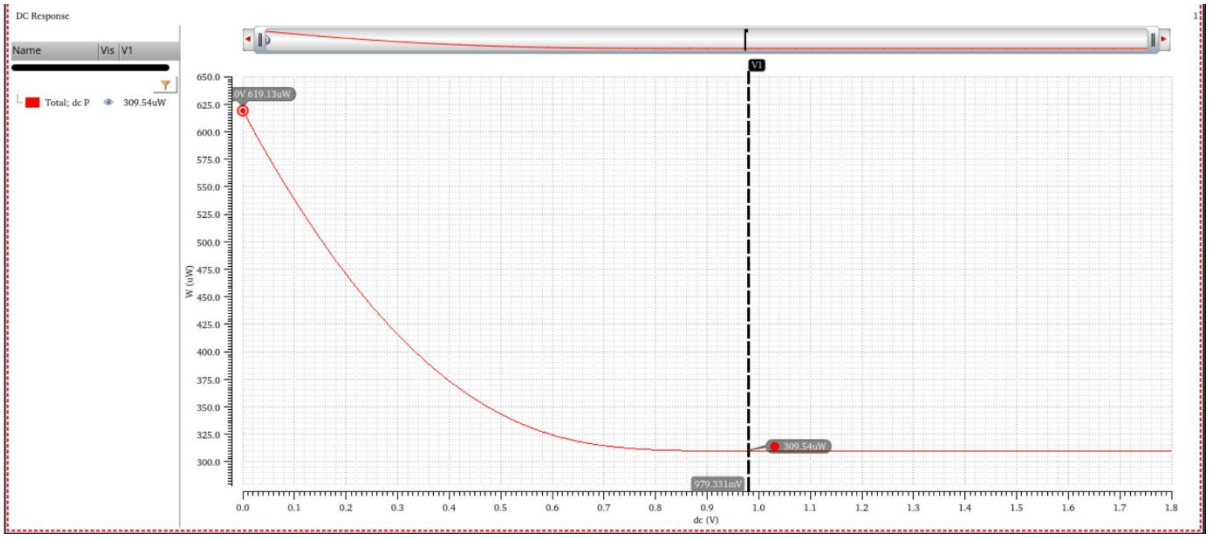


B)T_PHL



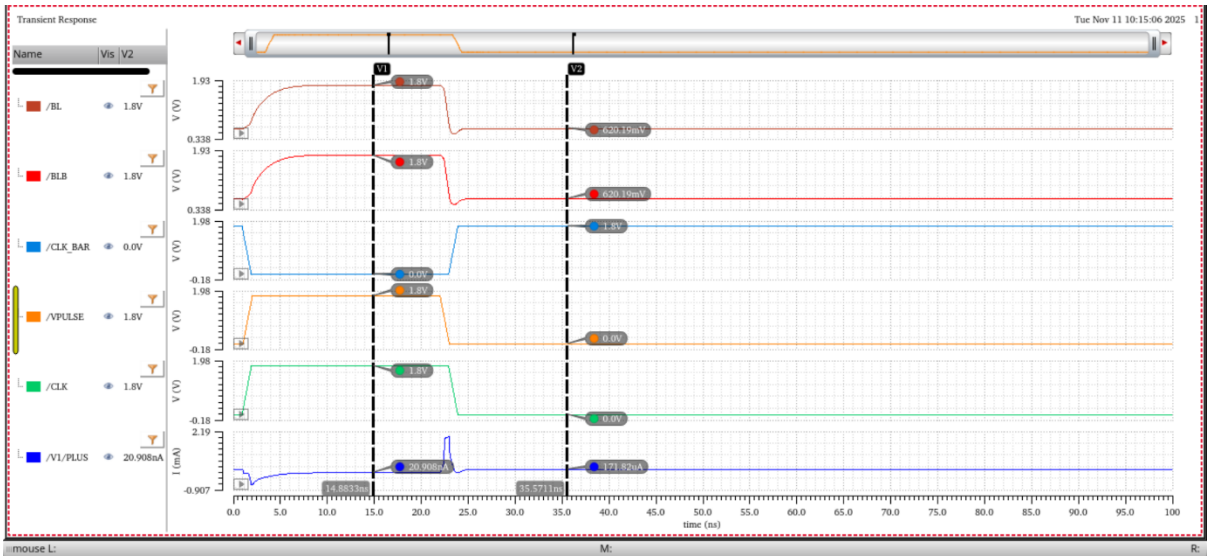
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (1139.4ps + 247.18ps)/2 = 1386.58 ps

STATIC POWER ANALYSIS:



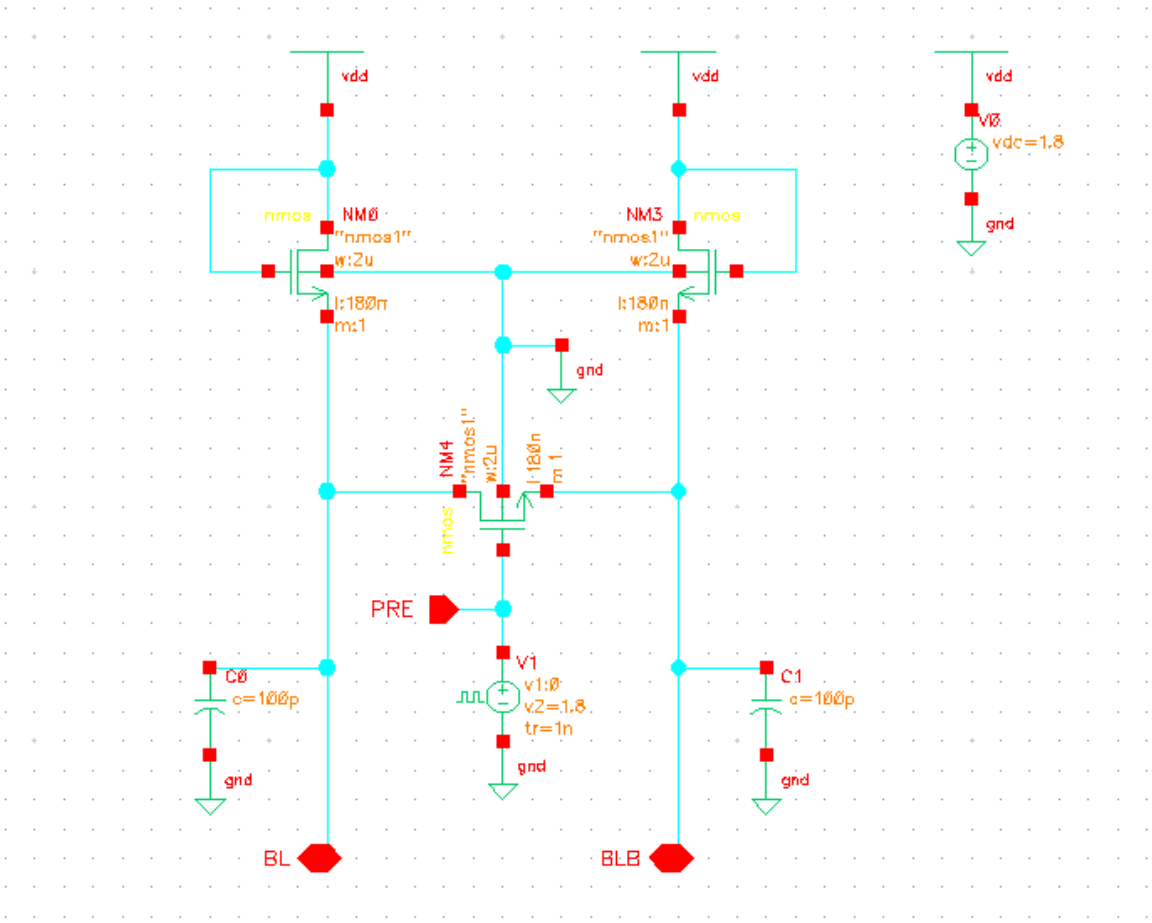
Average static power: 0.464335 mW

DYNAMIC POWER ANALYSIS:

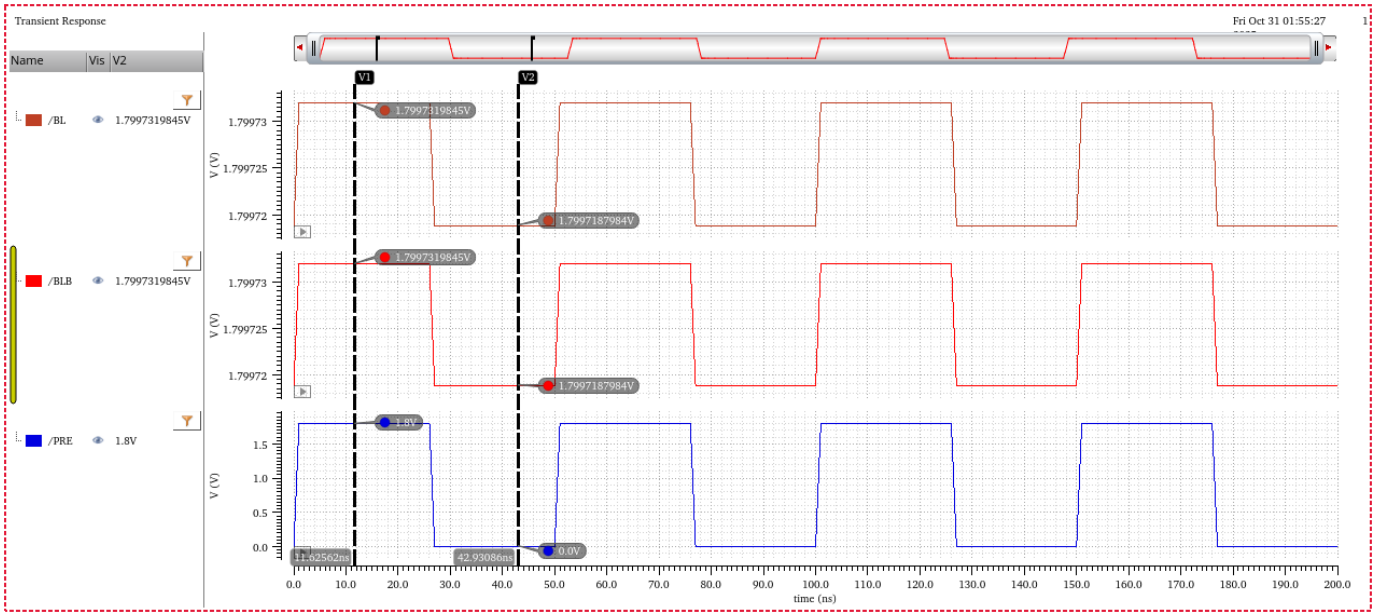


Average dynamic power: 136.3 uW

3. **Circuit (b) – NMOS only**

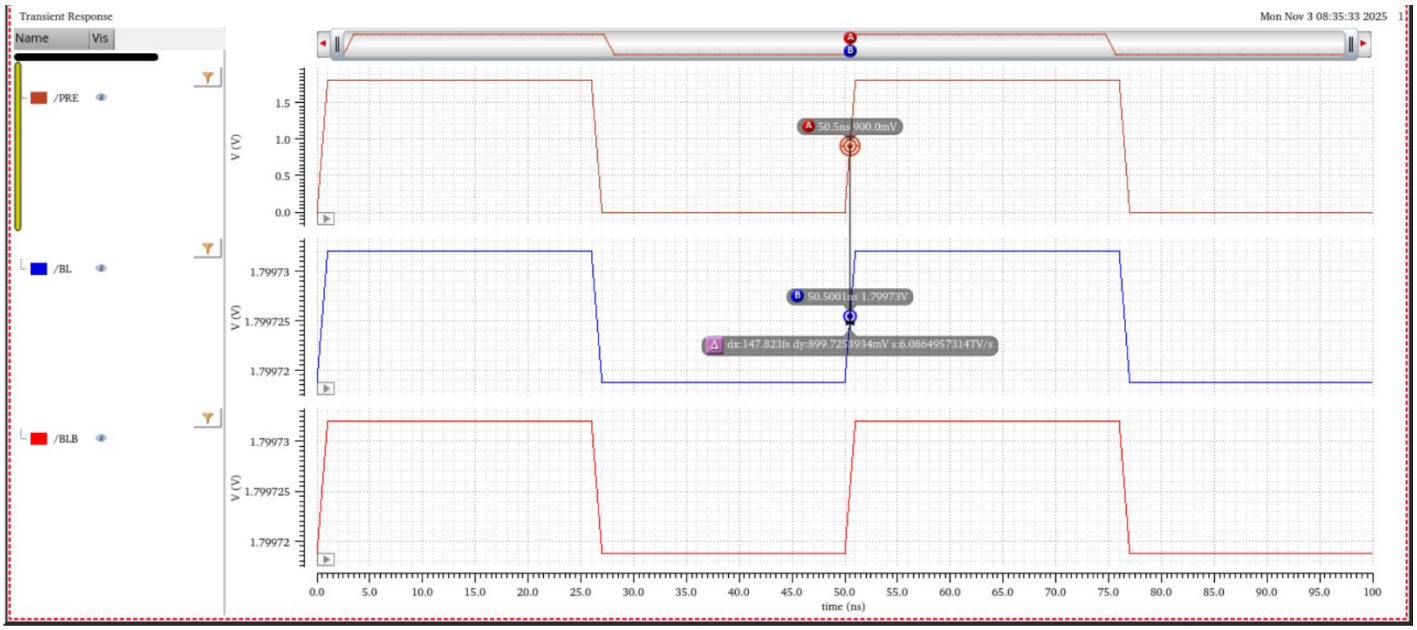


TRANSIENT ANALYSIS:

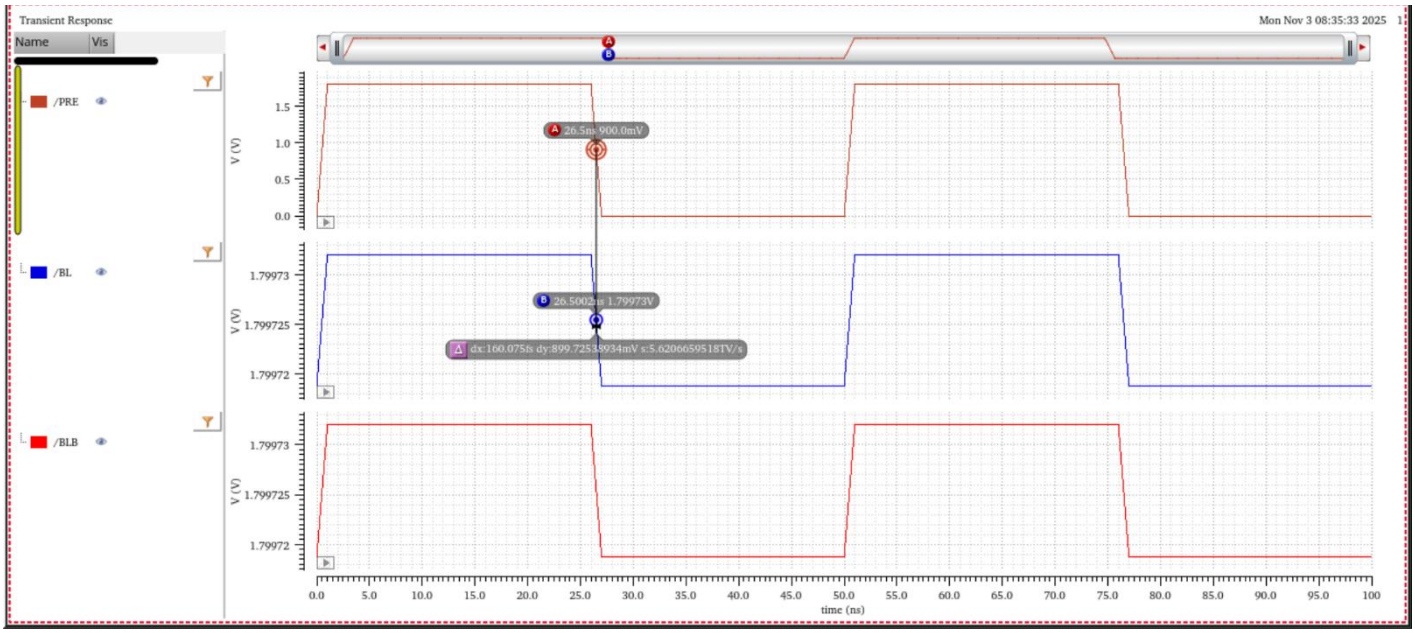


TIME DELAY CALCULATION:

A) T_PLH

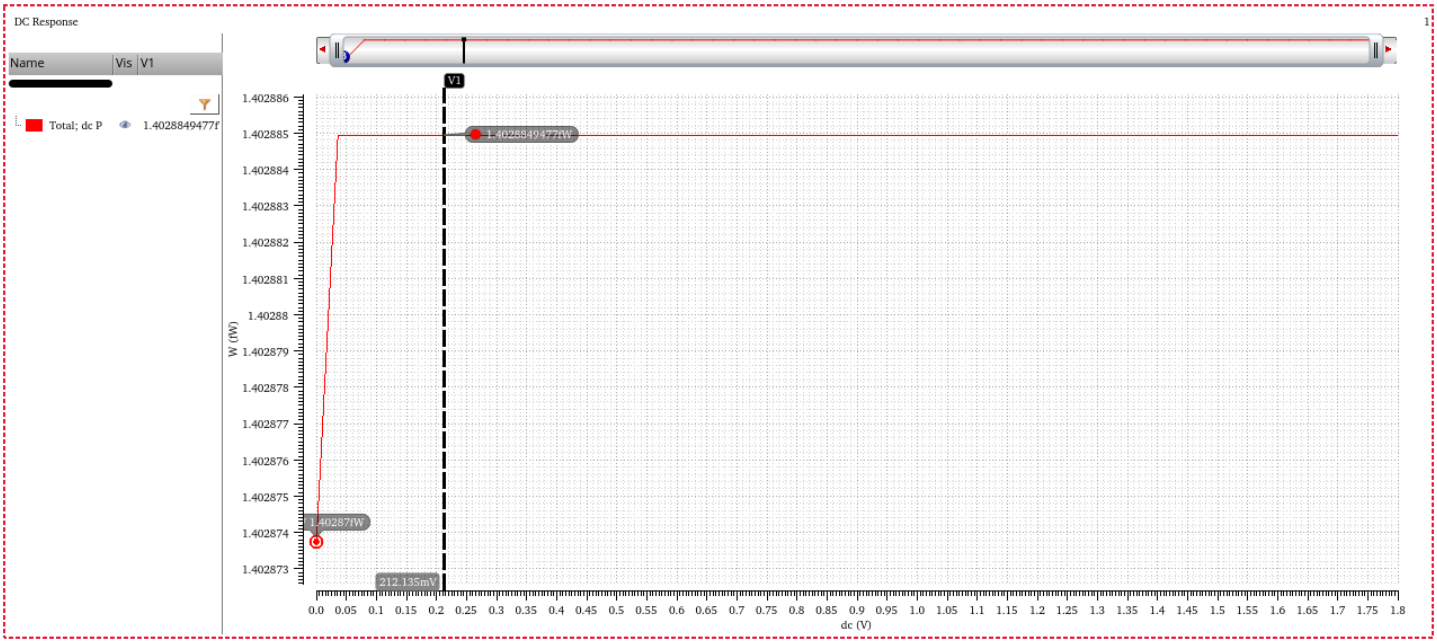


B)T_PHL



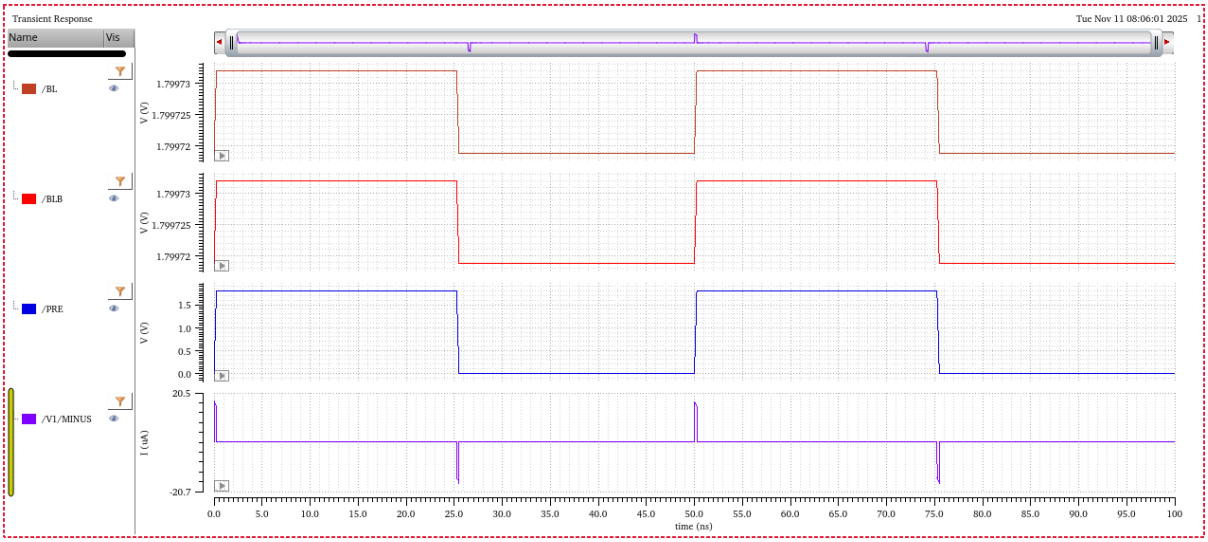
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (147.823 fs + 160.075 fs)/2 = 153.949 fs

STATIC POWER ANALYSIS:



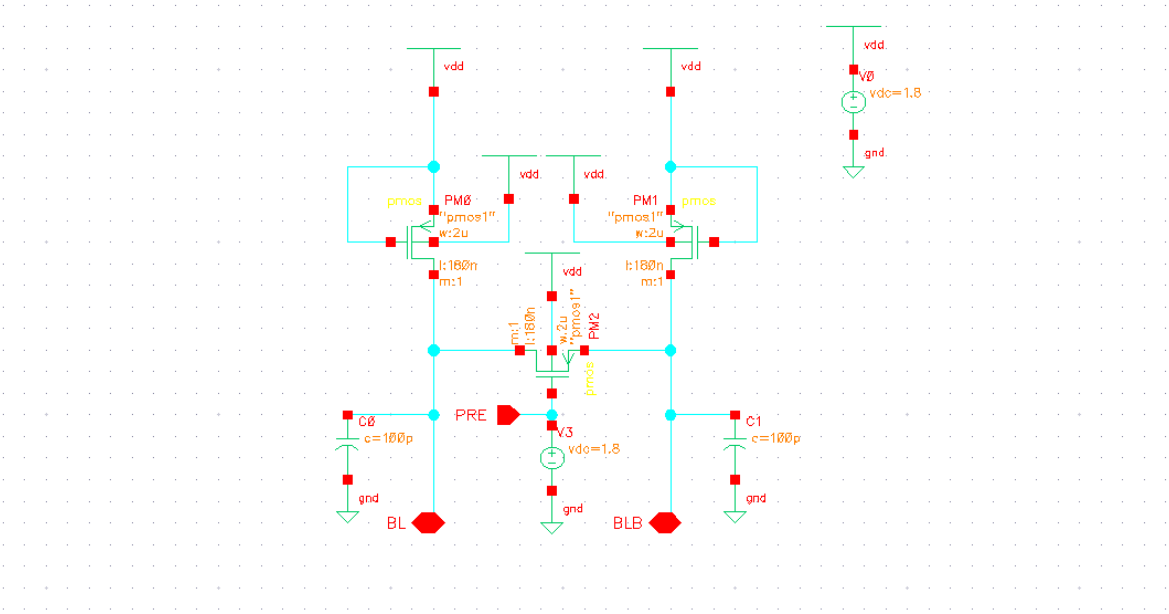
Average static power: 1.40287747385 fW

DYNAMIC POWER ANALYSIS:

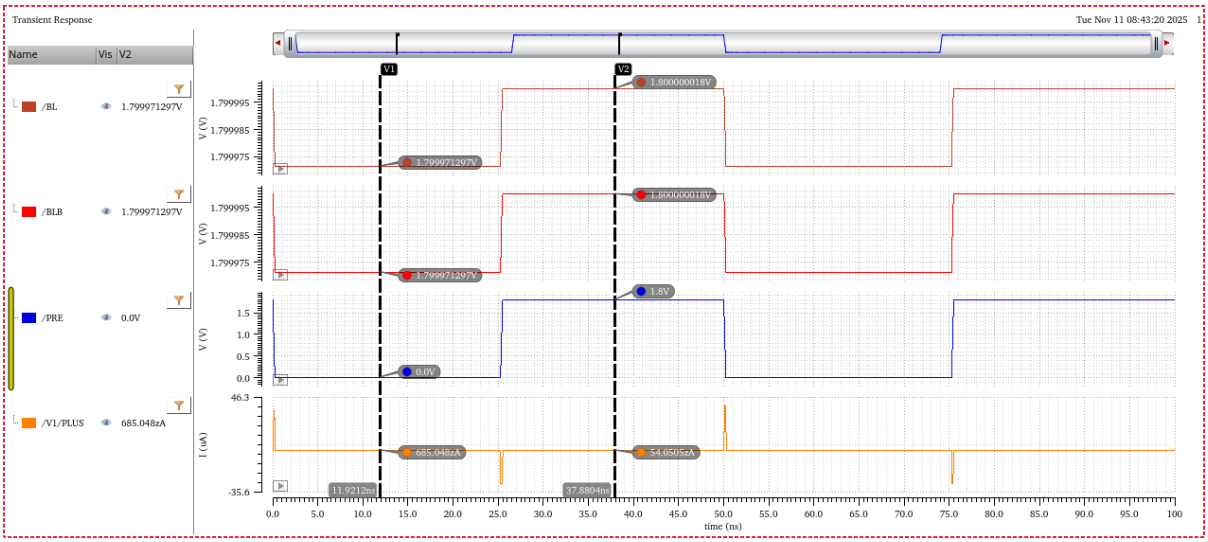


Average dynamic power: 1.298 nW

4. Circuit (b) – PMOS only

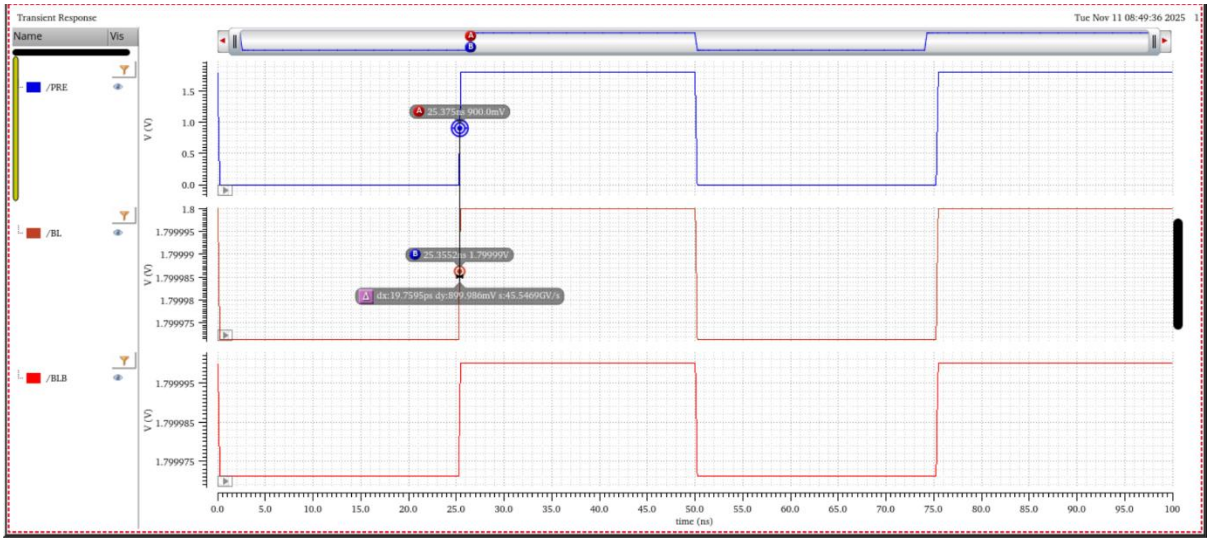


TRANSIENT ANALYSIS:

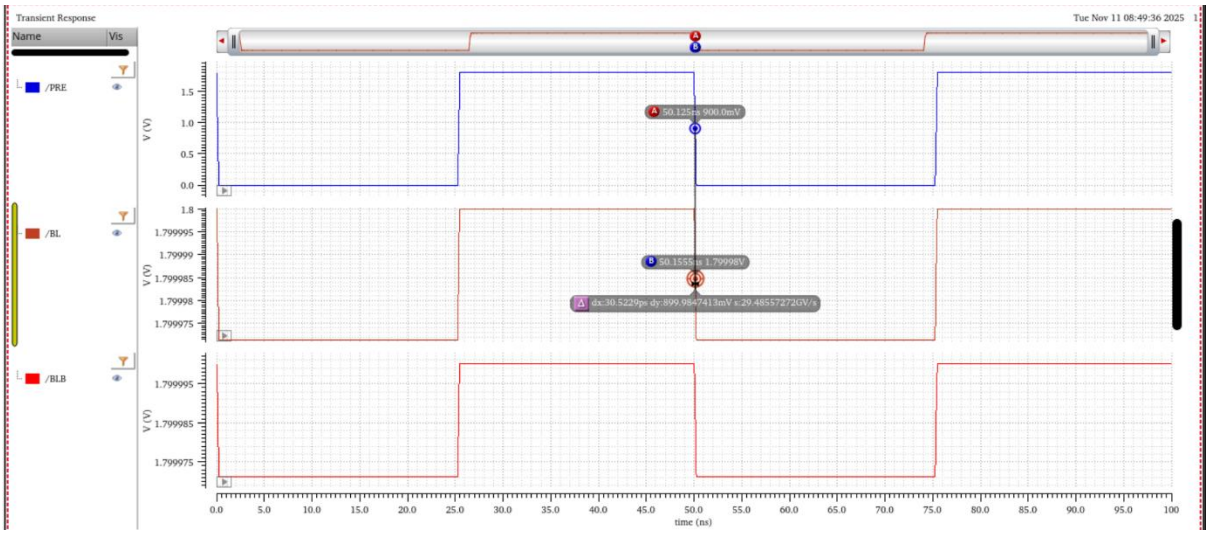


TIME DELAY CALCULATION:

A) T_PLH

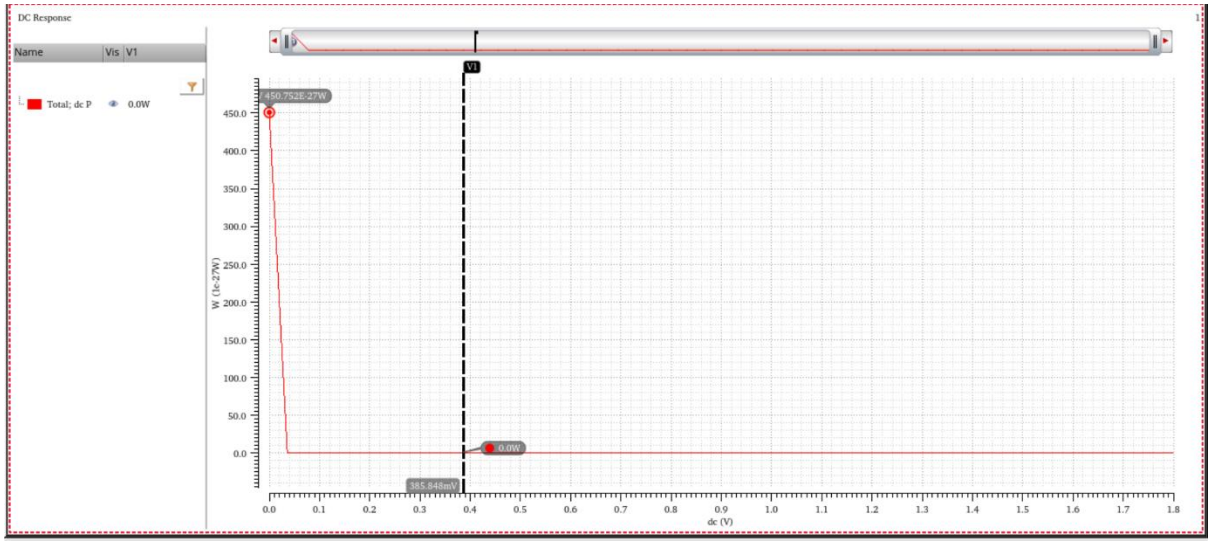


B)T_PHL



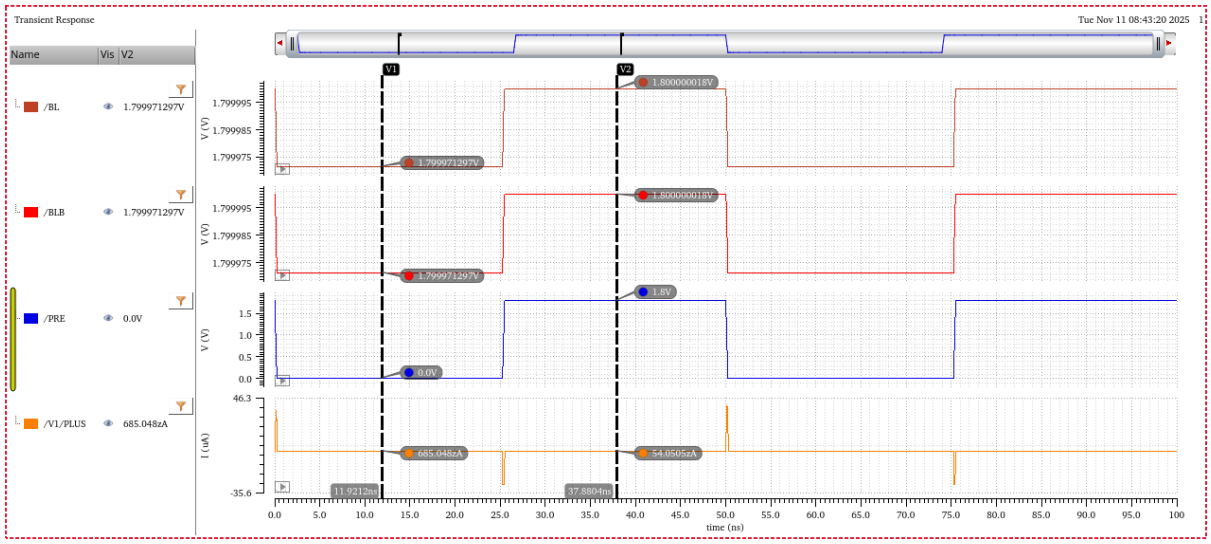
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (19.7595ps + 30.5229ps)/2 = 25.1412ps

STATIC POWER ANALYSIS:



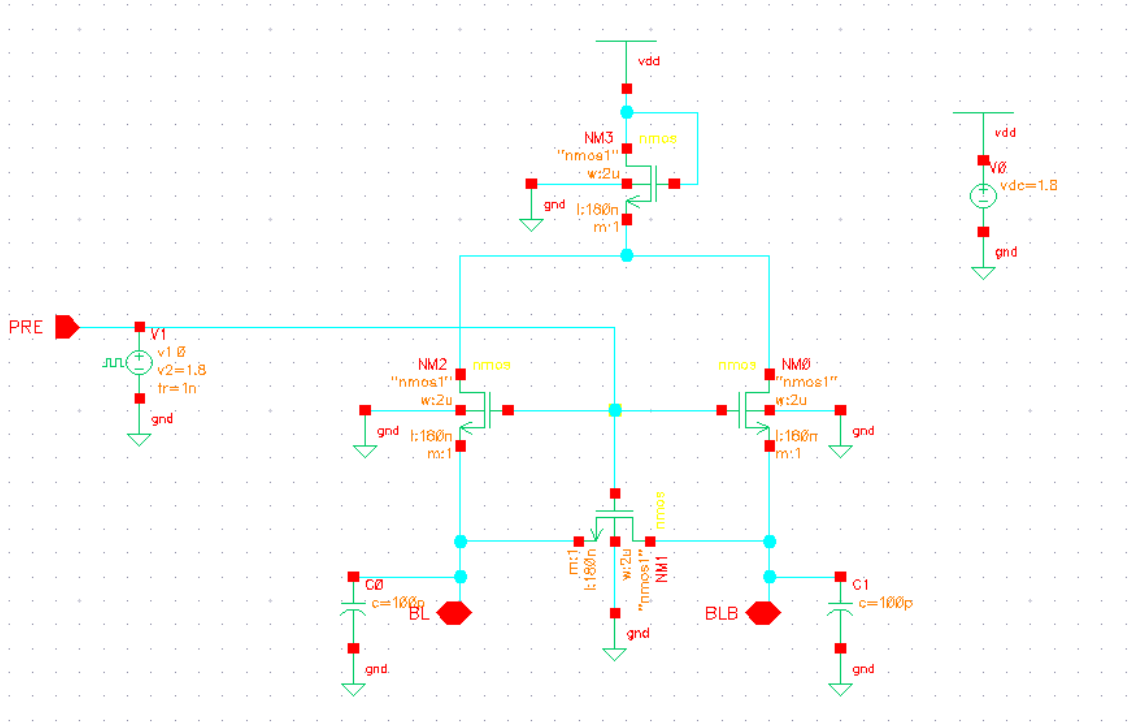
Average static power: $225.376 * 10^{-27} W$

DYNAMIC POWER ANALYSIS:

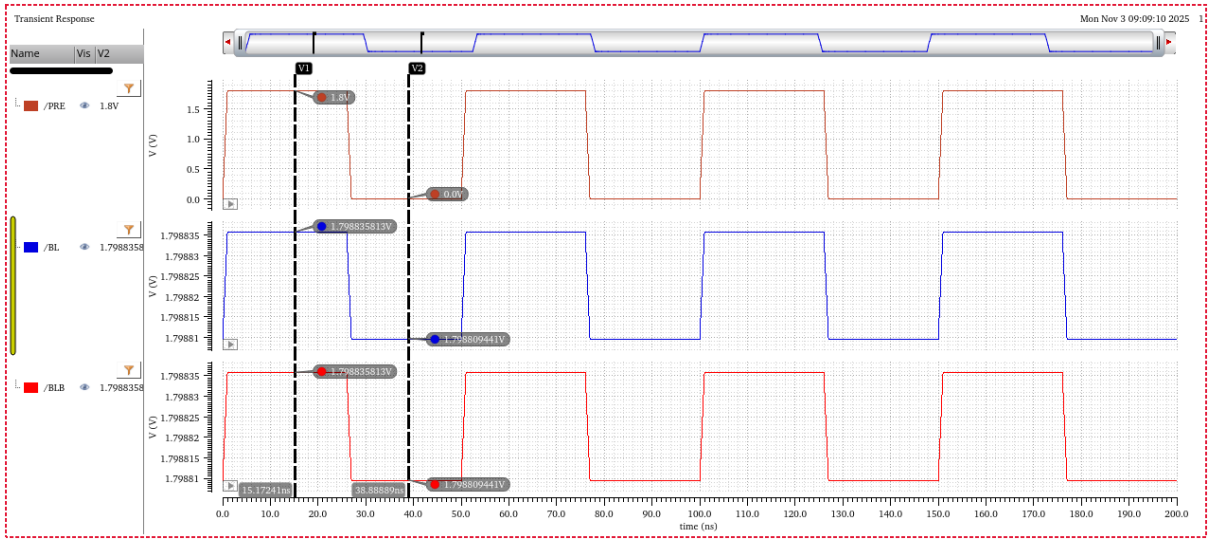


Average dynamic power: 2.3 nW

5. Circuit (c) – NMOS only

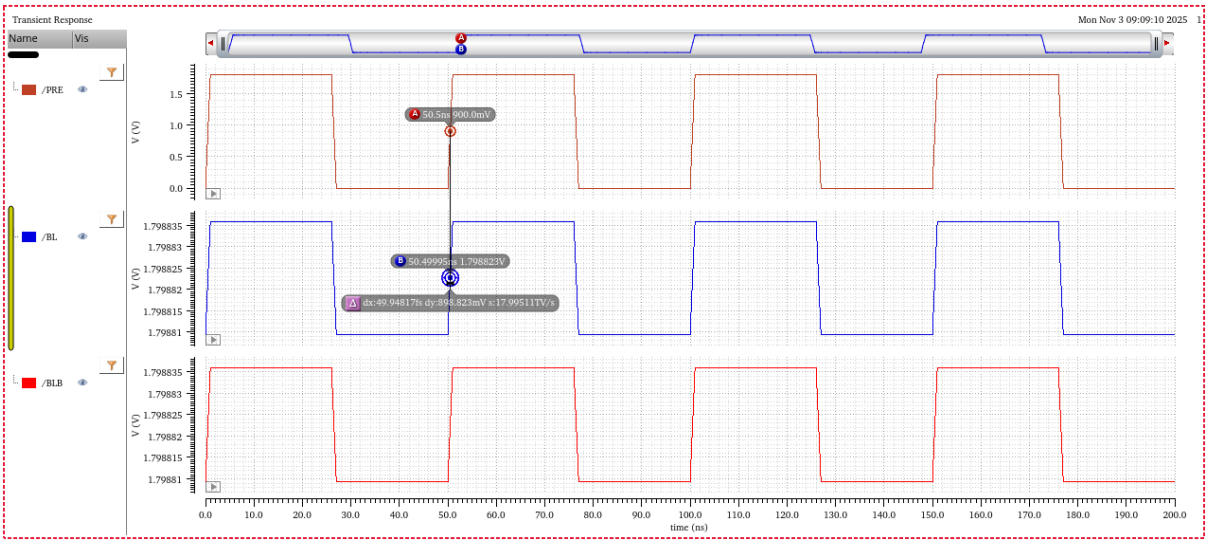


TRANSIENT ANALYSIS:

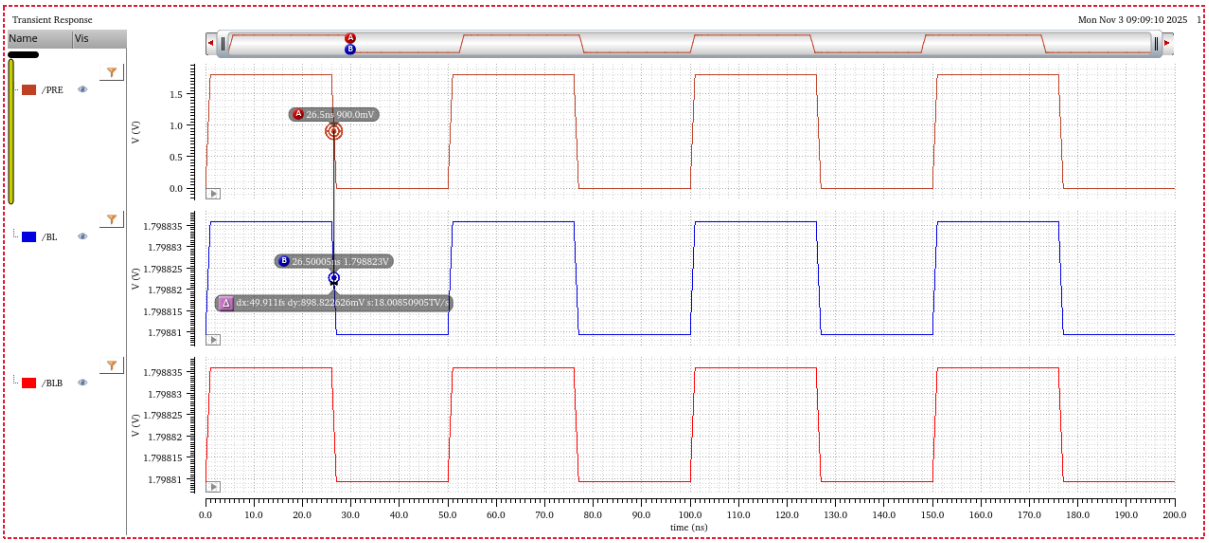


TIME DELAY CALCULATION:

A) T_PLH

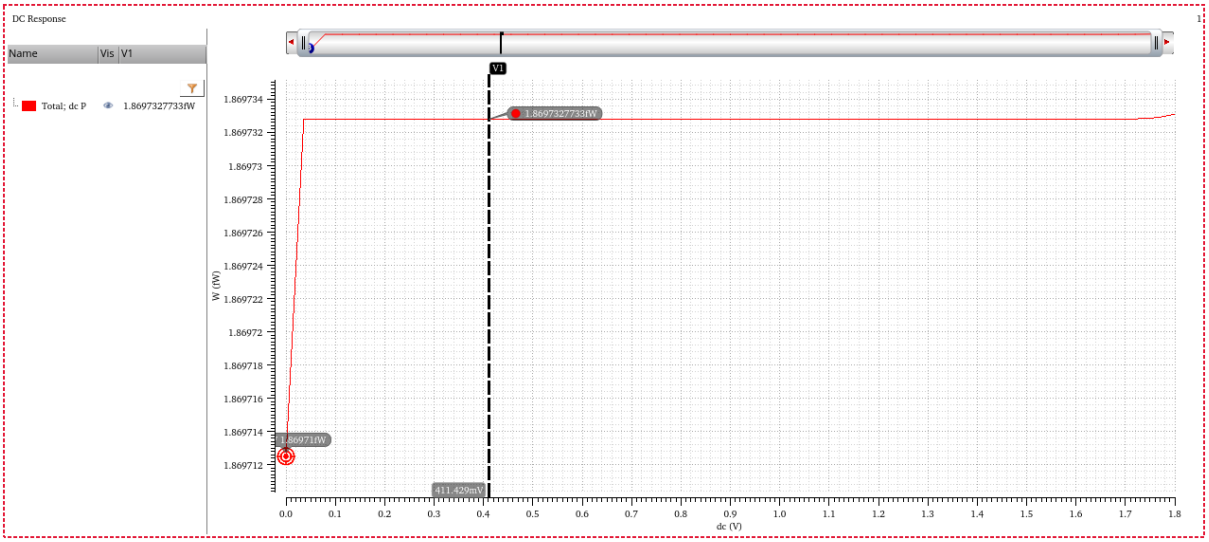


B)T_PHL



TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (49.94817fs + 49.911fs)/2 = 49.929585fs

STATIC POWER ANALYSIS:

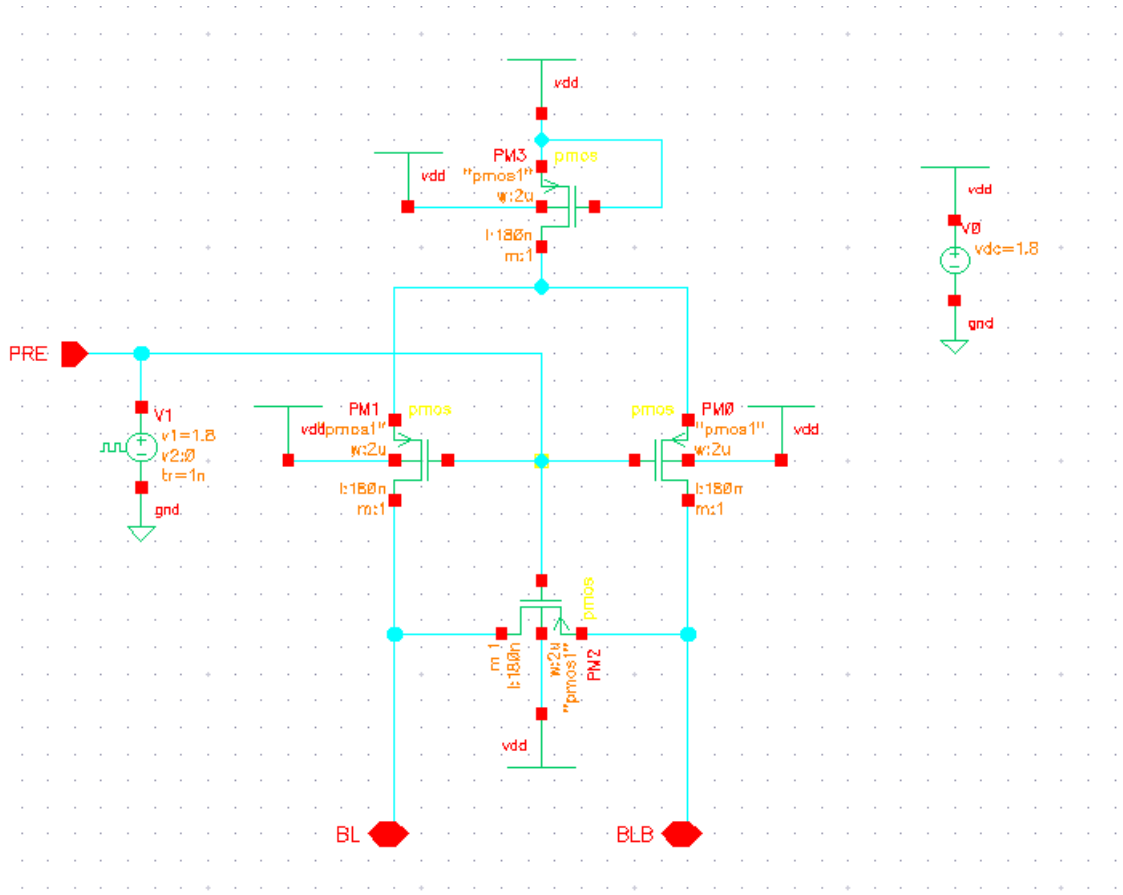


Average static power: 1.86972 fW

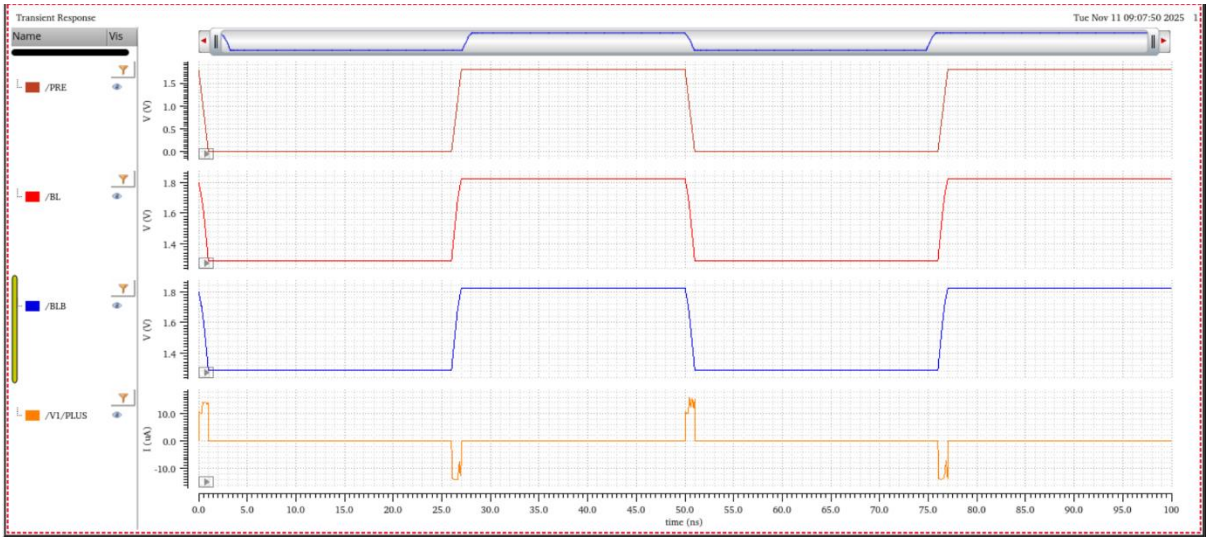
DYNAMIC POWER ANALYSIS:

Average dynamic power: 4.165 nW

6. Circuit (c) – PMOS only

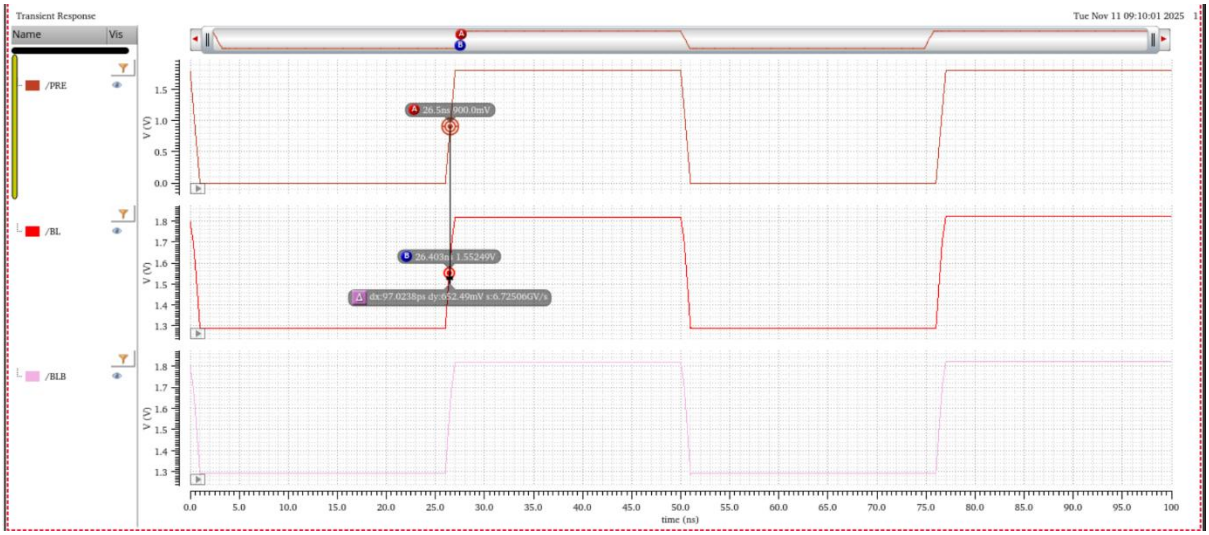


TRANSIENT ANALYSIS:

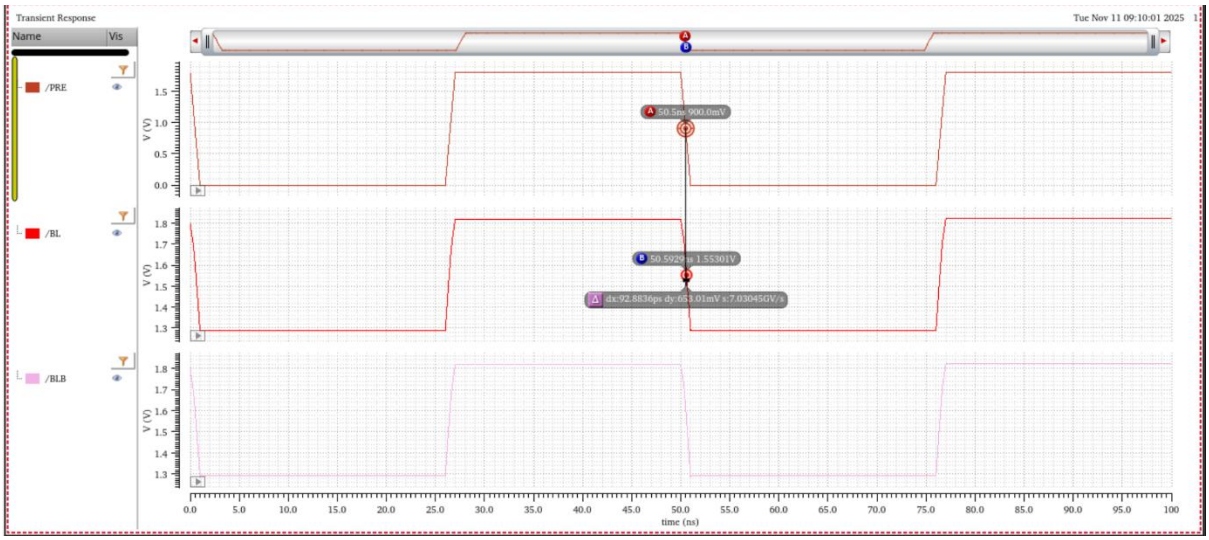


TIME DELAY CALCULATION:

A) T_PLH

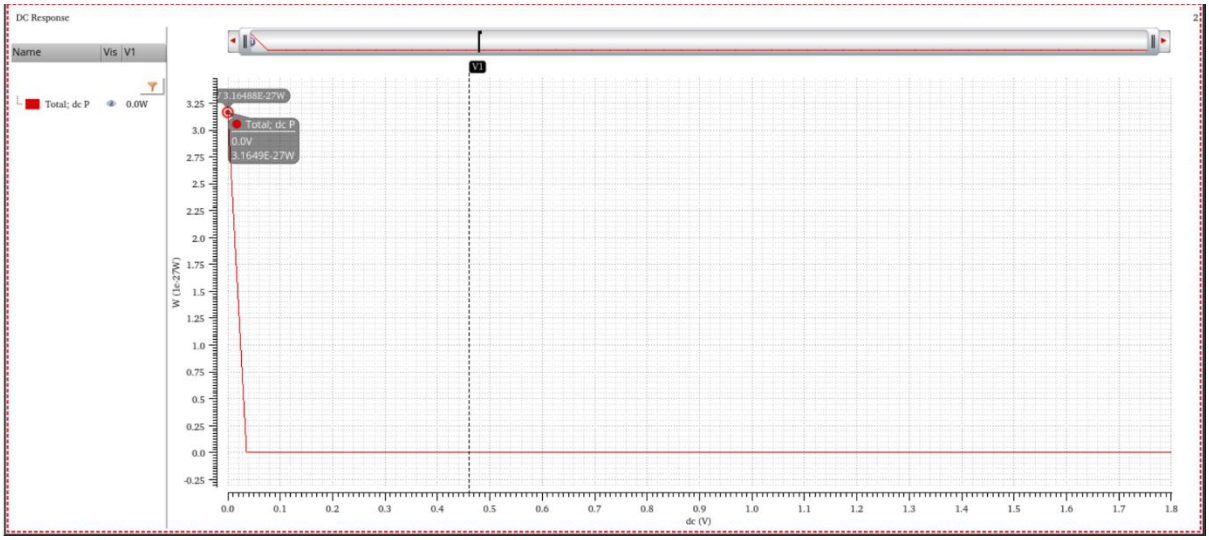


B)T_PHL



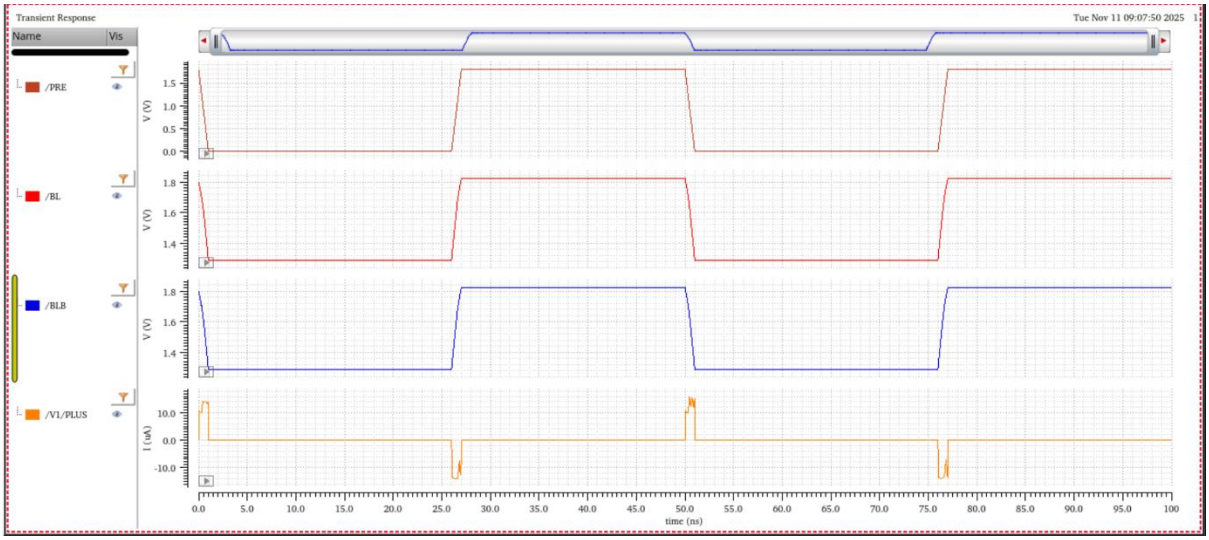
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (97.0238ps + 92.8836ps)/2 = 94.9537ps

STATIC POWER ANALYSIS:



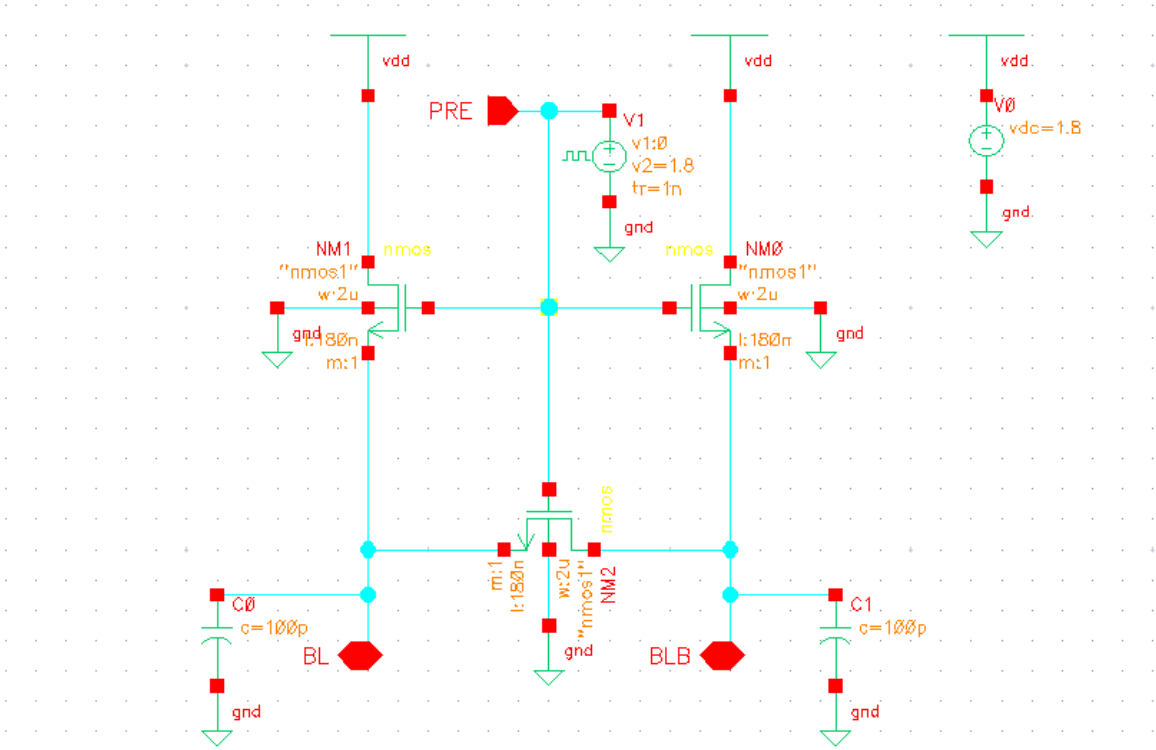
Average static power: $1.58245 * 10^{-27}\ W$

DYNAMIC POWER ANALYSIS:

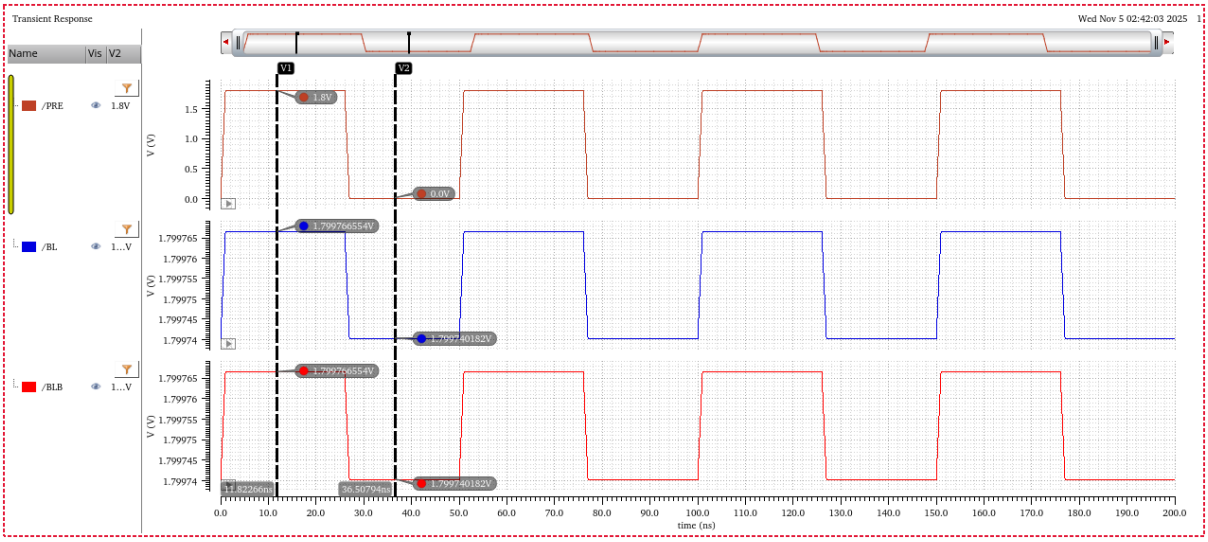


Average dynamic power: 5.214 nW

7. Circuit (d) – NMOS only

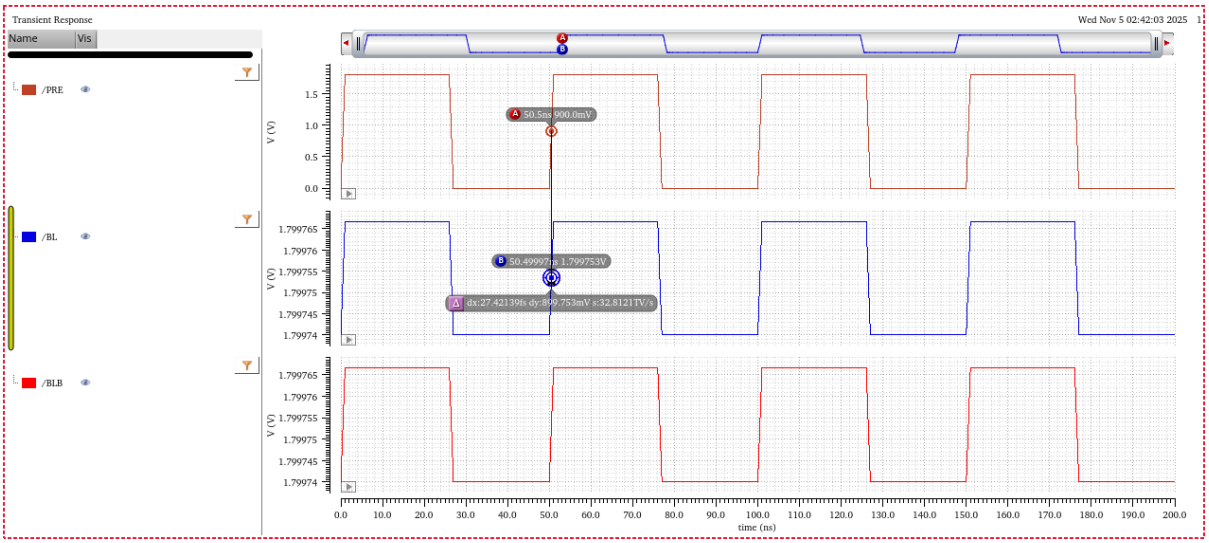


TRANSIENT ANALYSIS:

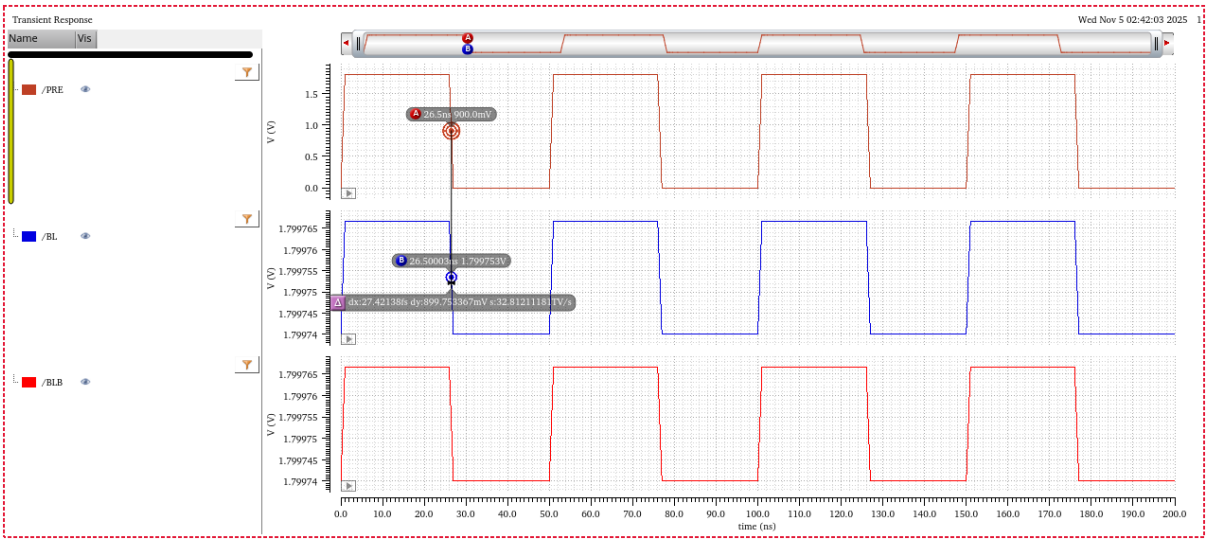


TIME DELAY CALCULATION:

A) T_PLH

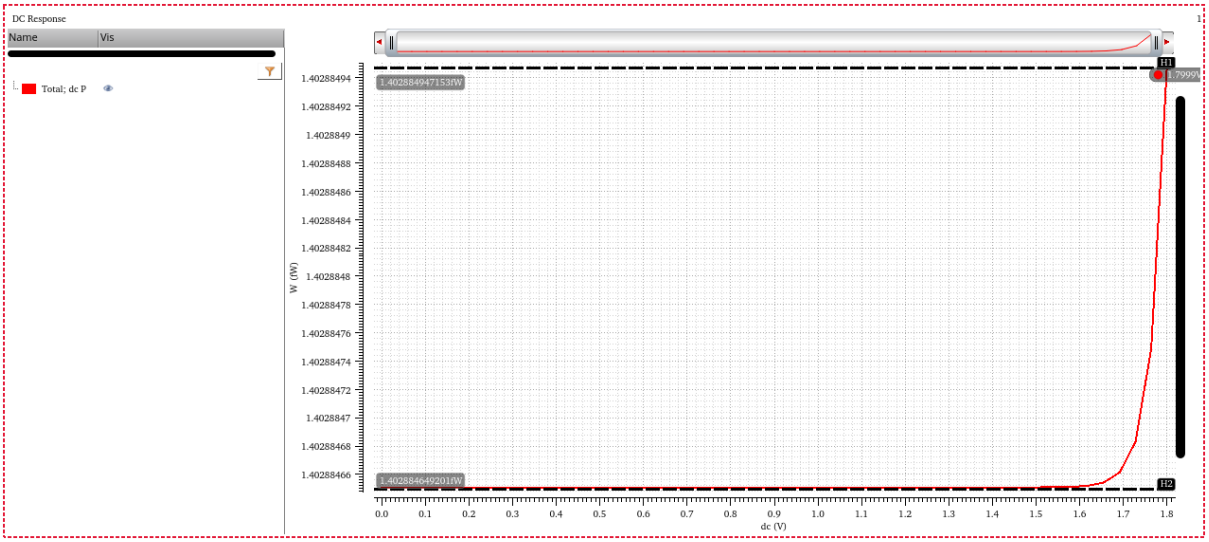


B)T_PHL



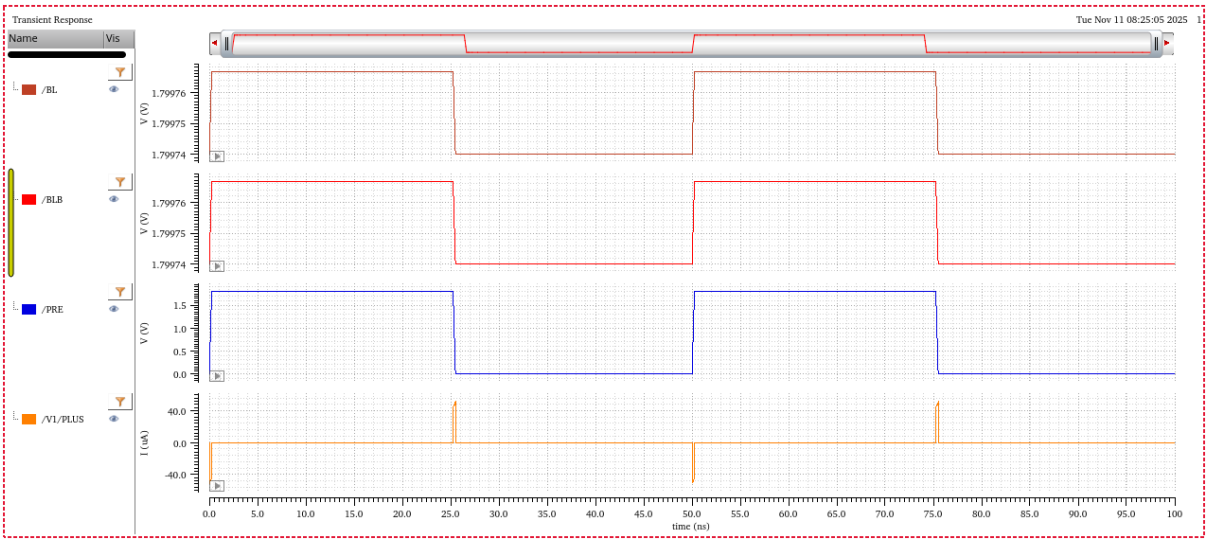
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (27.42139fs + 27.42138fs)/2 = 27.421385fs

STATIC POWER ANALYSIS:



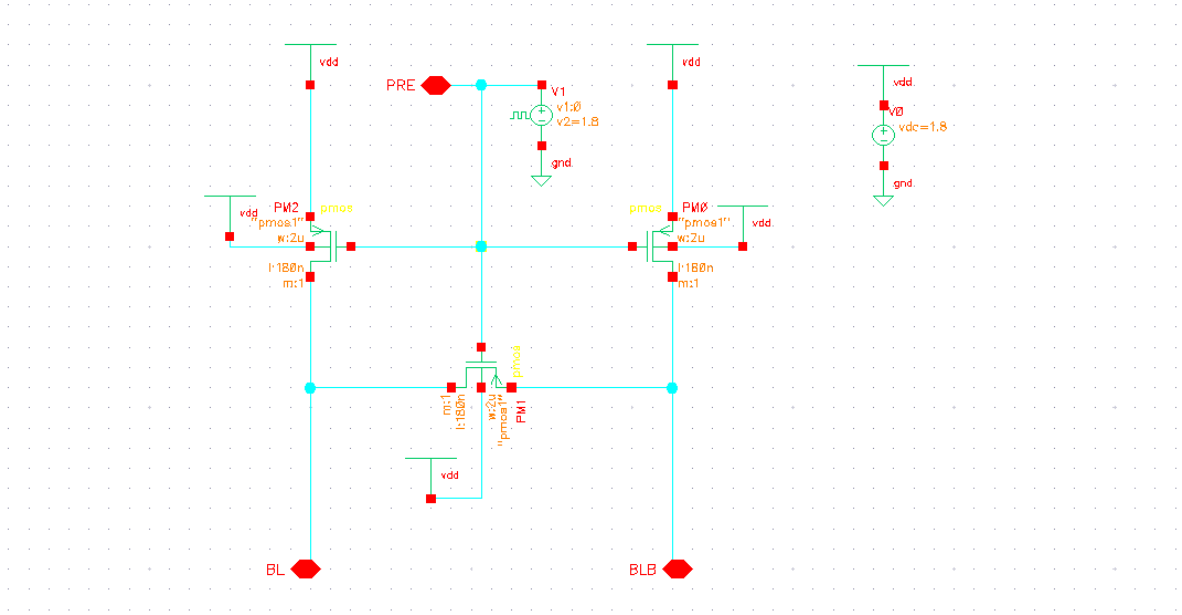
Average static power: 1.40288245 fW

DYNAMIC POWER ANALYSIS:

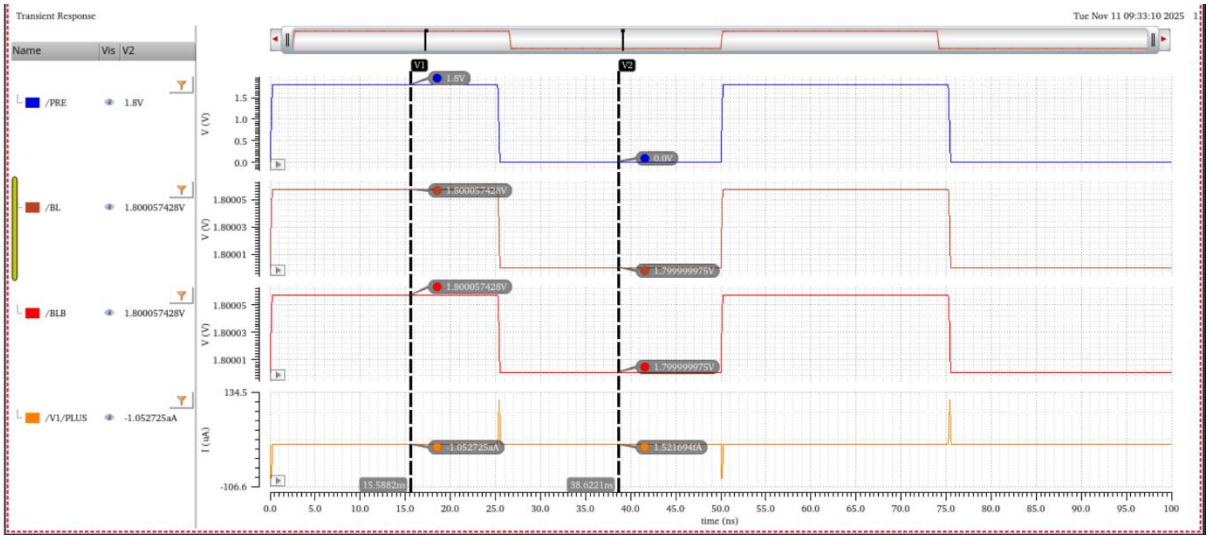


Average dynamic power: 3.893 nW

8. Circuit (d) – PMOS only

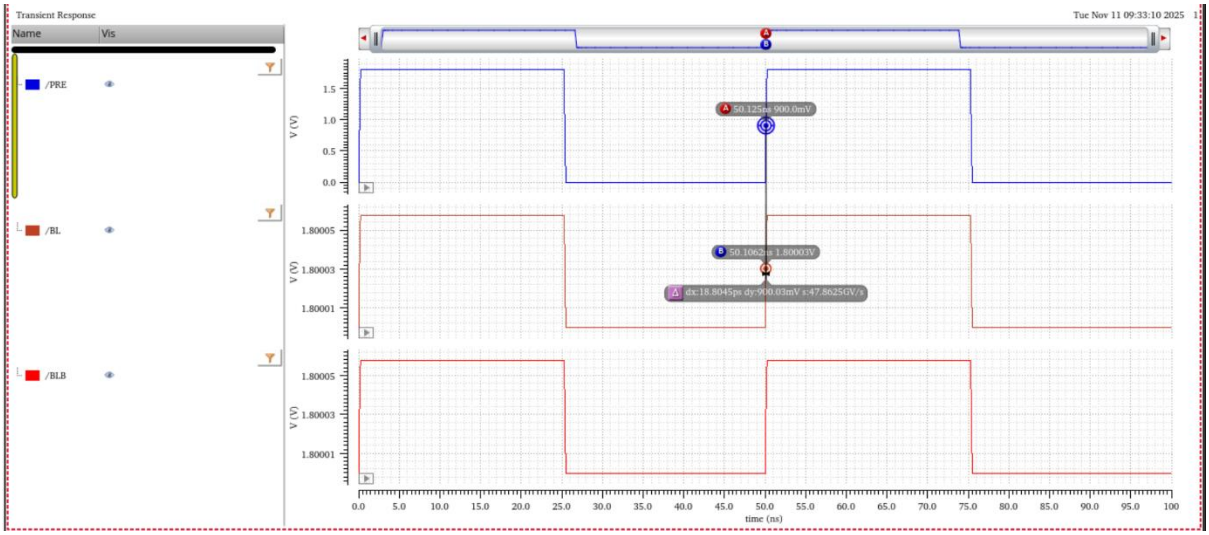


TRANSIENT ANALYSIS:

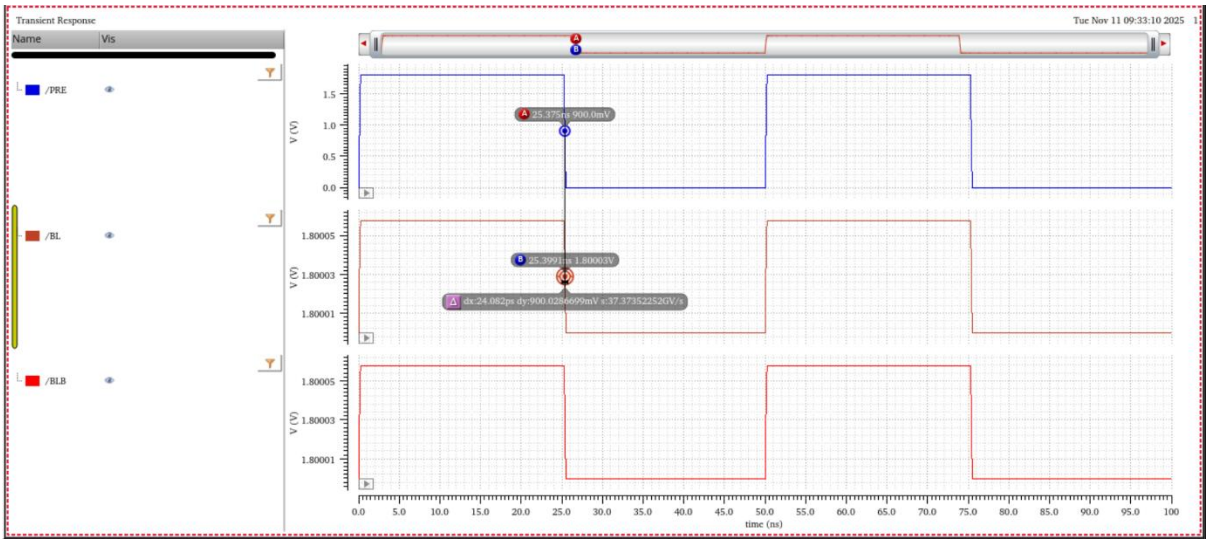


TIME DELAY CALCULATION:

A) T_PLH

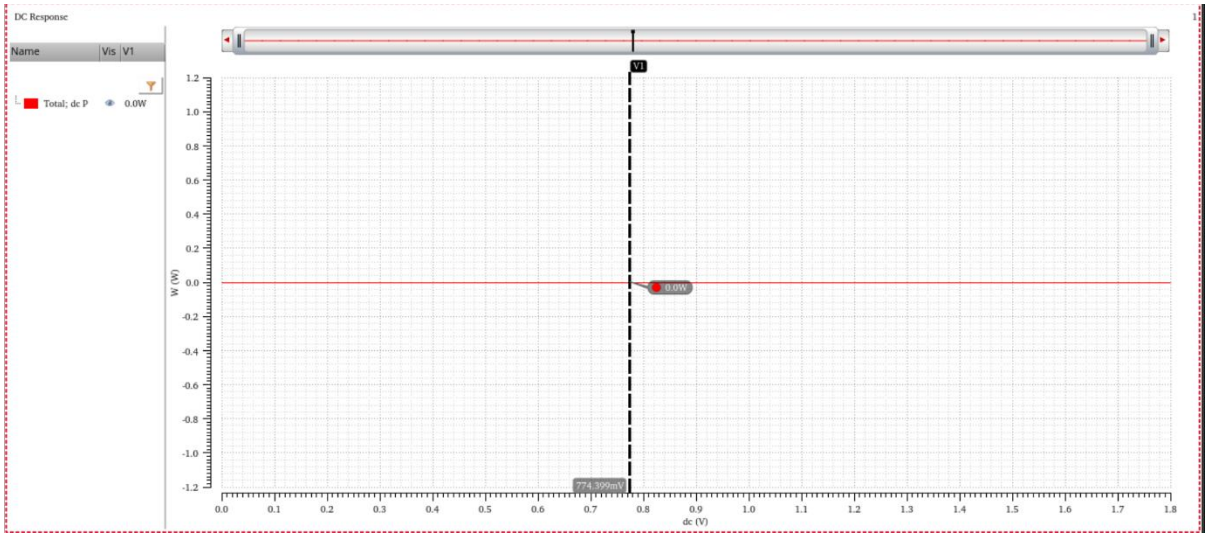


B)T_PHL



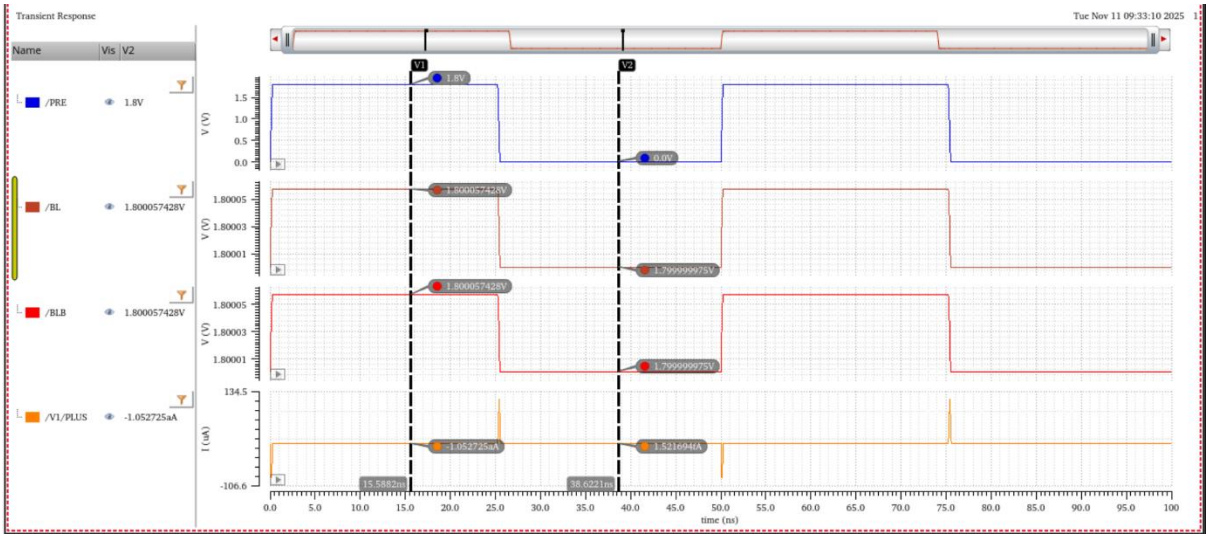
TOTAL TIME DELAY = (T_PLH+T_PHL)/2 = (18.8045ps + 24.082ps)/2 = 21.44325ps

STATIC POWER ANALYSIS:



Average static power: 0 W

DYNAMIC POWER ANALYSIS:



Average dynamic power: 6.9 nW

Comparison of all Circuits:

The table below summarizes the extracted simulation results for all NMOS-only and PMOS-only versions of circuits (a)–(d).

S. No.	Circuit	Device Type	Propagation Delay	Avg. Static Power	Avg. Dynamic Power
1	(a)	NMOS only	5.001209ns	0.9598 mW	322.7 µW
2	(a)	PMOS only	1386.58 ps	0.464335 mW	136.3 µW
3	(b)	NMOS only	153.949 fs	1.40287747385 fW	1.298 nW
4	(b)	PMOS only	25.1412 ps	2.25376×10^{-25} W	2.3 nW
5	(c)	NMOS only	49.929585 fs	1.86972 fW	4.165 nW
6	(c)	PMOS only	94.9537 ps	1.58245×10^{-27} W	5.214 nW
7	(d)	NMOS only	27.421385 fs	1.40288245 fW	3.893 nW
8	(d)	PMOS only	21.44325 ps	0 W	6.9 nW

Discussion and Analysis:

Propagation delays indicate that circuit (d) offers the best performance in both NMOS and PMOS-only implementations. Static power consumption is significantly higher for circuit (a) in both categories, while circuits (b), (c), and (d) demonstrate extremely low static power. Dynamic power consumption is also lowest for circuits (b) and (c), making them strong choices for low-power SRAM designs.

Overall, Circuit (d) – PMOS only – provides the optimal performance with:
• Lowest delay among PMOS circuits
• Zero static power consumption
• Very low dynamic power

CONCLUSION:

For SRAM bitline precharge operation, the recommended design is:
→ Circuit (d) – PMOS only

This choice achieves high speed, low leakage, and minimized switching power, which are essential for high-performance low-power SRAM architectures.