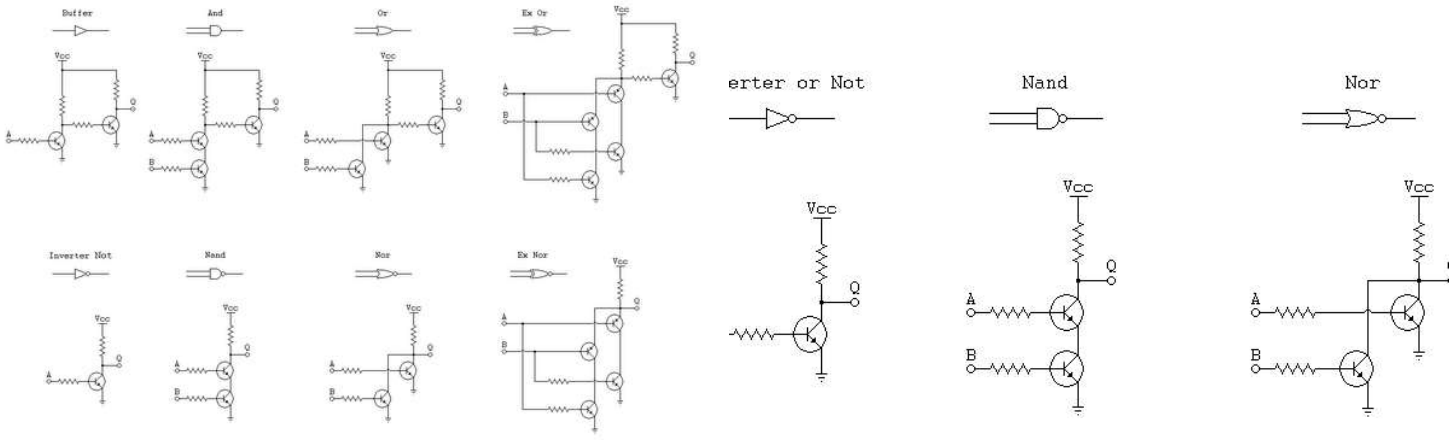
AUTODESK Instructables

# Dual Logic Transistor Gates

By Josehf Murchison in CircuitsElectronics



## Introduction: Dual Logic Transistor Gates




I build transistor gates a little different than most other electronics engineers. Most people when they build transistor gates; build them with only positive logic in mind, however gates in ICs have two logic's, positive logic and negative logic. And I build my transistor gates with positive and negative logic.

Although there are eight gates; Buffer, Inverter or Not, And, Nand, Or, Nor, Xor, and Xnor, they are made from three gate circuits. And when you are building dual logic gates, the three circuits used to build a gate are Inverter or Not, Nand, and Nor, the rest of the gates are made from two or more of these three gates.

Why build transistor gates? Well here are five reasons to build your own gates.

1. You haven’t got the gate you need.

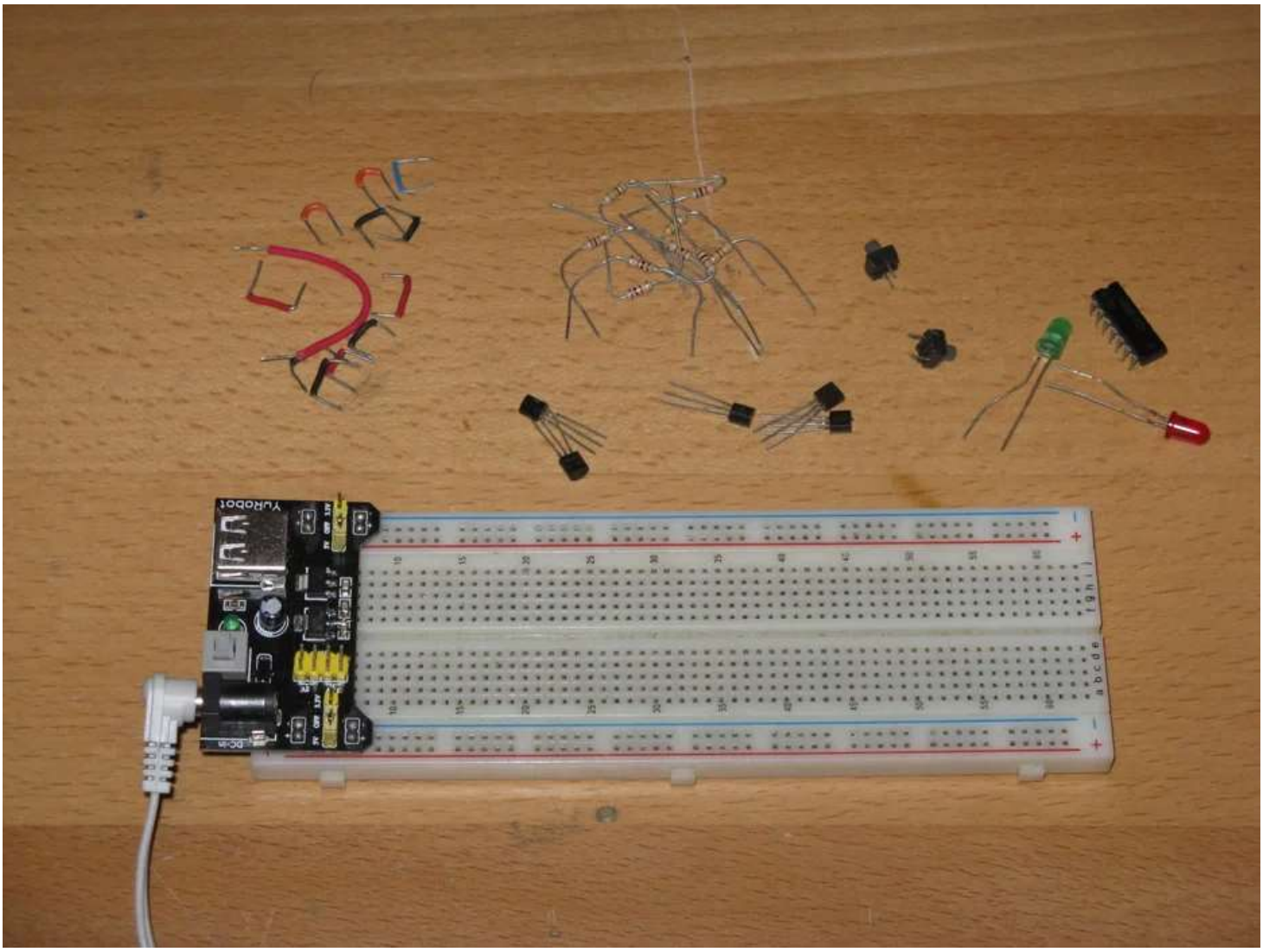
2. You want a gate that carries more power than a standard gate IC.

3. You only want one gate and you hate wasting the rest of the gates on the IC.

4. Cost, a one transistor Inverter is less than $0.25 and a hex Inverter IC is $1.00 and up.

5. You want to understand gates better.

# Step 1: Tools & Parts



The gates in this Instructable are ¼ watt gates if you want to build gates with a higher wattage you will need heaver wattage components.

Jumper Wires

Breadboard

Power Supply

1 x SN74LS04 IC

2 x Switches

2 x LEDs 1 red 1 green

2 x 820 Ω ¼ w resistors

2 x 1 kΩ ¼ w resistors

3 x 10 kΩ ¼ w resistors

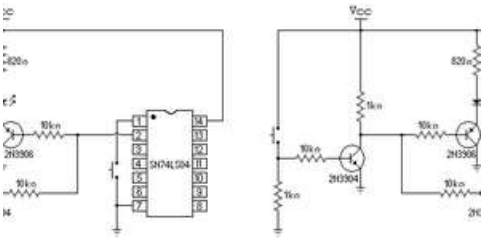
3 x NPN general purpose transistors, I used 2N3904.

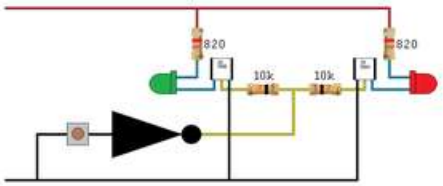
2 x PNP general purpose transistors, I used 2N3906.

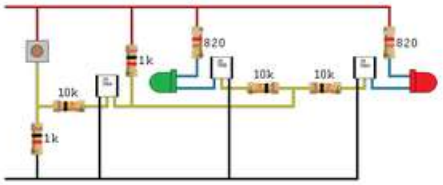
# Step 2: Dual Logic

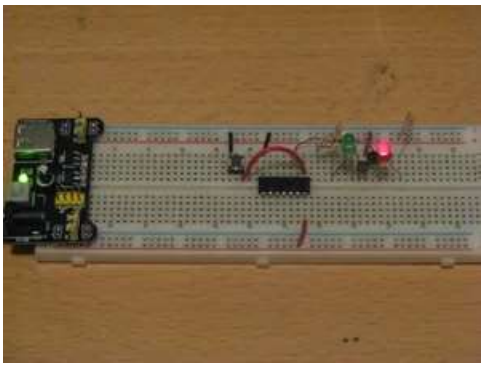
## Or Truth Table

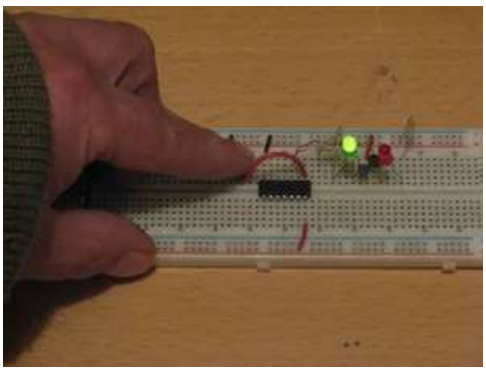
| A | B | Q |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

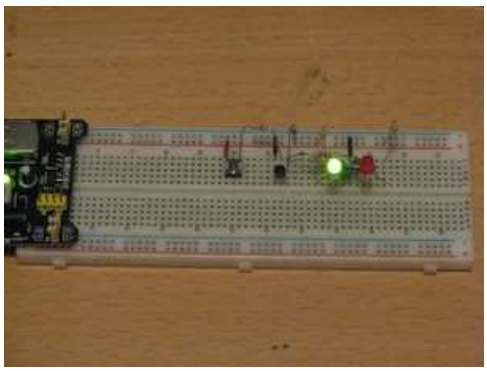


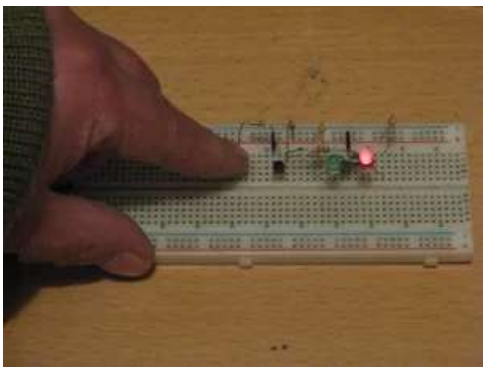








When you look up the truth table of a gate; such as a two input Or gate, you will get a truth table that looks like this. This is a positive truth table for an Or gate. Under A and B is the inputs to the gate and Q is the output. 1 represents logic value of 1 or + 5 volts and 0 represents a logic value of 0 or 0 volts. So when most people build a gate out of transistors they build it logic value of 1 or + 5 volts and logic value of 0 or no volts. But that isn't what happens to the output of a gate, in an IC.

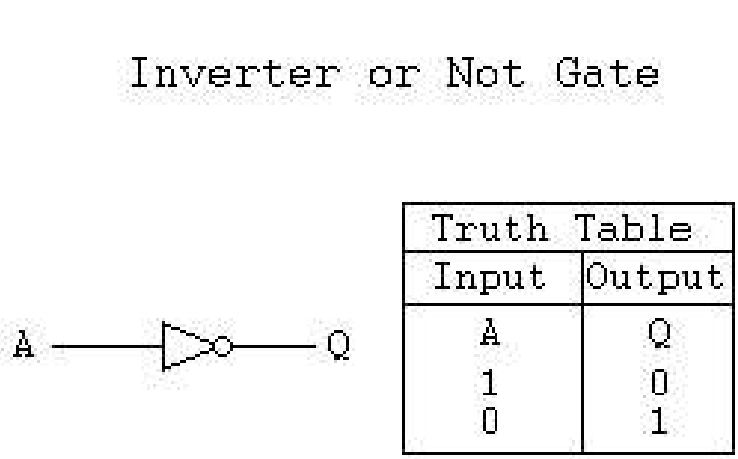
When the output of a gate goes from logic value 1 to logic value 0 the output of that gate goes from + 5 volts with the current flowing out of the output to 0 volts with the current flowing into the output of the

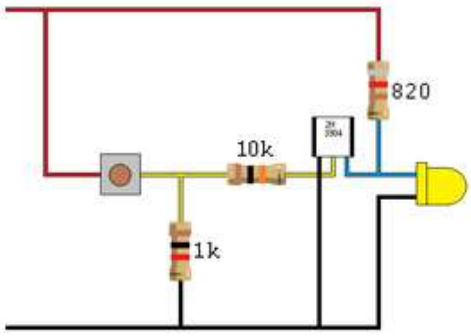
gate. The current reverses direction. When you use the reversed current flow this is called negative logic where 0 volts is – 1 logic value and + 5 volts is – 0 logic value.

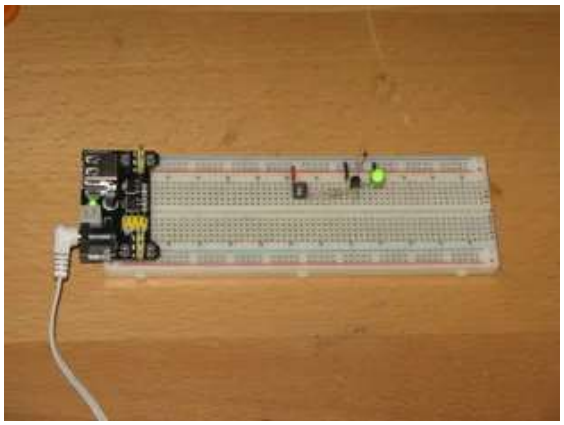
It is easiest to see what this does is when you connect the output of any gate; to the base of a NPN transistor and a PNP transistor, in series with an LED. While the output of the gate is logic value 1, (5 Volts), the NPN transistor is closed and the LED in series with the NPN transistor lights up. When the gate output goes from logic value 1 to logic value 0, (5 volts to 0 volts), the current reverses direction and the NPN transistor opens as the PNP transistor closes. This turns off the LED in series with the NPN transistor and lights up the LED in series with the PNP transistor.

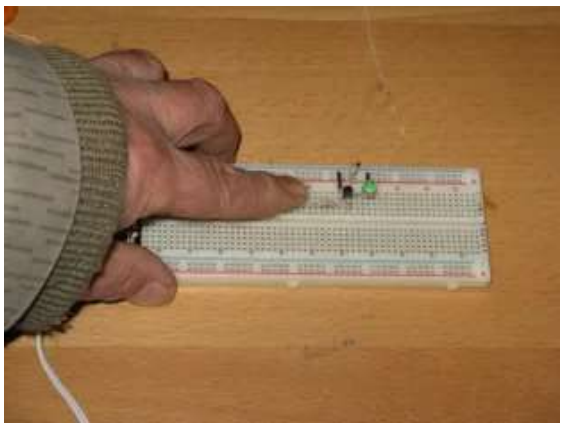
My transistor gates have the same dual logic as the gates in ICs. While the output of the gate is logic value 1, (5 Volts), the NPN transistor is closed and the LED in series with the NPN transistor lights up. When the gate output goes from logic value 1 to logic value 0, (5 volts to 0 volts), the current reverses direction and the NPN transistor opens as the PNP transistor closes. This turns off the LED in series with the NPN transistor and lights up the LED in series with the PNP transistor.

# Step 3: Not or Inverter Gate





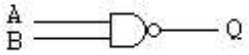
Not or Inverter gate is the first of the 3 gates needed to make the other 5 gates.

When the input, (A) of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out of the output (Q).

When the input, (A) of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

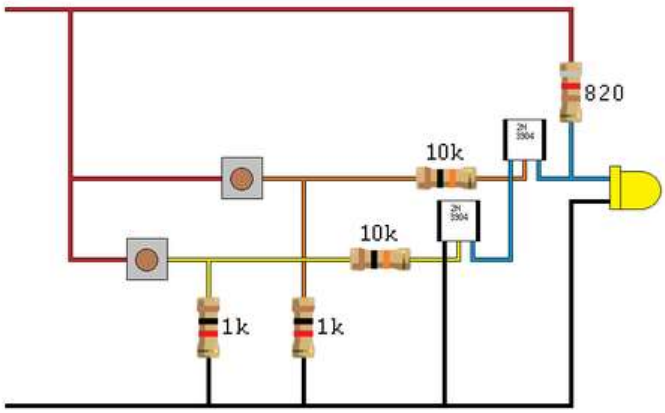
# Step 4: Nand Gate

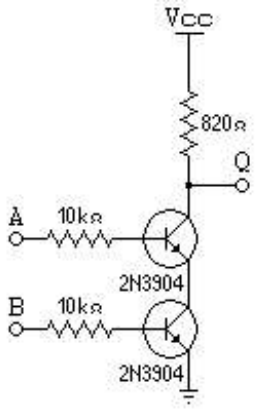
2 Input Nand Gate

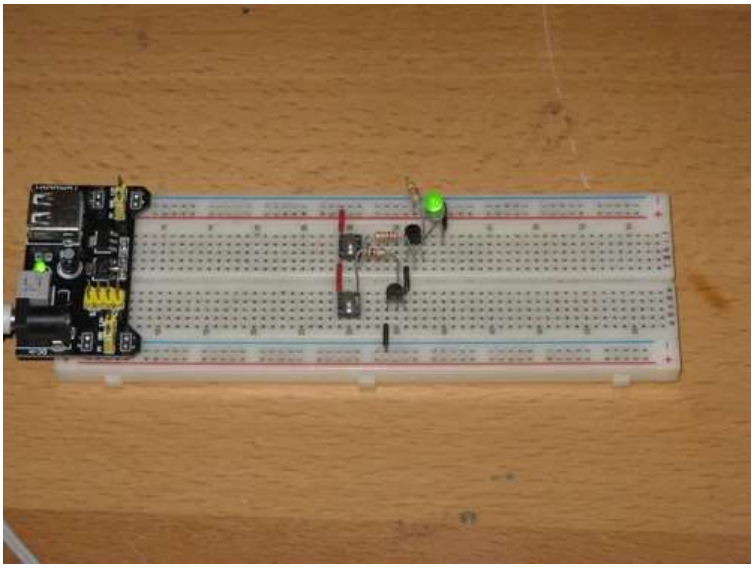


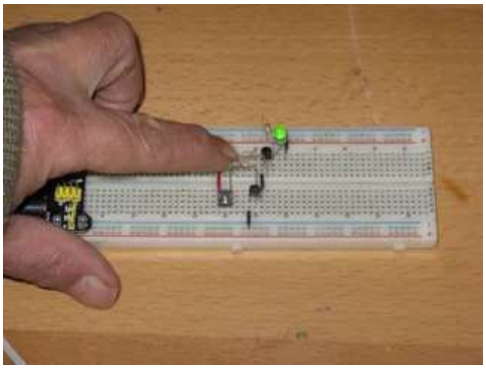

| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

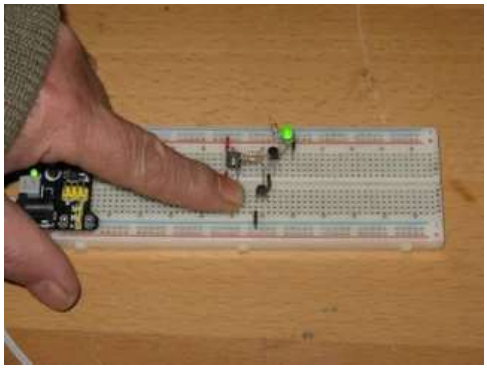
2 Input Transistor Nand Gate

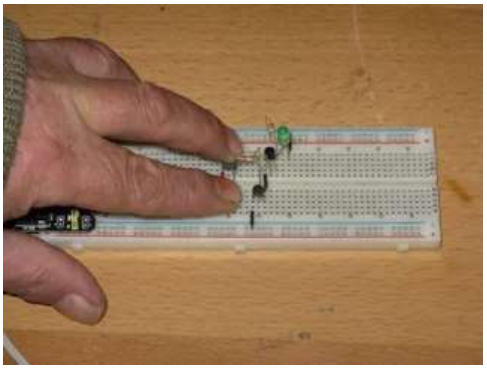








The Nand gate is the second of the three gates needed to make the other 5 gates.

When the inputs, (A and B) of the Nand gate is 0 or 0 volts both of the NPN transistors are open and the output, (Q) is 1 or +5 volts and any positive current goes out of the output (Q).

When the input, (A) of the Nand gate is 1 or +5 volts the NPN transistor on A input is closed. And when the input, (B) of the Nand gate is 0 or 0 volts the NPN transistor on B input is open and the output, (Q) is 1 or +5 volts and any positive current goes out of the output (Q).

When the input, (A) of the Nand gate is 0 or 0 volts the NPN transistor on A input is open. And when the input, (B) of the Nand gate is 1 or +5 volts the NPN transistor on B input is closed and the output,

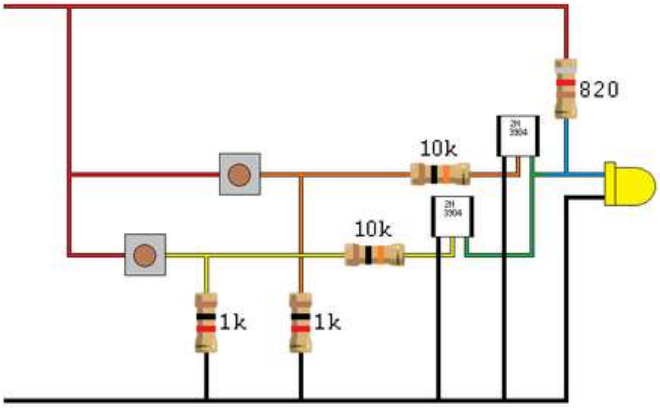
(Q) is 1 or +5 volts and any positive current goes out of the output (Q).

When the inputs, (A and B) of the Nand gate is 1 or +5 volts the both of the NPN transistors are closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistors.

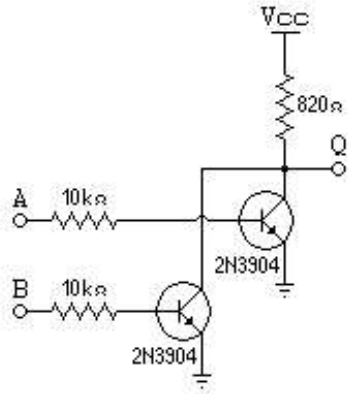
# Step 5: Nor Gate

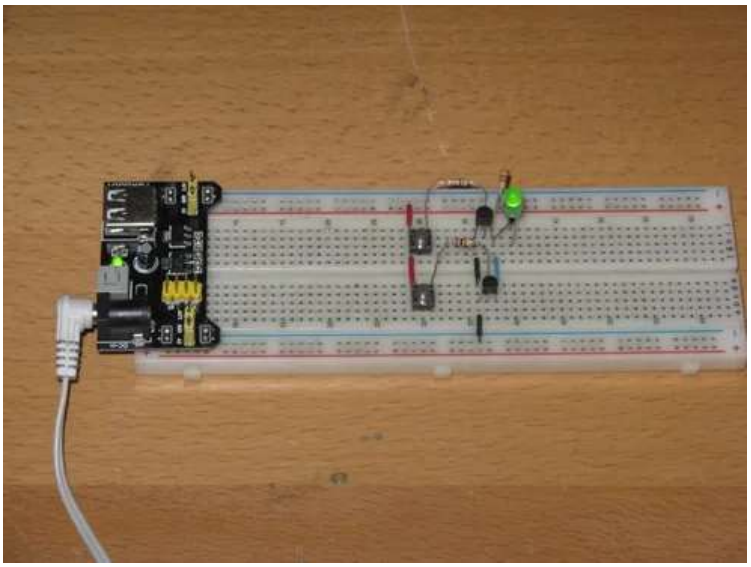
2 Input Nor Gate

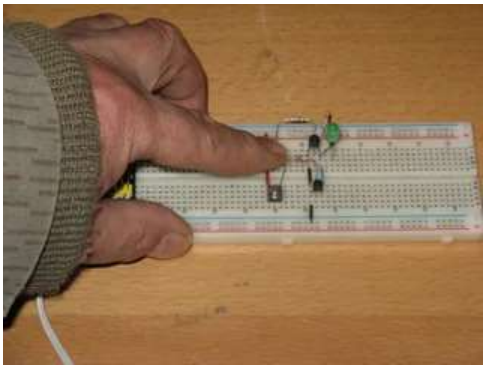

| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

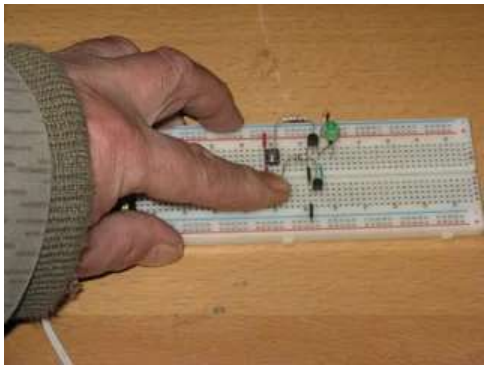


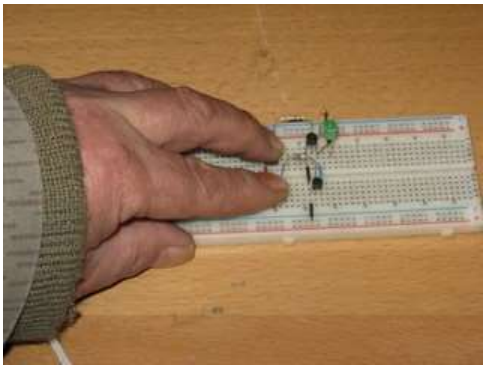

2 Input Transistor Nor Gate









The Nor gate is the third of the three gates needed to make the other 5 gates.

When the inputs, (A and B) of the Nor gate is 0 or 0 volts both of the NPN transistors are open and the output, (Q) is 1 or +5 volts and any positive current goes out of the output (Q).

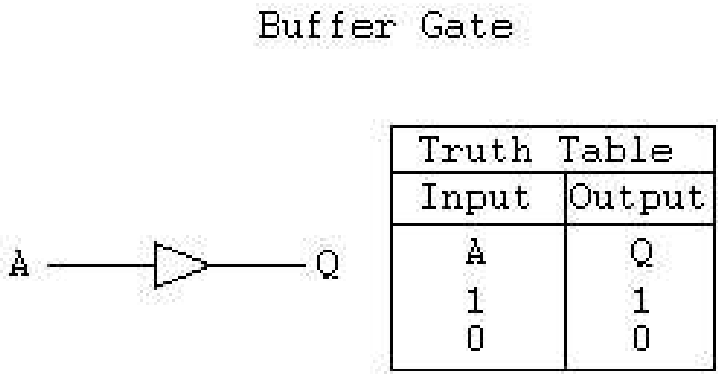
When the input, (A) of the Nor gate is 1 or +5 volts the NPN transistor on A input is closed. And when the input, (B) of the Nor gate is 0 or 0 volts the NPN transistor on B input is open and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor on A input.

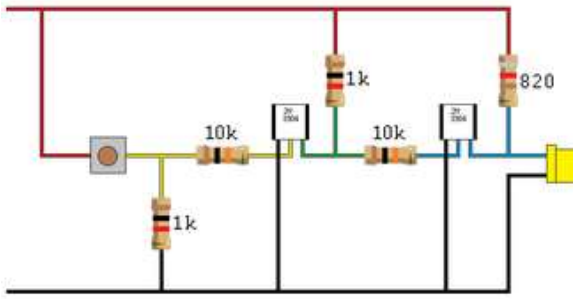
When the input, (A) of the Nor gate is 0 or 0 volts the NPN transistor on A input is open. And when the input, (B) of the Nor gate is 1 or +5 volts the NPN transistor on B input is closed and the output, (Q) is

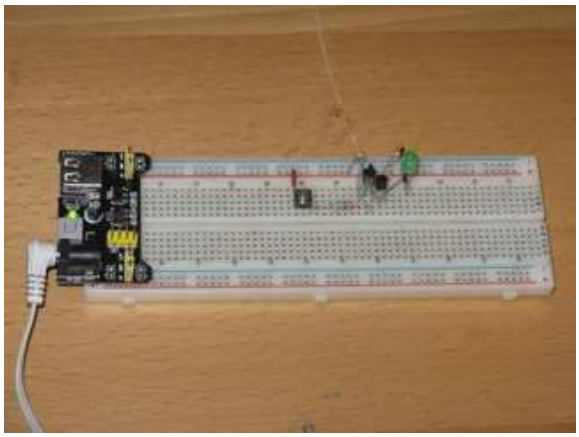
0 or 0 volts and any positive current goes to ground through the transistor on B input.

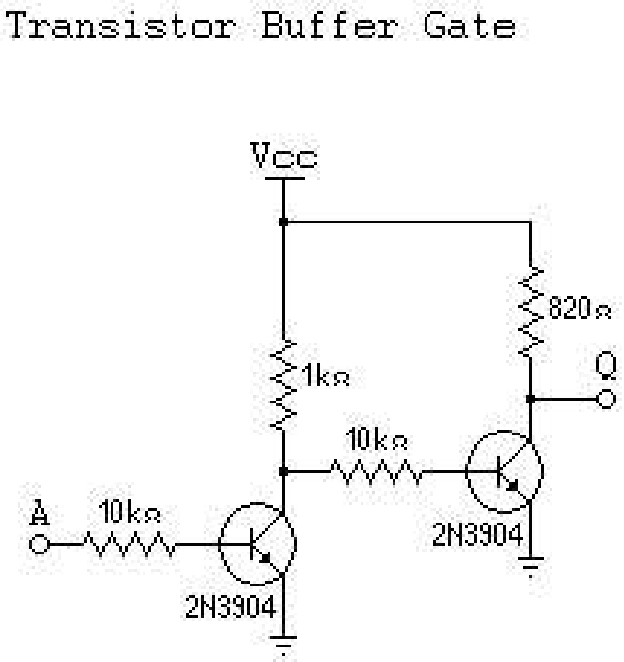
When the inputs, (A and B) of the Nor gate is 1 or +5 volts the both of the NPN transistors are closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through both of the transistors.

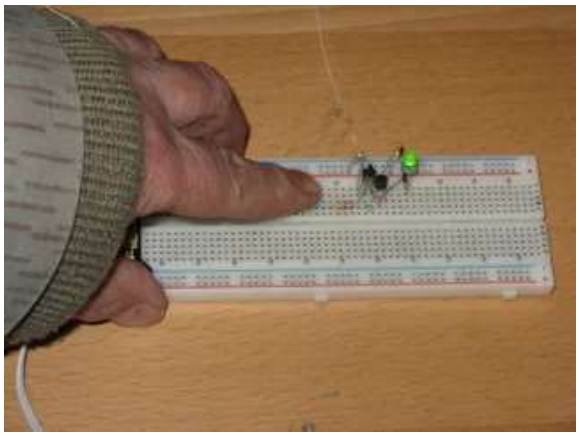
# Step 6: Buffer





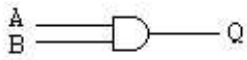
A Buffer uses two of the same gates; two Not or Inverter gates in series.

When the input, (A) of the first Inverter gate is 0 or 0 volts the NPN transistor is open and the output, is 1 or +5 volts to the input of the second inverter. When the input of the second Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

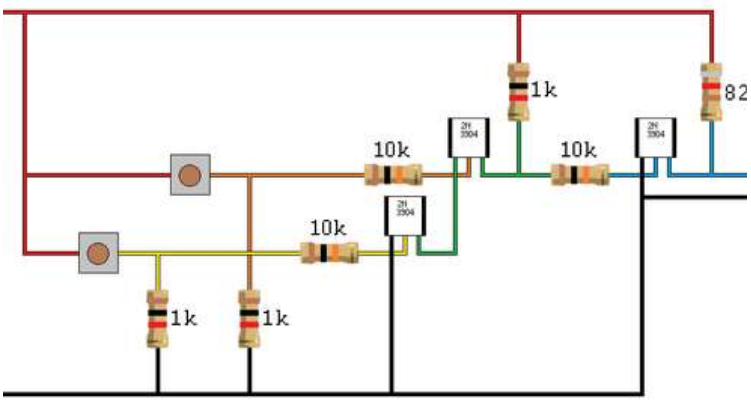
When the input, (A) of the first Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, is 0 or 0 volts to the input of the second inverter. When the input of the second Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

# Step 7: And Gate

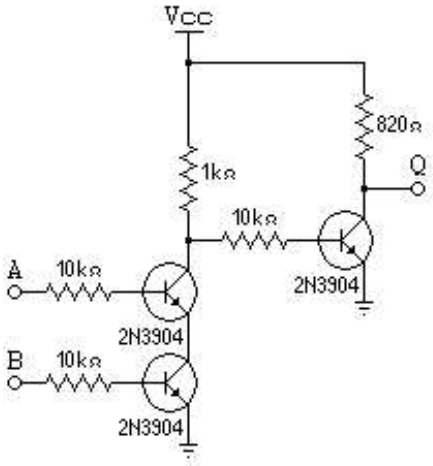
2 Input And Gate

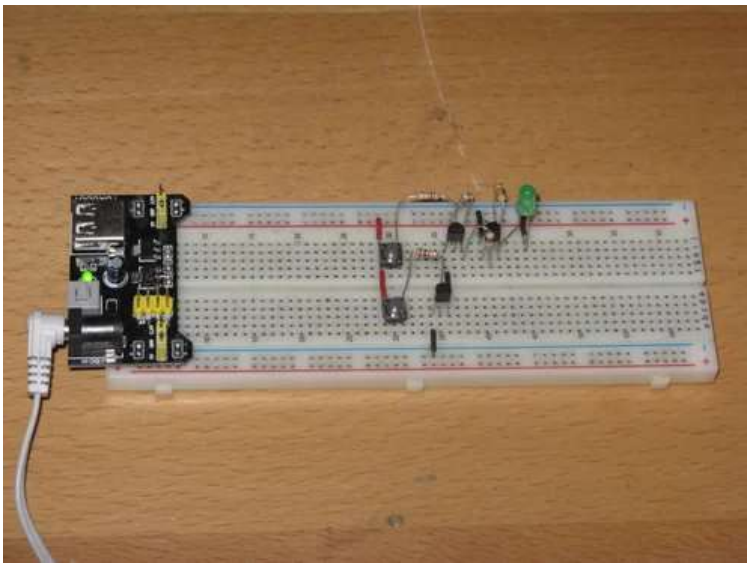


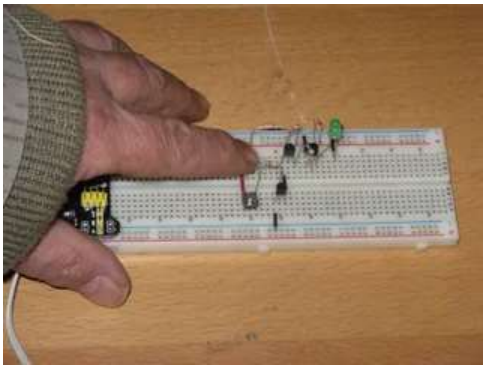

| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 0 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

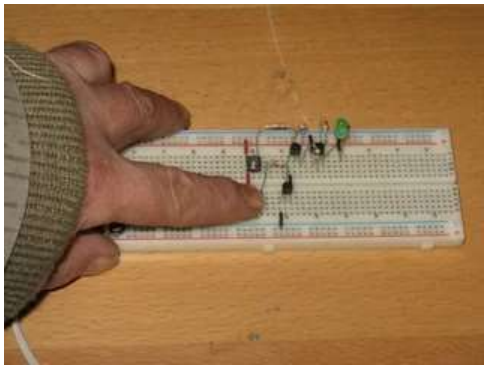


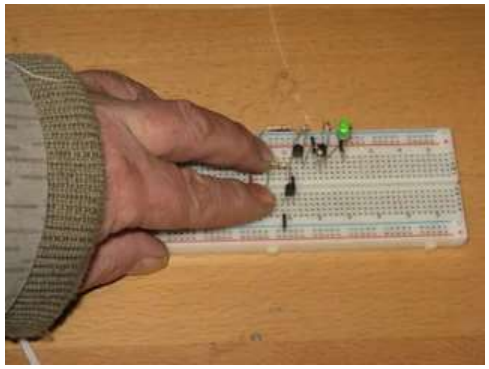

2 Input Transistor And Gate









The And gate is a Nand gate and a Not or Inverter gate in series.

The inputs are the same as the Nand gate however the output is reversed by the Not or Inverter gate.

When the inputs, (A and B) of the And gate is 0 or 0 volts both of the NPN transistors are open, the output of the first gate is 1 or +5 volts. When the input of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

When the input, (A) of the And gate is 1 or +5 volts the NPN transistor on A input is closed. And when the input, (B) of the And gate is 0 or 0 volts the NPN transistor on B input is open, the output of the first

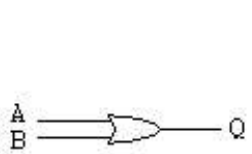
gate is 1 or +5 volts. When the input of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

When the input, (A) of the And gate is 0 or 0 volts the NPN transistor on A input is open. And when the input, (B) of the And gate is 1 or +5 volts the NPN transistor on B input is closed, the output of the first gate is 1 or +5 volts. When the input of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

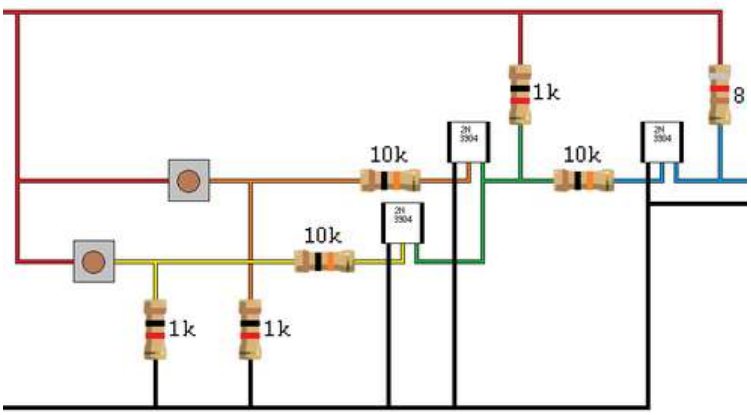
When the inputs, (A and B) of the Nand gate is 1 or +5 volts the both of the NPN transistors are closed and the output of the first gate is 0 or 0 volts. When the input of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

# Step 8: Or Gate

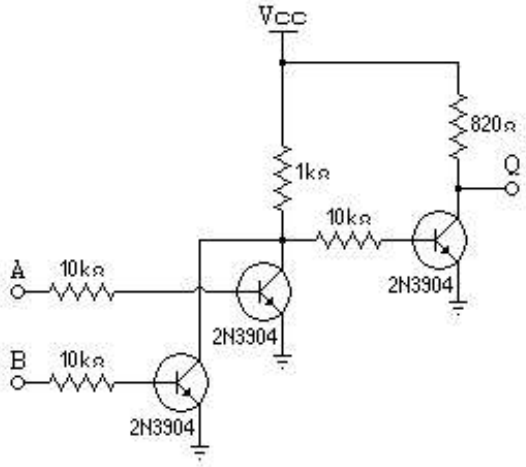
2 Input OR Gate

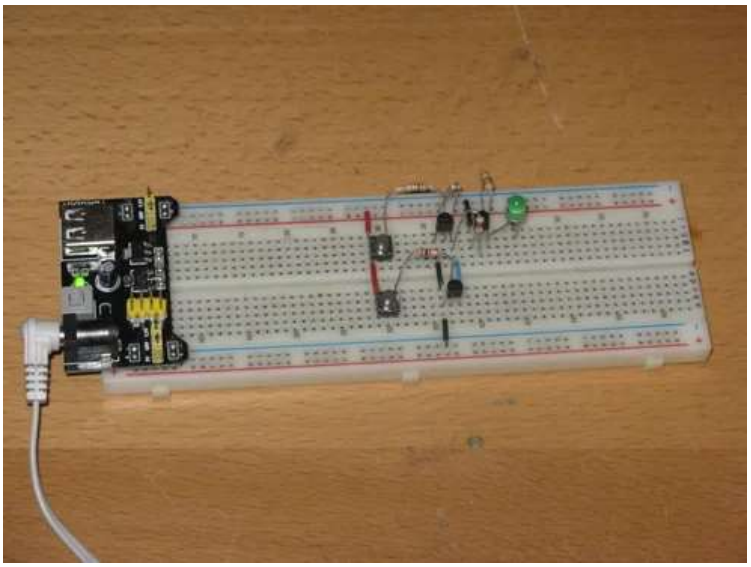


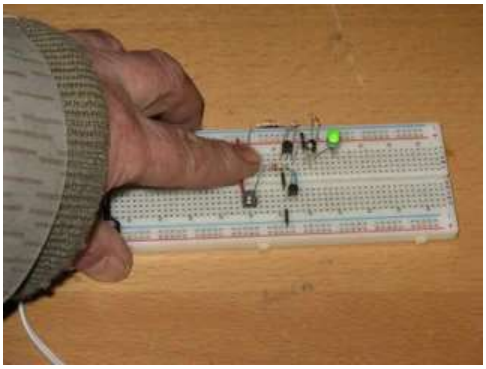

| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |

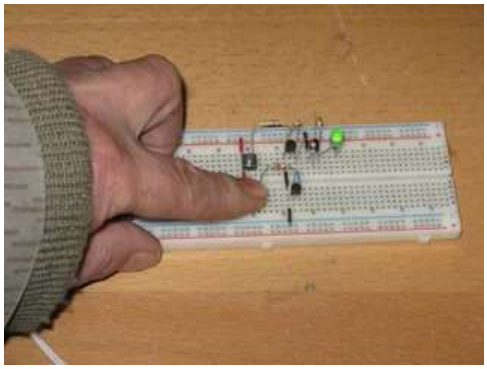


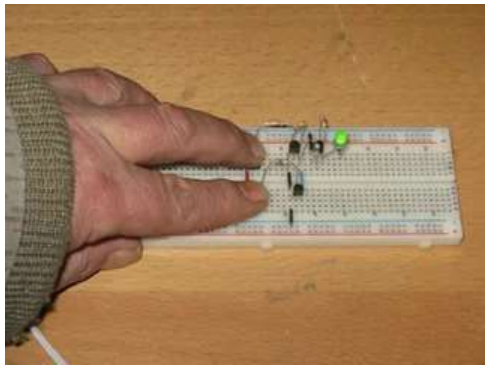

2 Input Transistor OR Gate









The Or gate is a Nor gate and a Not or Inverter gate in series.

The inputs are the same as the Nor gate however the output is reversed by the Not or Inverter gate.

When the inputs, (A and B) of the Or gate is 0 or 0 volts both of the NPN transistors are open, the output of the first gate is 1 or +5 volts. When the input of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

When the input, (A) of the Or gate is 1 or +5 volts the NPN transistor on A input is closed. And when the input, (B) of the Nor gate is 0 or 0 volts the NPN transistor on B input is open and the output of the

first gate is 0 or 0 volts. When the input of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

When the input, (A) of the Or gate is 0 or 0 volts the NPN transistor on A input is open. And when the input, (B) of the Nor gate is 1 or +5 volts the NPN transistor on B input is closed and the output of the first gate is 0 or 0 volts. When the input of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

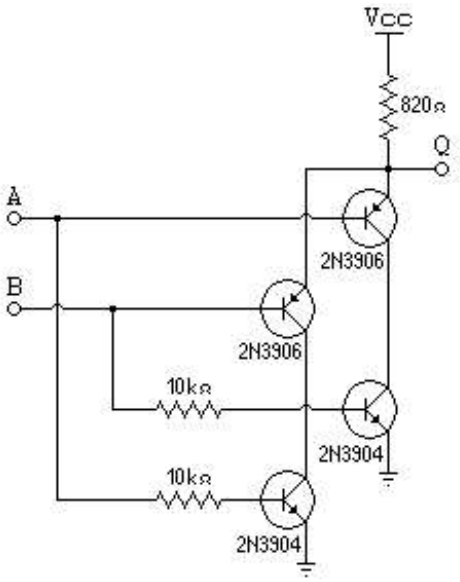
When the inputs, (A and B) of the Or gate is 1 or +5 volts the both of the NPN transistors are closed and the output of the first gate is 0 or 0 volts. When the input of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

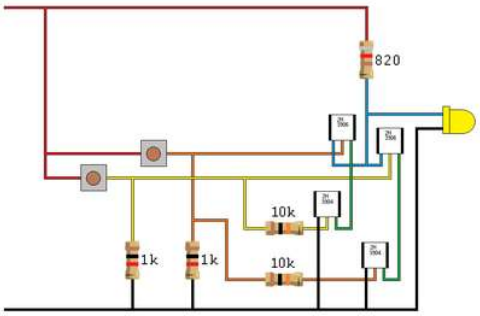
# Step 9: Exclusive Nor Gate (Xnor)

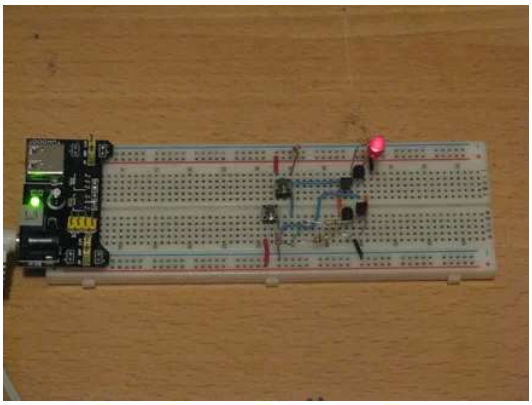
2 Input Xnor Gate

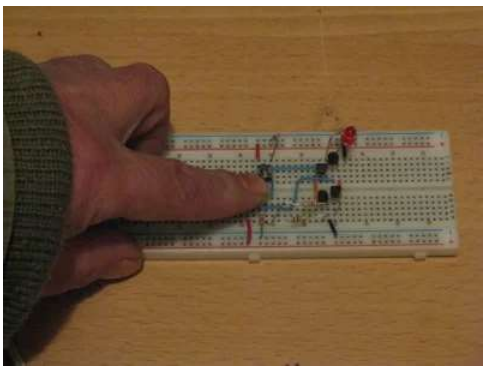
| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

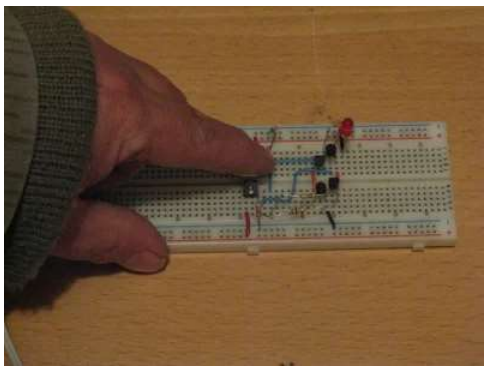
2 Input Transistor Xnor Gate

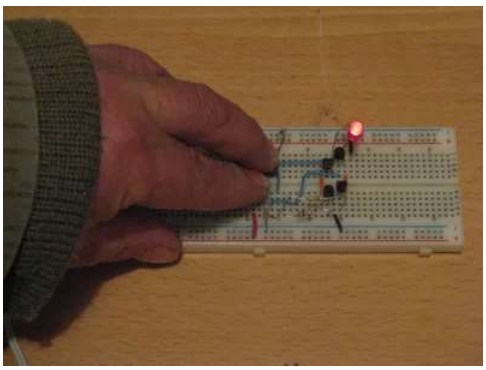








The Exclusive Nor gate is configured as two Nand gates connected in parallel as a Nor gate with the two top transistors PNP transistors.

When the inputs, (A and B) of the Xnor gate is 0 or 0 volts both of the NPN transistors are open and both the PNP transistors are closed. The output, (Q) is 1 or +5 volts and any positive current goes out of the output (Q).

When the input, (A) of the Xnor gate is 1 or +5 volts the NPN transistor on A input is closed and the PNP transistor is open. With the input, (B) of the Xnor gate is 0 or 0 volts the PNP transistor on B input is closed and the NPN transistor is open. The output, (Q) is 0 or 0 volts and any positive current goes to ground through the closed transistors.

When the input, (A) of the Xnor gate is 0 or 0 volts the NPN transistor on A input is open and the PNP transistor is closed. With the input, (B) of the Xnor gate is 1 or +5 volts the PNP transistor on B input is open and the NPN transistor is closed. The output, (Q) is 0 or 0 volts and any positive current goes to ground through the closed transistors.

When the inputs, (A and B) of the Xnor gate is 1 or +5 volts the both of the NPN transistors are closed and both the PNP transistors are open. The output, (Q) is 1 or +5 volts and any positive current goes

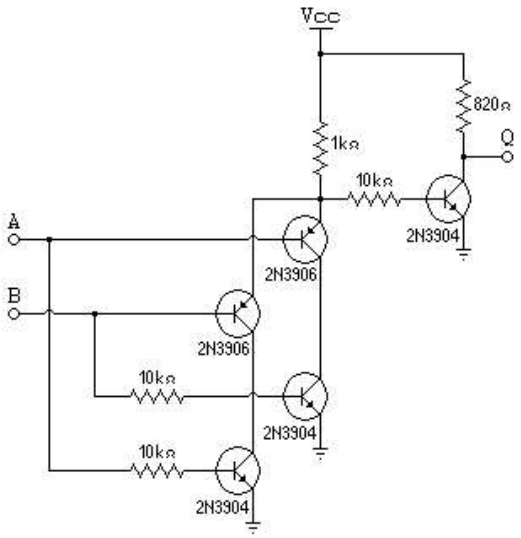
out of the output (Q).

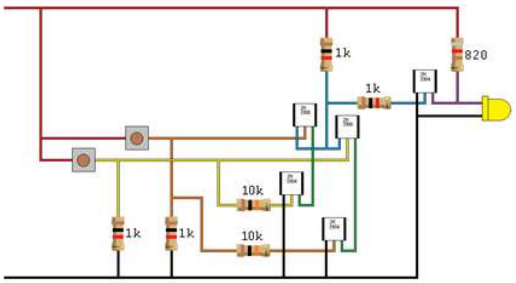
# Step 10: Exclusive or Gate (Xor)

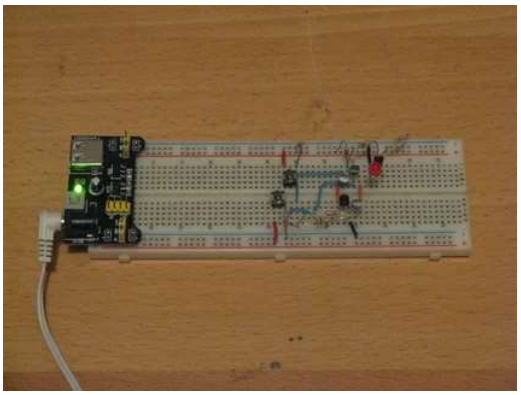
2 Input Xor Gate

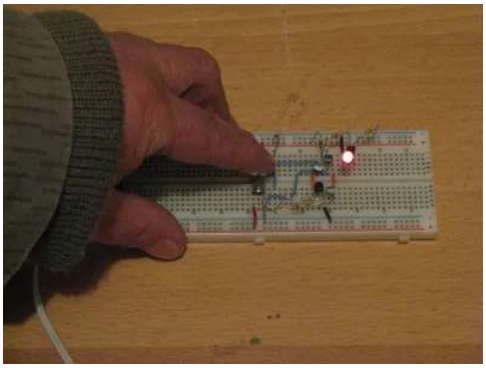

| Truth Table | | |
|---|---|---|
| Input | | Output |
| A | B | Q |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

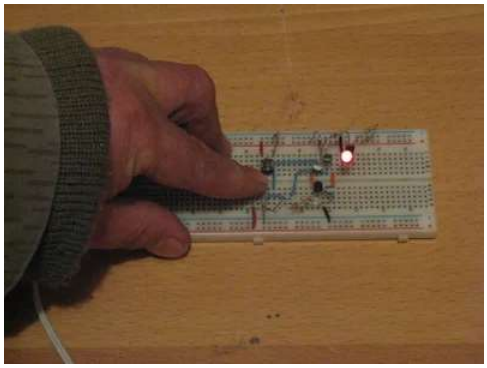
2 Input Transistor Xor Gate

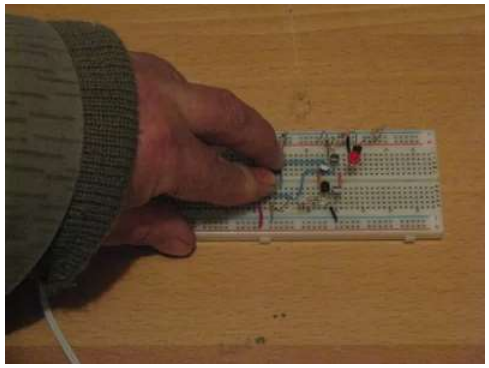








The Exclusive Or gate; uses all three of the key gates, it is configured as two Nand gates connected in parallel as a Nor gate with the two top transistors PNP transistors and a Not or Inverter gate in series.

The Xor gate inputs are the same as the Xnor gate however the output is reversed by the Not or Inverter gate.

When the inputs, (A and B) of the Xnor gate is 0 or 0 volts both of the NPN transistors are open and both the PNP transistors are closed and the output of the first set of gates is 1 or +5 volts. When the input of the Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.

When the input, (A) of the Xnor gate is 1 or +5 volts the NPN transistor on A input is closed and the PNP transistor is open. With the input, (B) of the Xnor gate is 0 or 0 volts the PNP transistor on B input is closed and the NPN transistor is open, 0 or 0 volts to the input of the Inverter. When the input of the Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

When the input, (A) of the Xnor gate is 0 or 0 volts the NPN transistor on A input is open and the PNP transistor is closed. With the input, (B) of the Xnor gate is 1 or +5 volts the PNP transistor on B input is open and the NPN transistor is closed, 0 or 0 volts to the input of the Inverter. When the input of the

Inverter gate is 0 or 0 volts the NPN transistor is open and the output, (Q) is 1 or +5 volts and any positive current goes out the output (Q).

When the inputs, (A and B) of the Xnor gate is 1 or +5 volts the both of the NPN transistors are closed and both the PNP transistors are open When the input of the second Inverter gate is 1 or +5 volts the NPN transistor is closed and the output, (Q) is 0 or 0 volts and any positive current goes to ground through the transistor.