Lab 6 - Part 1

Group 49

Timing Diagrams

Instructions

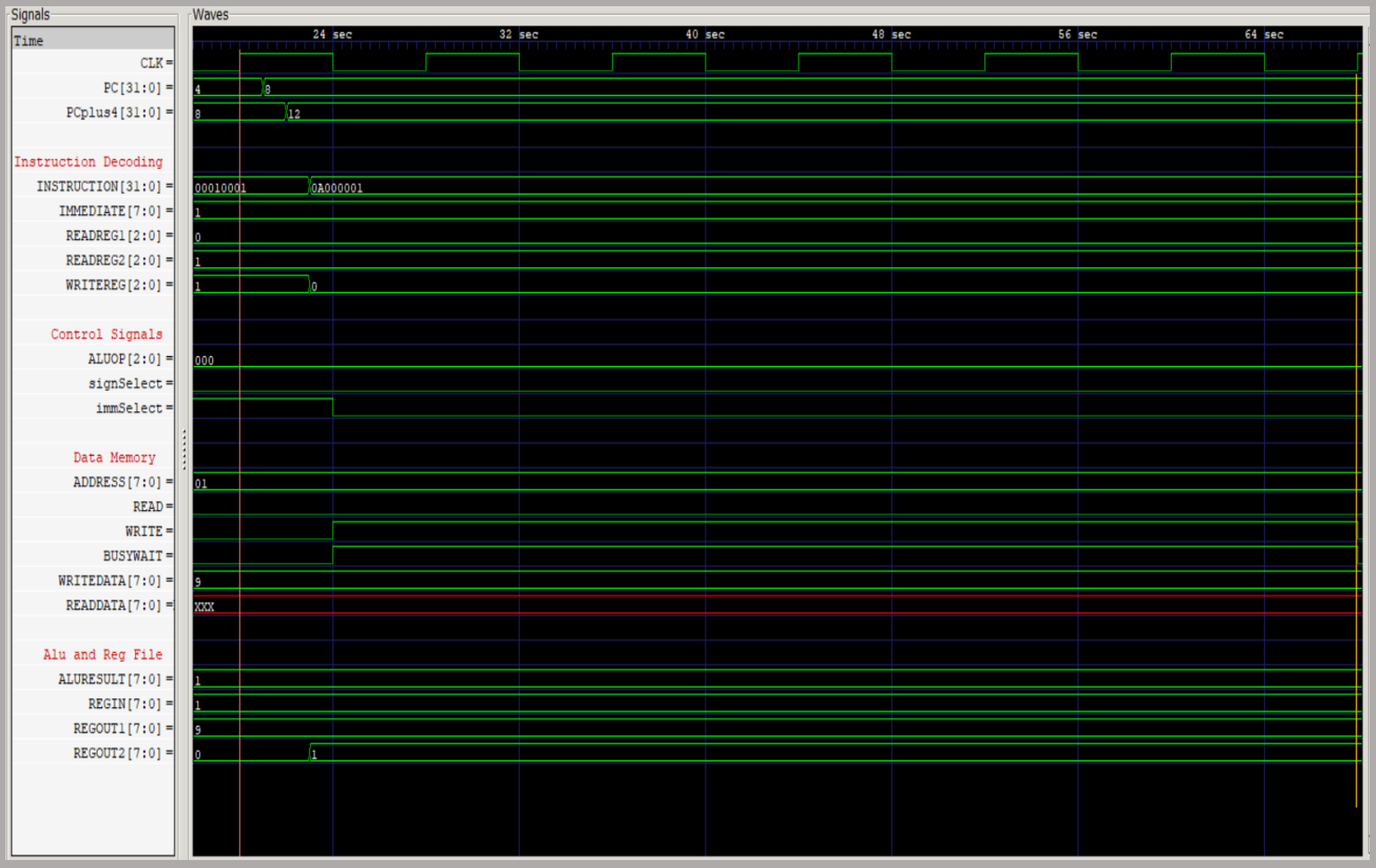
```
//This is a sample assembly program for CO224 Lab 5
loadi 0 0x09
loadi 1 0x01
swd 0 1
swi 1 0x00
lwd 2 1
lwd 3 1
sub 4 0 1
swi 4 0x02
lwi 5 0x02
swi 4 0x20
lwi 6 0x20
```

```
00001001 00000000 00000000 00000000
00000001 00000000 00000001 00000000
00000001 00000000 00000000 00001010
00000000 00000000 00000001 00001011
00000001 00000000 00000010 00001000
00000001 00000000 00000011 00001000
00000001 00000000 00000100 00000011
00000010 00000000 00000100 00001011
00000010 00000000 00000101 00001001
00100000 00000000 00000100 00001011
00100000 00000000 00000110 00001001
```

```
# Opcode Definitions dictionary
opcodes = {
    "loadi": "00000000",
    "mov": "00000001",
    "add": "00000010",
    "sub": "00000011",
    "and": "00000100",
    "or": "00000101",
    "j": "00000110",
    "beq": "00000111",
    "lwd": "00001000",
    "lwi": "00001001",
    "swd": "00001010",
    "swi": "00001011",
}
```

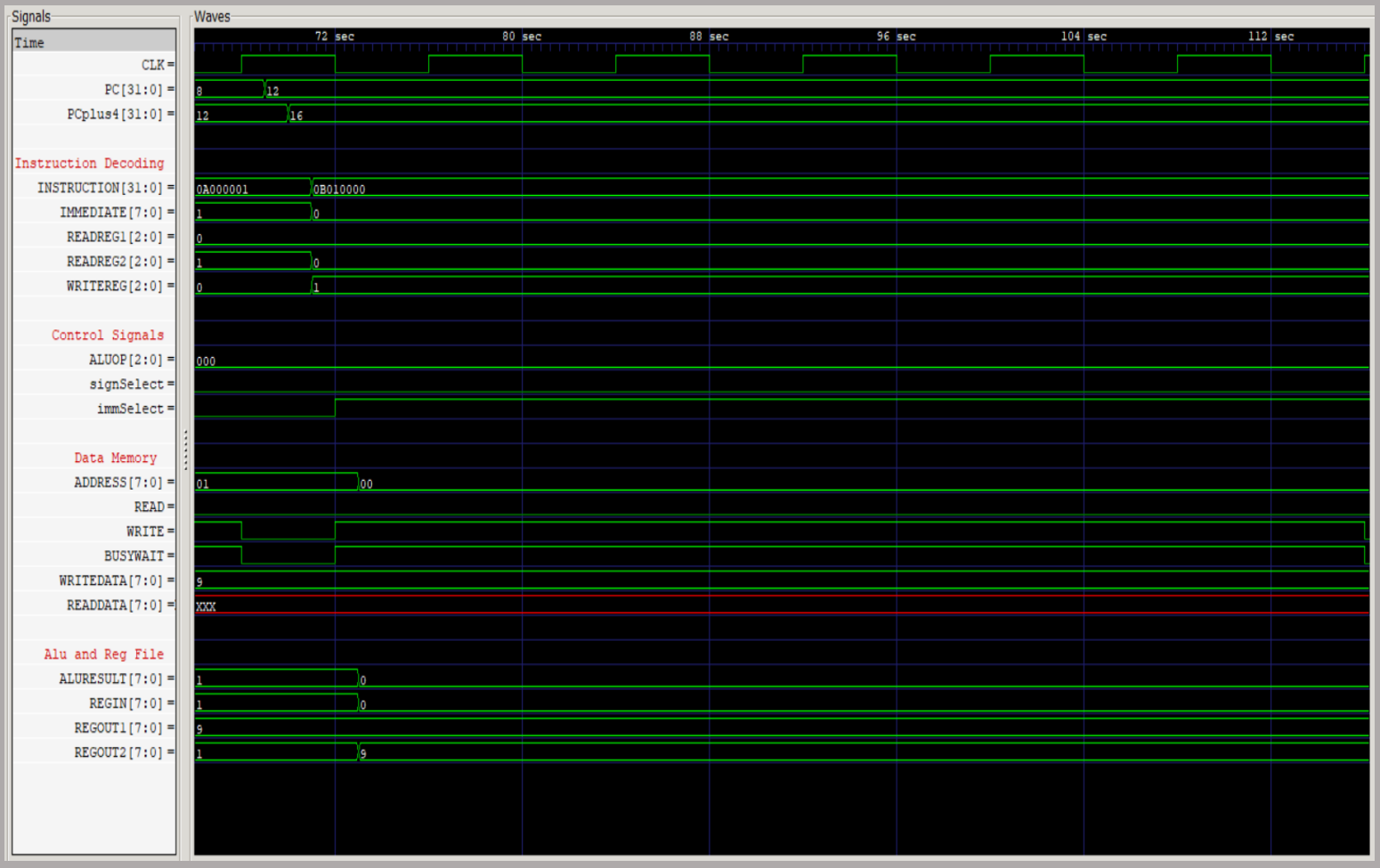
```
================================================
 Change of register Content Starting from Time #5
================================================

time    reg0    reg1    reg2    reg3    reg4    reg5    reg6    reg7
------------------------------------------------------------------------
   5       0       0       0       0       0       0       0       0
  13       9       0       0       0       0       0       0       0
  21       9       1       0       0       0       0       0       0
 165       9       1       9       0       0       0       0       0
 213       9       1       9       9       0       0       0       0
 221       9       1       9       9       8       0       0       0
 317       9       1       9       9       8       9       0       0
 413       9       1       9       9       8       9       9       0
```

1. swd 0 1



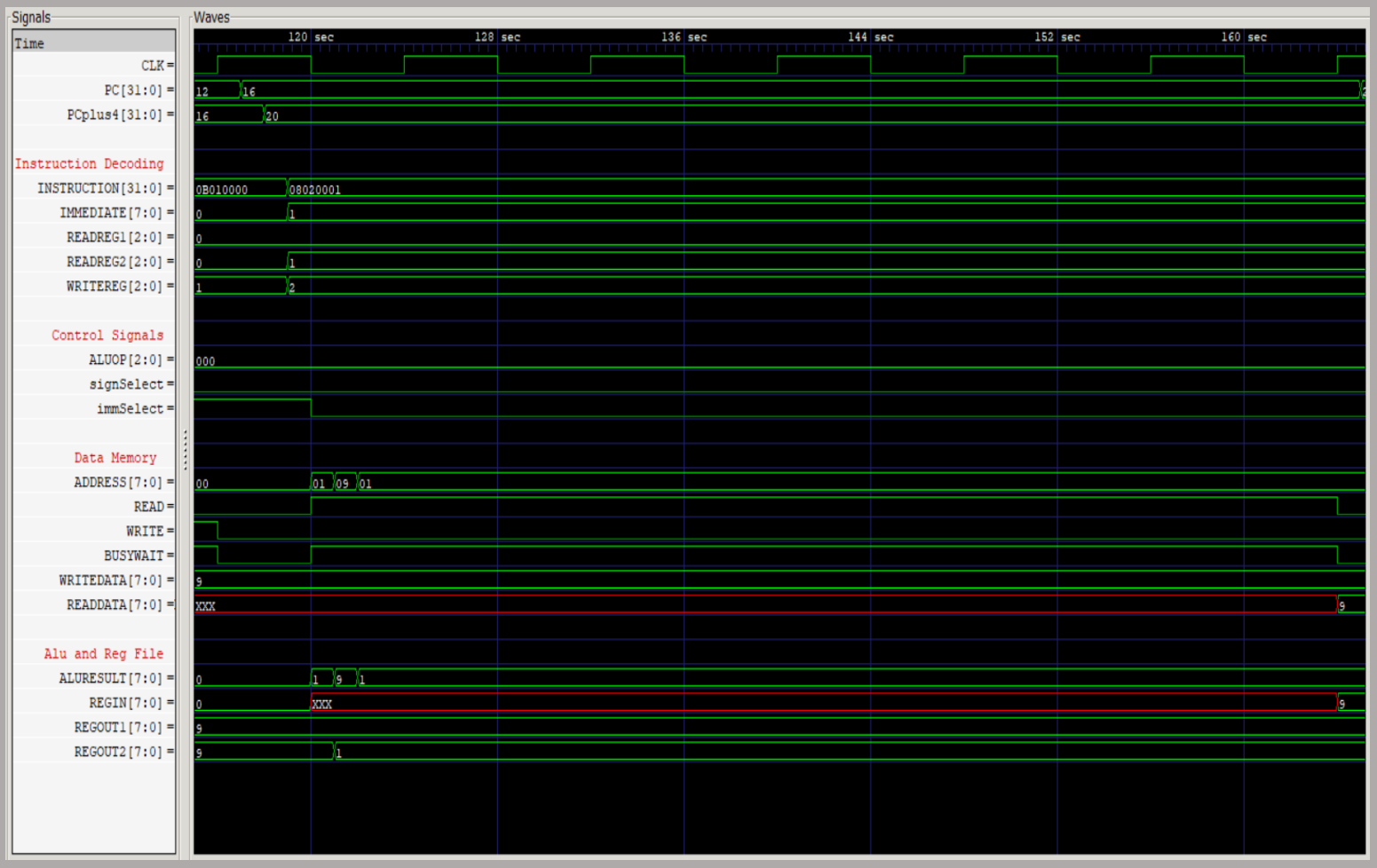
PC Update	Instruction Memory Read		Register Read		ALU	Data Memory Access
#1	#2		#2		#1	#2
	PC+4 Adder		Decode			
	#1		#1			

2. swi 1 0x00



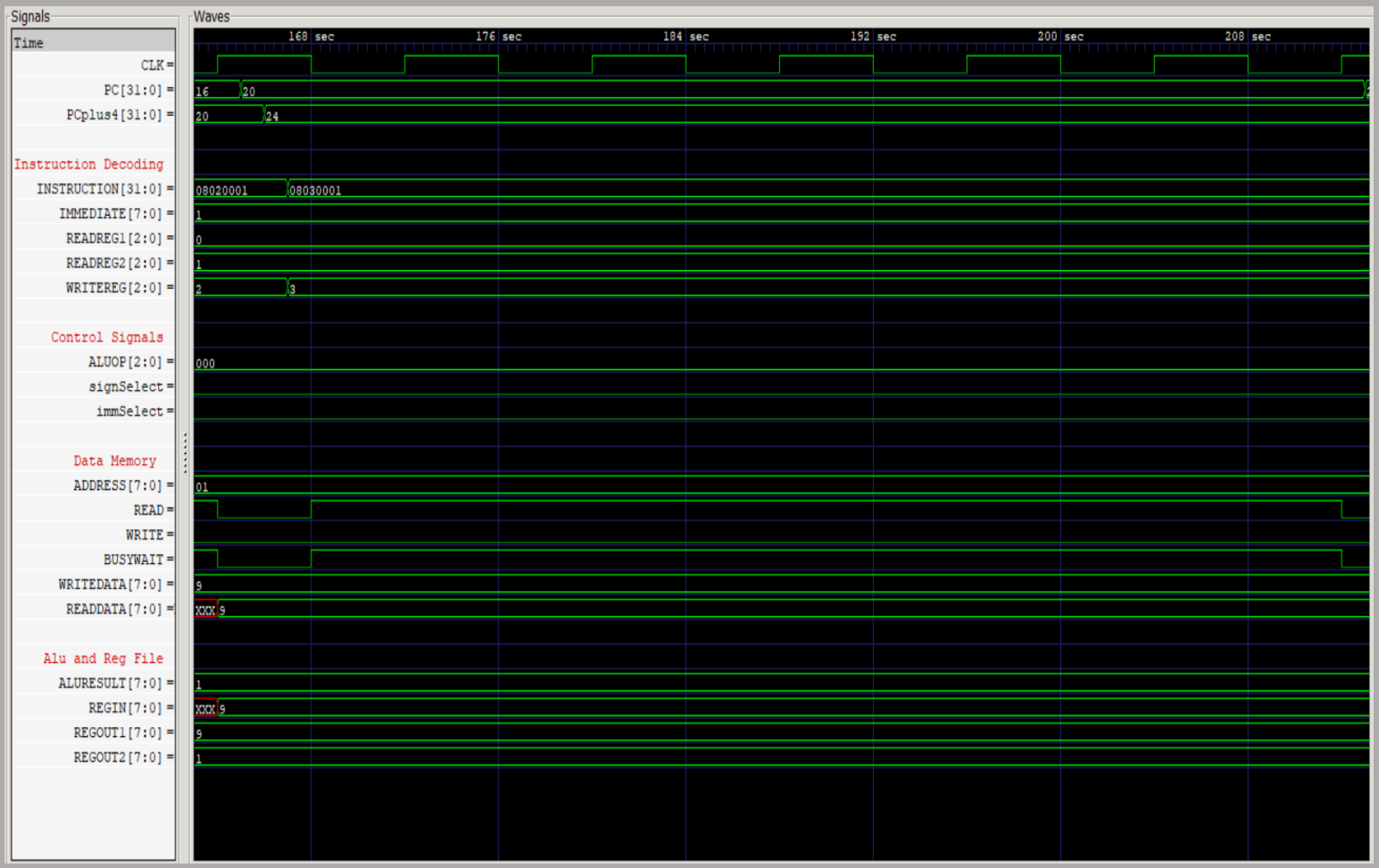
PC Update	Instruction Memory Read		Register Read		Data Memory Access	
#1	#2		#2		#2	
	PC+4 Adder		Decode	ALU		
	#1		#1	#1		

3. lwd 2 1



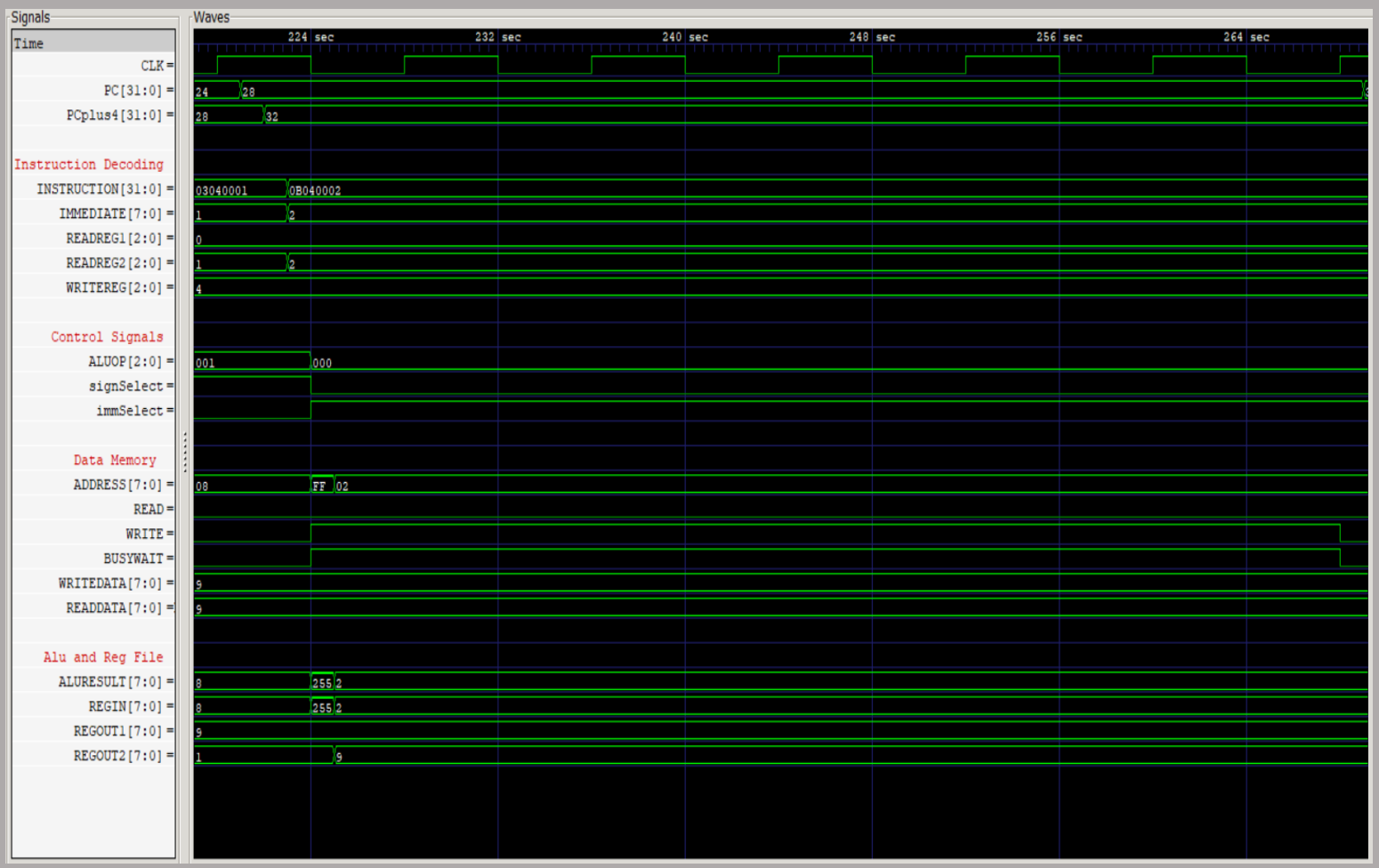
PC Update	Instruction Memory Read		Register Read	ALU	Data Memory Access
#1	#2		#2	#1	#2
	PC+4 Adder		Decode		
	#1		#1		
Register Write					
#1					

4. lwd 3 1



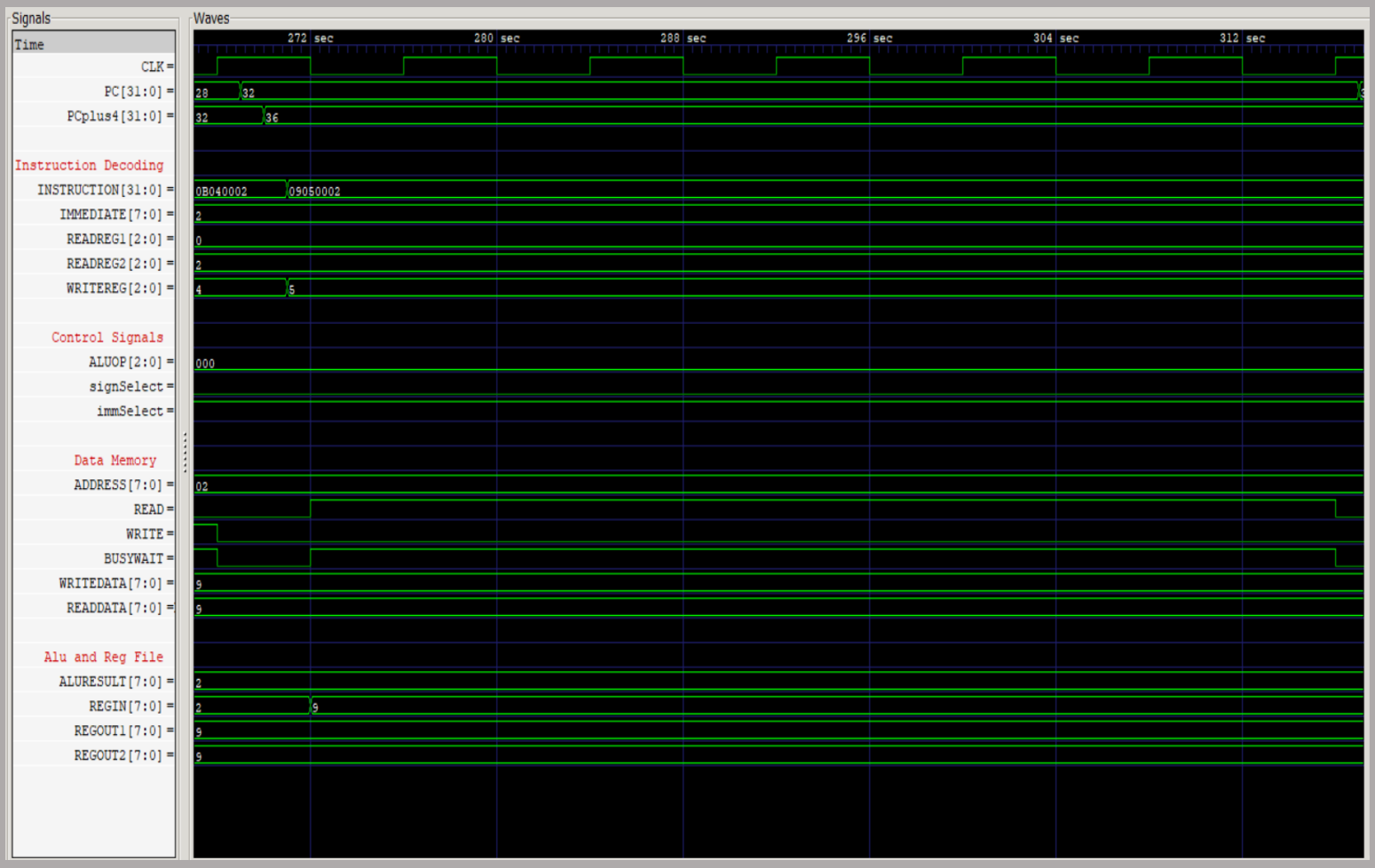
PC Update	Instruction Memory Read		Register Read	ALU	Data Memory Access
#1	#2		#2	#1	#2
	PC+4 Adder		Decode		
	#1		#1		
Register Write					
#1					

5. swi 4 0x02



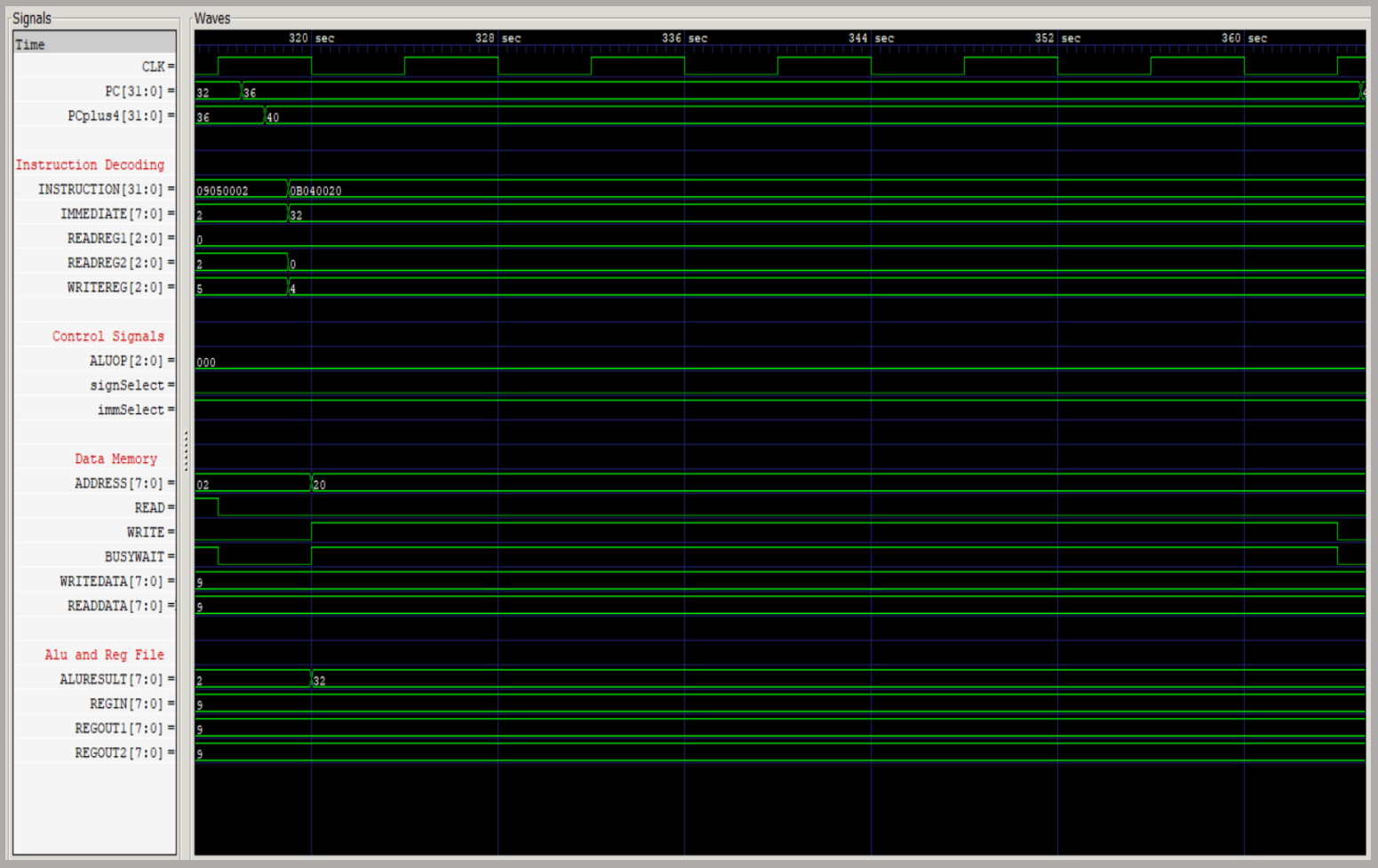
PC Update	Instruction Memory Read		Register Read		Data Memory Access	
#1	#2		#2		#2	
	PC+4 Adder		Decode	ALU		
	#1		#1	#1		

6. lwi 5 0x02



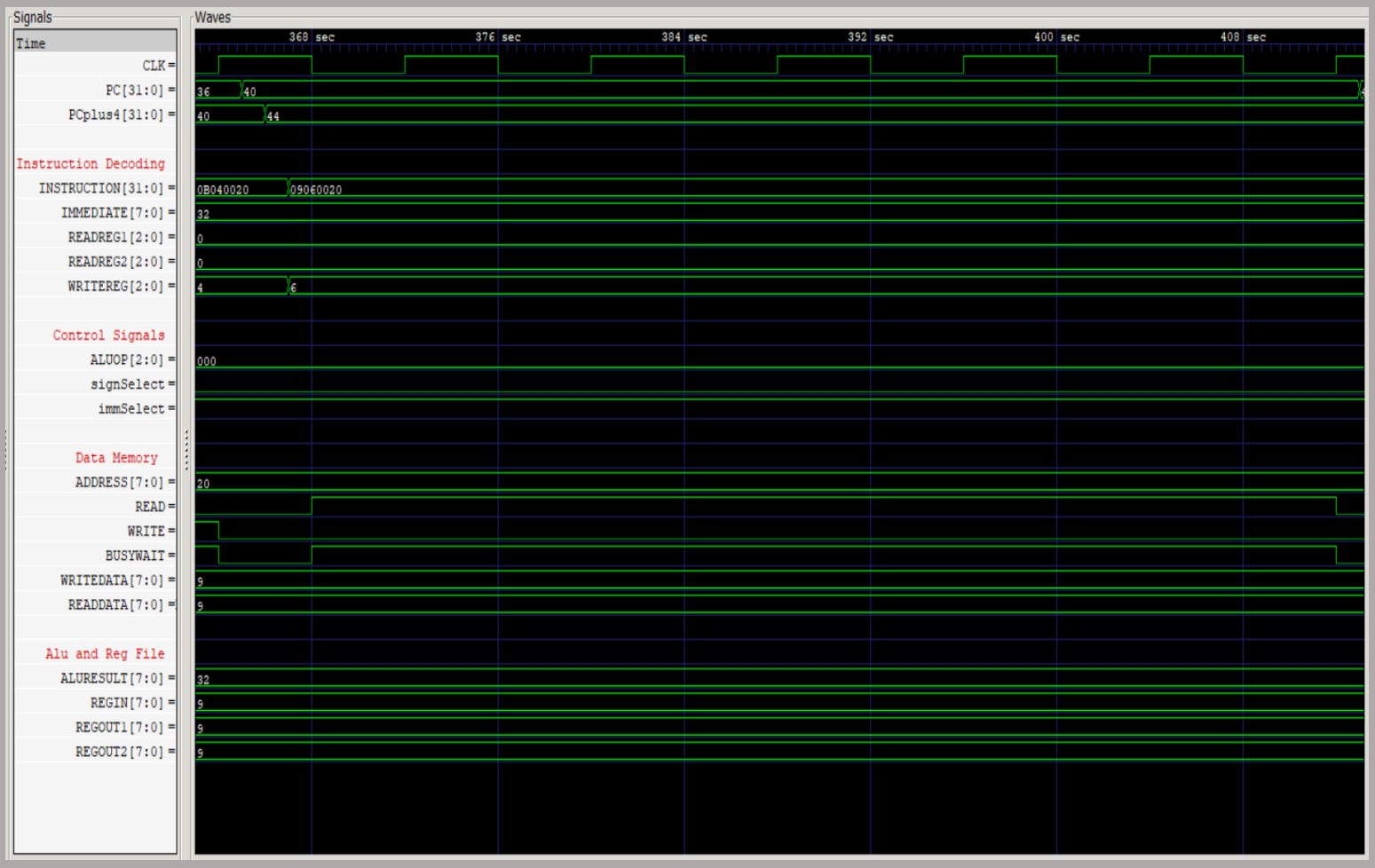
PC Update	Instruction Memory Read			ALU	Data Memory Access	
#1	#2			#1	#2	
	PC+4 Adder		Decode			
	#1		#1			
Register Write						
#1						

7. swi 4 0x20



PC Update	Instruction Memory Read		Register Read		Data Memory Access	
#1	#2		#2		#2	
	PC+4 Adder		Decode	ALU		
	#1		#1	#1		

8. lwi 6 0x20



PC Update	Instruction Memory Read			ALU	Data Memory Access	
#1	#2			#1	#2	
	PC+4 Adder		Decode			
	#1		#1			
Register Write						
#1						