Program Studi Teknik Elektro ITB

Nama Kuliah (Kode) : Praktikum Arsitektur Sistem Komputer (EL3111)
Tahun / Semester : 2023-2024 / Ganjil
Modul : 4-Synthesizable MIPSpc32® Microprocessor Bagian I Instruction Set, Register, Dan Memory
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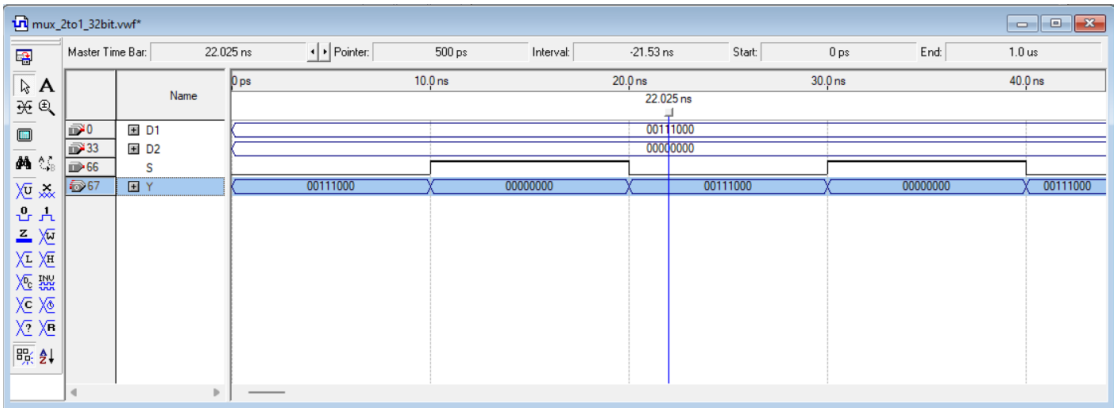
Tugas Pendahuluan

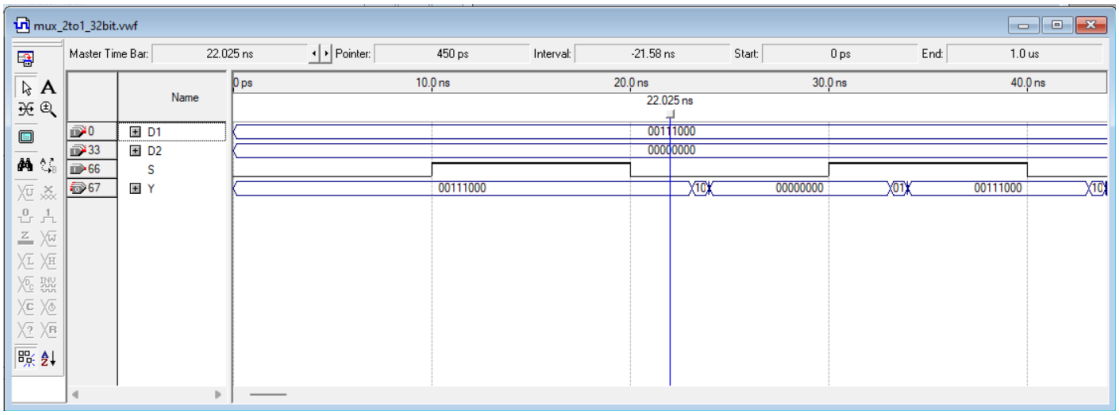
1. **Buatlah komponen 2-to-1 multiplexer dengan lebar data 32-bit dalam bahasa VHDL lalu simulasikan dalam simulasi fungsional dan timing.**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity mux_2to1_32bit is
  port (
    D1 : in std_logic_vector(31 downto 0); -- Data Input 1
    D2 : in std_logic_vector(31 downto 0); -- Data Input 2
    Y  : out std_logic_vector(31 downto 0); -- Selected Data
    S  : in std_logic
  );
end entity mux_2to1_32bit;

architecture Behavioral of mux_2to1_32bit is
begin
  process(S, D1, D2)
  begin
    if S = '0' then
      Y <= D1; -- Select Data Input 1
    else
      Y <= D2; -- Select Data Input 2
    end if;
  end process;
end architecture Behavioral;
```

Simulasi Functional



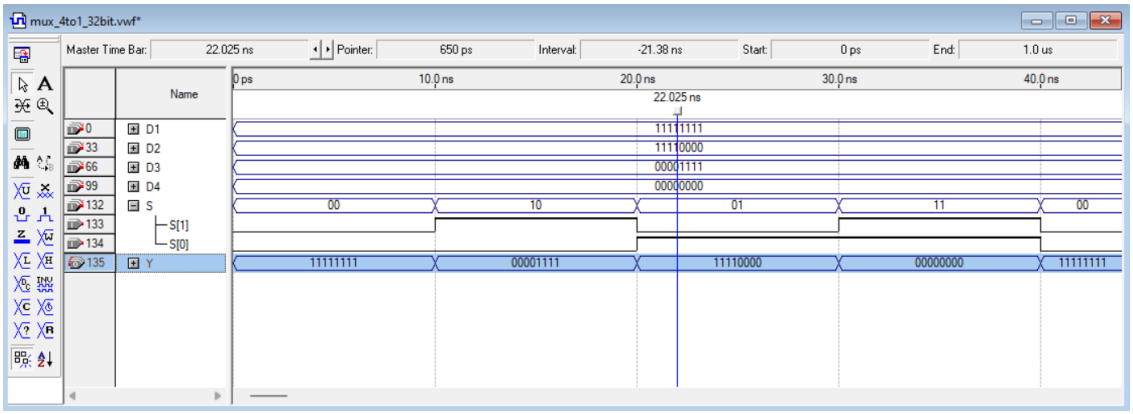
Simulasi Timing



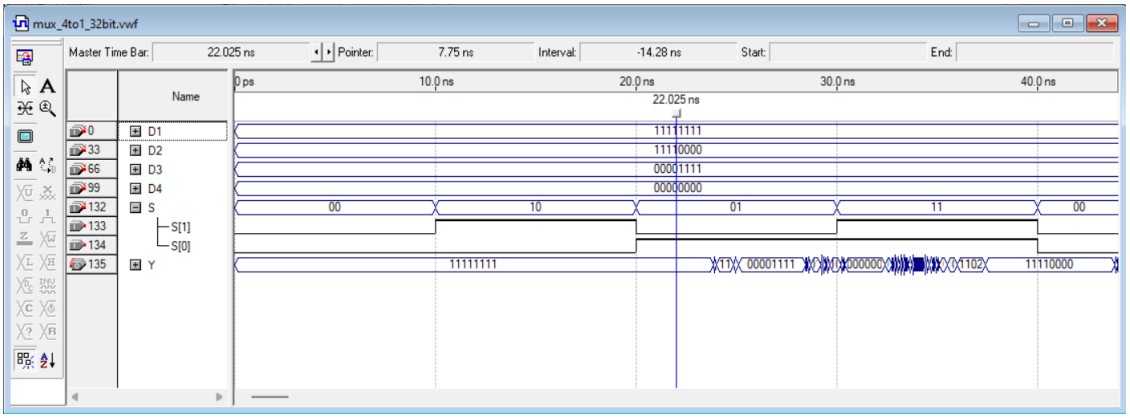
2. **Buatlah komponen 4-to-1 multiplexer dengan lebar data 32-bit dalam bahasa VHDL lalu simulasikan dalam simulasi fungsional dan timing.**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity mux_4to1_32bit is
  port (
    D1 : in std_logic_vector(31 downto 0); -- Data Input 1
    D2 : in std_logic_vector(31 downto 0); -- Data Input 2
    D3 : in std_logic_vector(31 downto 0); -- Data Input 3
    D4 : in std_logic_vector(31 downto 0); -- Data Input 4
    Y  : out std_logic_vector(31 downto 0); -- Selected Data
    S  : in std_logic_vector(1 downto 0)      -- 2-bit Selector
  );
end entity mux_4to1_32bit;


architecture Behavioral of mux_4to1_32bit is
begin
  process(S, D1, D2, D3, D4)
  begin
    case S is
      when "00" =>
        Y <= D1;  -- Select Data Input 1
      when "01" =>
        Y <= D2;  -- Select Data Input 2
      when "10" =>
        Y <= D3;  -- Select Data Input 3
      when others =>
        Y <= D4;  -- Select Data Input 4
    end case;
  end process;
end architecture Behavioral;
```

Simulasi Functional



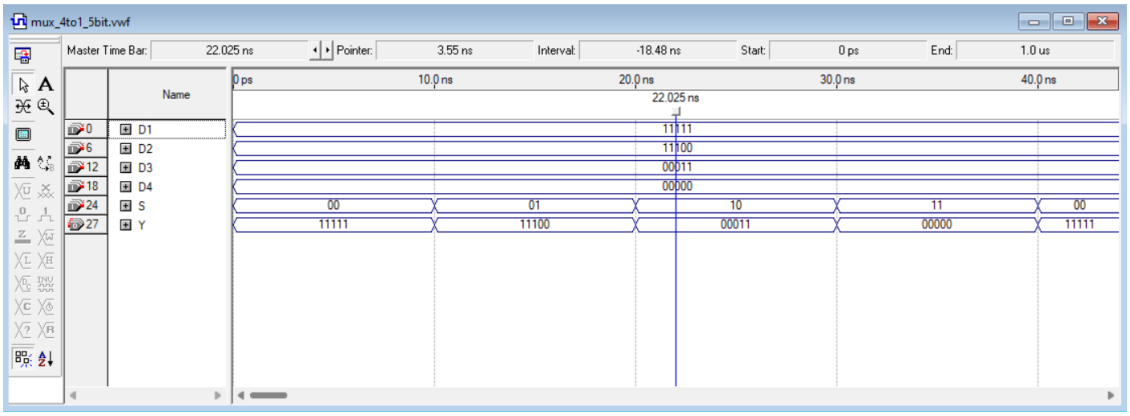
Simulasi Timing



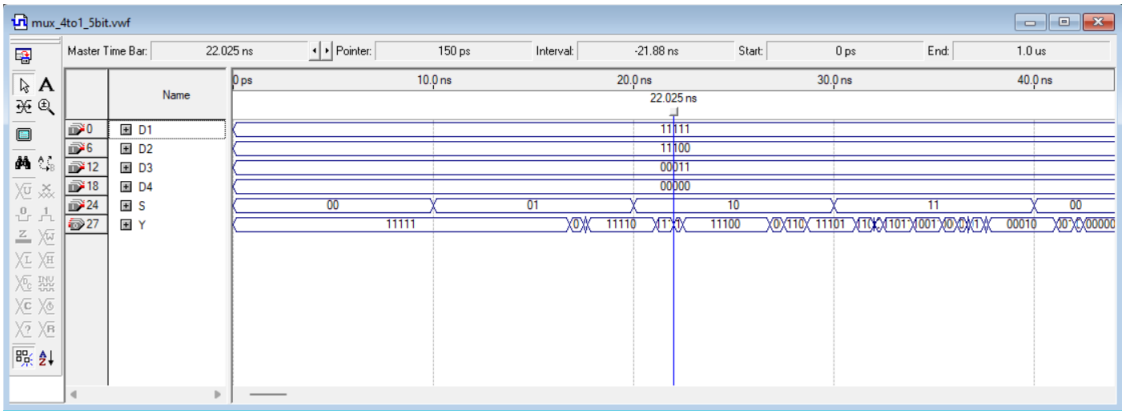
3. **Buatlah komponen 4-to-1 multiplexer dengan lebar data 5-bit dalam bahasa VHDL lalu simulasikan dalam simulasi fungsional dan timing.**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity mux_4to1_5bit is
  port (
    D1 : in std_logic_vector(4 downto 0);    -- Data Input 1
    D2 : in std_logic_vector(4 downto 0);    -- Data Input 2
    D3 : in std_logic_vector(4 downto 0);    -- Data Input 3
    D4 : in std_logic_vector(4 downto 0);    -- Data Input 4
    Y  : out std_logic_vector(4 downto 0);   -- Selected Data
    S  : in std_logic_vector(1 downto 0)     -- 2-bit Selector
  );
end entity mux_4to1_5bit;

architecture Behavioral of mux_4to1_5bit is
begin
  process(S, D1, D2, D3, D4)
  begin
    case S is
      when "00" =>
        Y <= D1;  -- Select Data Input 1
      when "01" =>
        Y <= D2;  -- Select Data Input 2
      when "10" =>
        Y <= D3;  -- Select Data Input 3
      when others =>
        Y <= D4;  -- Select Data Input 4
    end case;
  end process;
end architecture Behavioral;
```

Simulasi Fungsional



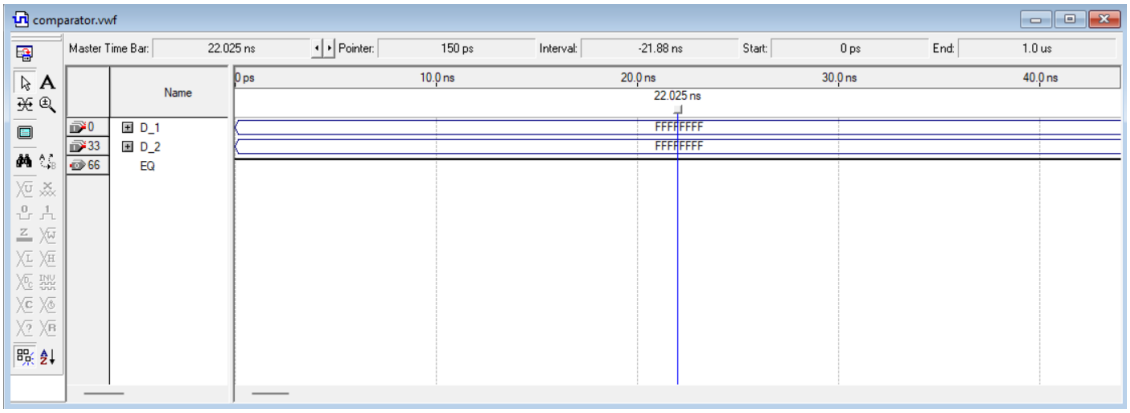
Simulasi Timing

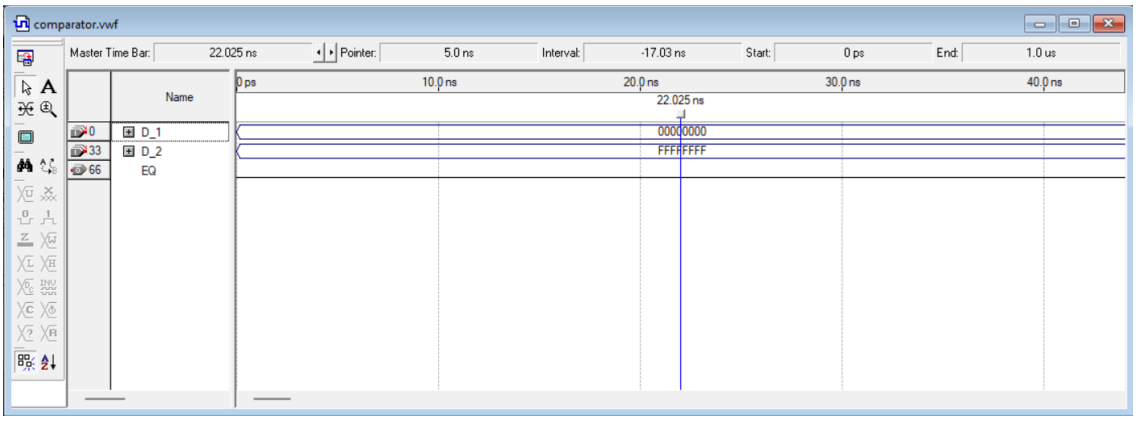


4. **Buatlah komponen komparator dengan dua buah input dengan lebar data 32-bit dalam bahasa VHDL lalu simulasikan dalam simulasi fungsional dan timing. Komparator akan menghasilkan output high saat kedua input sama. Komparator akan menghasilkan output low saat kedua input berbeda.**

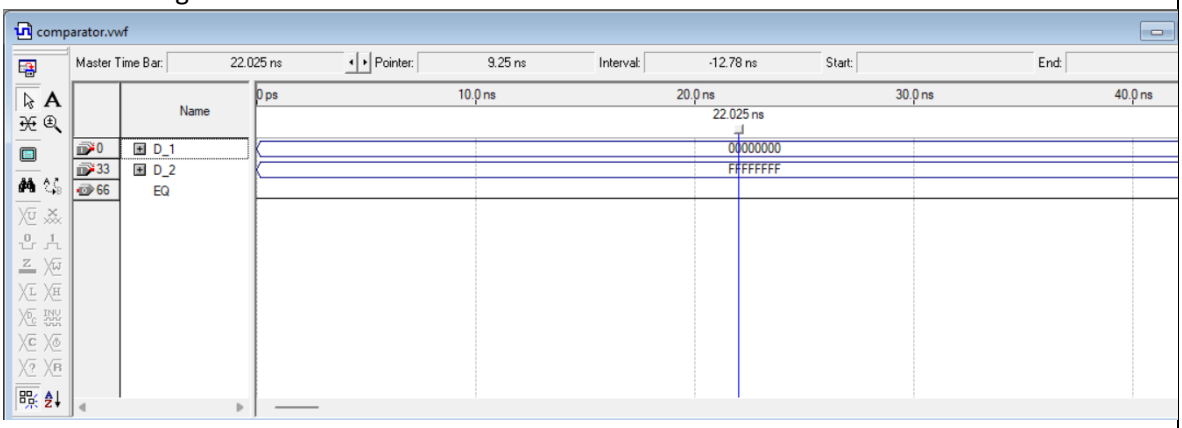
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY comparator IS
  PORT (
    D_1 : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
    D_2 : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
    EQ : OUT STD_LOGIC -- Comparison result EQ
  );
END comparator;

ARCHITECTURE Behavioral OF comparator IS
BEGIN
  PROCESS(D_1, D_2)
  BEGIN
    IF D_1 = D_2 THEN
      EQ <= '1'; -- Output high when inputs are equal
    ELSE
      EQ <= '0'; -- Output low when inputs are different
    END IF;
  END PROCESS;
END Behavioral;
```

Simulasi Fungsional





Simulasi Timing

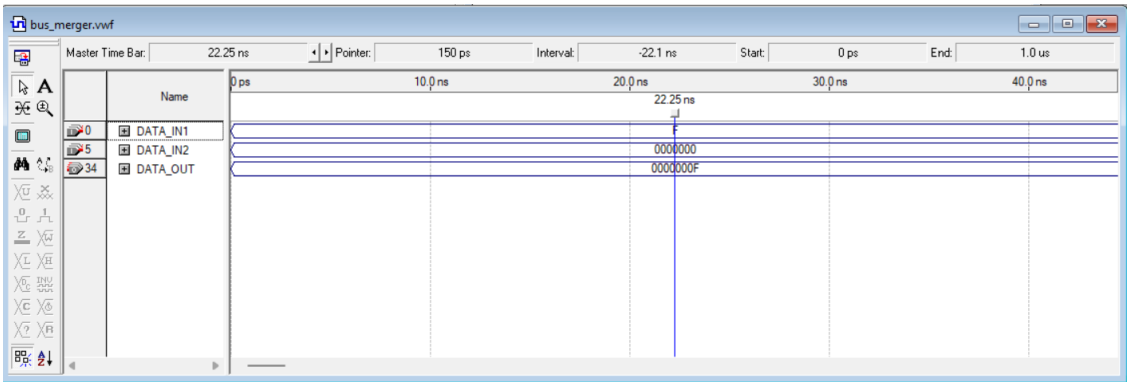


5. **Buatlah komponen bus merging yang menerima dua buah input dengan lebar 4 bit dan 28 bit untuk digabung menjadi satu buah output dengan lebar 32-bit dalam bahasa VHDL lalu simulasikan dalam simulasi fungsional dan timing.**

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY bus_merger IS
PORT (
     DATA_IN1 : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
     DATA_IN2 : IN STD_LOGIC_VECTOR (27 DOWNTO 0);
     DATA_OUT : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
);
END bus_merger;
```

```
ARCHITECTURE arch_bus_merger OF bus_merger IS
BEGIN
    DATA_OUT <= DATA_IN2 & DATA_IN1;
END arch_bus_merger;
```

Simulasi Fungsional



Simulasi Timing