ECE 200 Digital Logic Design
Drexel University
Fall 2020-2021

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Course description: The course introduces number systems and representation, two's complement arithmetic, digital logic devices, switching algebra, truth tables, minimization of boolean functions, combination logic design and analysis, sequential circuit analysis and design. Course material (notes, assignments, solutions, grades) will be distributed over Blackboard Learn, which can be reached through Drexel.

Textbook (Required):

Interactive/Electronic: Zybooks Digital Design Book

- Sign up at zyBooks.com
- Enter zyBook code **DREXELECE200TaskinFall2020**
- Click *Subscribe*
- A subscription is **$58** and will last until Jan 09, 2021.

Instructor's personal note about the book choice: The electronic book choice is not a typical e-book. It has interactive learning components that supplement an abridged version of the textbook. The electronic (zybooks) version is cheaper, allows printing of the pdfs while the subscription is active but would need renewal subscription to have the interactive portions alive after the quarter. There are also many other Digital Logic books on the market (old and new – old versions are just as good) that you can purchase, if you would like to have a paper book in your library post-ECE 200.

Course Topics

We will study the following topics:

- Number systems and binary addition
- Logic components
- Analysis and design of combinational circuits, arithmetic circuits

- Latches and Flip-flops
- Analysis and design of sequential circuits
- Registers and counters, memory and programmable logic

Course Outcomes

1. Perform number conversions to different bases
2. Calculate binary addition
3. Demonstrate an ability to use Boolean algebra, truth tables, sum of products and product of sum to represent logic functions
4. Perform minimization of Boolean functions
5. Solve combinational logic design
6. Represent a sequential system using a finite state machine
7. Design sequential systems including registers and combinational logic
8. Demonstrate competence in analyzing a digital design represented in a hardware design language (eg, VHDL, Verilog)

Grading

- Final: 30%
- Midterm: 25%
- Zybooks (P&C), homework problems: 15%
- Quizzes: 15%
- Labs: 15%

The Academic Policies of Drexel University Office of the Provost dictates the scale of letter grades http://www.drexel.edu/provost/policies/grades.asp. Below are the percentages to be used in assignment of these grades:

Letter Grade percentage A+ 100–97, A 96.9 – 93, A- 92.9 – 90, B+ 89.9 – 87, B 86.9 – 83, B- 82.9 – 80, C+ 79.9 – 77, C 76.9 – 73, C- 72.9 – 70, D+ 69.9 – 67, D 66.9 – 63, F Below 63

The instructor reserves the right to adjust the grade percentages (e.g. based on the distribution of grades) to accommodate non-standard (low or high) distributions.

Policies

The overall grade will be a weighted sum of the components listed above. No components will be curved but the overall grade itself will be. Late homework will NOT be accepted once the solutions are posted on the website.

As Drexel will remain closed, all lectures, recitations, and laboratory meetings will be online through Zoom. Lectures and recitation videos will be posted, labs will be synchronous and may not be recorded.

Both the Midterm and Final will be open-book, open-note, take home exams, where each student will be given 24 hours to submit their completed exam. Each student is to work on their own for both exams.

For laboratory exercises, beyond the meeting with the TA hosting the lab, students will be asked to use a remote desktop or install ModelSim on their local computers to complete lab assignments. Information provided by the College of Engineering IT group on how to login to the remote desktop is as follows:

> The Windows remote desktop server has 192GB of RAM available to it (dynamically allocated, so it won't necessarily show that much all the time). Please follow the instructions at
>
> https://tech.coe.drexel.edu/labs/remotedesktop/
>
> to connect to the Windows remote desktop, and
>
> https://tech.coe.drexel.edu/labs/ece/xunil/
>
> for Xunil.

The software available on the remote desktop is for academic teaching only and not for research.

There will be no make-up exams unless arrangements are made in advance. Collaboration is permitted and encouraged on homework problems, but each student must hand in their own work. Academic dishonesty will not be tolerated. The academic policies defined by the Office of Provost are upheld for this course. The complete list of policies (academic and otherwise) is listed at http://www.drexel.edu/policies/. The students should particularly be aware of the following policies:

Academic Integrity	http://www.drexel.edu/provost/policies/academic dishonesty.asp
	http://www.drexel.edu/studentlife/judicial/honesty.html

Course Drop Statement	http://www.drexel.edu/provost/policies/course drop.asp
Disability Statement	http://www.drexel.edu/oed/disabilityResources/

Quizzes will be given during lecture or lab hours. There will be NO make-up quizzes. To compensate for the no make-up quiz policy, the lowest quiz will be dropped.

Please check your grades often and carefully. If you want to dispute any grade, it MUST be done within 3 week after the return of the homework, quiz, or exam.

Tentative Schedule

Week	*Monday*	*Wednesday*
Week 1 *Sep 21*	**Introduction 1.1-1.4, 8.1** Bits, Boolean, Radix, Hex, VHDL	**Section 1.6-1.11** Switches, Comb. Logic, Boolean algebra
Week 2 *Sep 28*	**Section 1.12-1.16,1.19** Boolean Properties, SoP, Minterms, Truth tables	**Section 8.2-8.3** Hardware design with VHDL
Week 3 *Oct 5*	**Section 2.1-2.4** K-maps	**Section 2.5-2.7** DeMorgan and Comb gates
Week 4 *Oct 12*	**Indigenous Peoples' Day**	**Section 2.8-2.12,4.6** Muxes, Decoders, Multi-bit MUX
Week 5 *Oct 19*	**Section 3.1-3.3** Load registers, Latch vs. FF review	**Section 4.7, 4.8, 6.5** Load and multi-function registers
Week 6 *Oct 26*	**Midterm review**	**MIDTERM EXAM**
Week 7 *Nov 2*	**Midterm review**	**Section 3.4-3.11** FSMs
Week 8 *Nov 9*	**Section 4.1-4.3** Adder, signed binary, subtraction	**Section 4.4-4.5** Comparators
Week 9 *Nov 16*	**Section 6.2,6.3** Adders, Multipliers	**Section 6.4-6.8** ALUs, SRAM/DRAM
Week 10 *Nov 23*	**Section 5.1-5.4** RTL Design I	**Thanksgiving**
Week 11 *Nov 30*	**Section 5.5-5.9** RTL Design II	**Final Exam Review**