Drexel University
College of Engineering
ECEC 302, Digital Systems Projects

1. ECEC 302, Digital System Projects
   https://courses.coe.drexel.edu/ECE/ECE-C302 access requires VPN

2. Credits: 3.00 Contact Hours: 100-minute Lecture and one 110-minute Lab

3. Instructor: Prawat Nagvajara, Ph.D. (Associate Professor) nagvajap@drexel.edu
   Office Bossone 103, 215 895-2378
   Hours: Wednesday 10-12 PM

   Teaching Assistant:
   Name and office hour

4. Textbook and Materials

Digital Systems Projects (Preliminary Edition), Cognella Academic Publishing, San Diego, CA. cognella.com, ISBN 978-1-7935-1437-0. Available for Purchase at https://store.cognella.com/83146-1B-001

5. Specific Course Information

   a. Brief description of the course (Course Catalog Description)
      To study the theory of digital system design and the top-down design methodology using hardware description language and software tools for simulation, synthesis and Field Programmable Gate Array (FPGA) implementation.
   b. Course Purpose within Electrical and Computer Engineering Program of Study
      This course covers rudimentary digital hardware design essential to development of systems in signal processing, telecommunication and controls.
   c. Pre-requisites or Co-requisites: ECE 200 (Minimum Grade: D)
   d. Required course in Computer Engineering program. Selected elective in Electrical Engineering program

6. Specific Goals for the Course

   a. Course Outcomes: Students will attain ability and knowledge to

      1. Design at a novice-level digital hardware systems comprising synchronous systems, state machines, combinational logic and data storages. Evaluated by in-lab design exam and assignment problems.
      2. Create design specifications and verification plan (debug and testing). Evaluated by in-lab design exam and assignment problems.
      3. Master design flow begins from Hardware Description Language (HDL), simulation, and synthesis of hardware from HDL on programmable electronics (Field Programmable Gate Array, FPGA). Evaluated by in-lab design exam and assignment problems.
      4. Use behavioral design HDL to create non-trivial systems. Evaluated by in-lab design exam and assignment problems.

5. Manipulate arithmetical digital numbers. Evaluated by in-lab design exam and assignment problems.
6. Map algorithms to hardware using data dependency graph and design pipeline parallelism hardware. Evaluated by in-lab design exam and assignment problems.
7. Use Intellectual Property (IP) cores in to create design. Evaluated by in-lab design exam and assignment problems.
8. Design circuits requiring asynchronous handshake synchronization. Evaluated by in-lab design exam and assignment problems.

b. Accreditation Board for Engineering and Technology (ABET) Student Outcomes
1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors

c. Drexel Student Learning Priorities (DSLPs)
Creative and Critical Thinking
Information Literacy
Self-directed Learning
Use of Technology Use
Professional Practice
Research, Scholarship and Creative Expression

7. Brief List of Topics by Weeks

7.1 Digital Systems Introduction – Theory, Hardware Description Language and Integrated Design Environment
7.2 Registers and Synchronous Circuits
7.3 State Machines
7.4 Combinational and Generic Parameters
7.5 Structural Description and Test Bench. Bit-vector arithmetical circuits (signed and unsigned).
7.6 Mapping algorithms to hardware: Data dependency graph, array structures
7.7 Pipeline Structure
7.8 Design with Intellectual Property Cores
7.9 Storages – Block RAM, Stack and First-In First-Out (FIFO) queues
7.10 Asynchronous handshake synchronization. Binary coded representation.

8. Evaluation

a. Evaluations on the labs, quizzes, and exams are based on student's demonstration of the design correctness and understanding. Students earn partial credits on incomplete designs by submitting attempted design codes for grading.

b. Labs
Eight Lab meetings
Evaluates on attendance (5%) and
Five Pre-lab and in-lab assignments announced one week before deadline (15%)
c. Exam
i. Two Quizzes 20% each 50 minutes during Week 4 and 8 Lectures
ii. Midterm 25% 100 minutes during Week 6 lab

iii. Final 35% 120 minutes during the examination week (Week 11)

d. Grades assignment

Score x
Grade : x < Upper Bound x ≥ Lower Bound

		Upper Bound	Lower Bound
A	:	x ≤ 100%	x ≥ 93%
A-	:	x < 93%	x ≥ 88%
B+	:	x < 88%	x ≥ 83%
B	:	x < 83%	x ≥ 78%
B-	:	x < 78%	x ≥ 73%
C+	:	x < 73%	x ≥ 68%
C	:	x < 68%	x ≥ 63%
C-	:	x < 63%	x ≥ 58%
D+	:	x < 58%	x ≥ 53%
D	:	x < 53%	x ≥ 48%
F	:	x < 48%	

9. Academic Policies

a. Academic Integrity, Plagiarism and Cheating Policy: Refer to "Student Conduct and Community Standards" www.drexel.edu/studentaffairs/community_standards/studentHandbook/
b. Students with Disabilities: Refer to http://drexel.edu/oed/disabilityResources/faculty/SyllabusStatement/
c. Course Drop Policy: Refer to http://www.drexel.edu/provost/policies/course_drop.asp
d. Course Change Policy: The instructor has the right to make changes to the course contents and the pedagogy. The changes will be announced prior to the action and the reasons will be communicated to students.