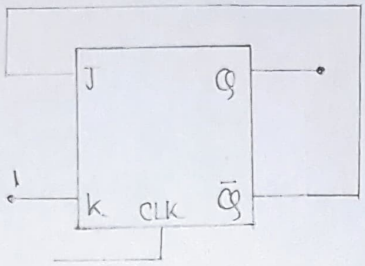
Q>1) In a J-K flip flop we have $J = \bar{Q}$ and $K = 1$ (see fig.). Assuming the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



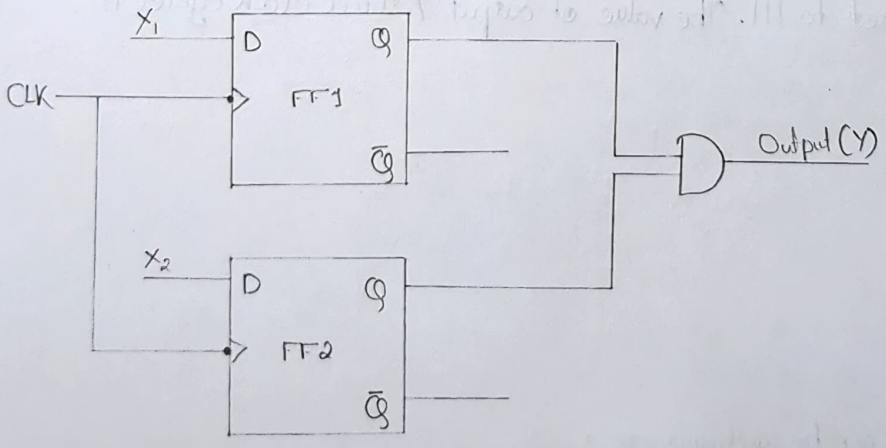
Ans→ Characteristics Table of JK flip-flop is:

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Output ~~table~~ →

Step	0	1	2	3	4	5	6
Q_n	0	1	0	1	0	1	0
$\bar{Q}_n$	1	0	1	0	1	0	1

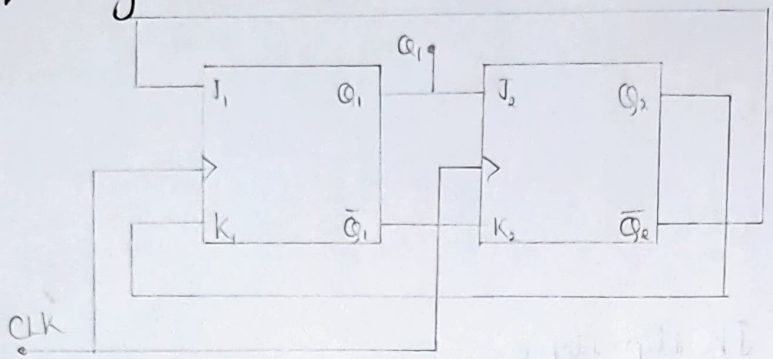
Q2) In the circuit shown, choose the correct timing diagram of the output (Y) from the given waveforms W_1, W_2, W_3 and W_4.



Ans→ Let Q_1 & Q_2 be output of the respective flip-flop. Since, its given that flip-flop is triggered at 0 or that it is a negative edge triggered.

We know that the function of the D flipflop is to follow the input when the flip-flop triggered. Here, the flip flop is triggered at the negative edge. So, output Y is similar to W_3.

3) The outputs of the two flip-flops Q_1, Q_2 in the figure shown are initialised to 0,0. The sequence generated at Q_1 upon application of clock signal is



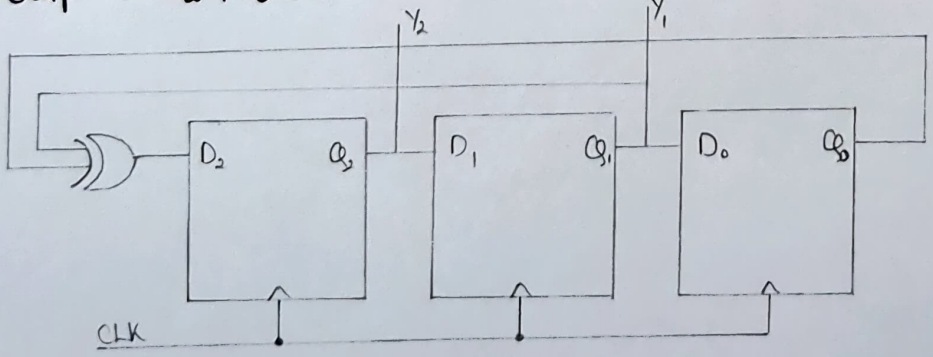
Ans → Initially Q_1 & Q_2 are 0,0

From the fig., $J_1 = \bar{Q}_2$, $K_1 = Q_2$, $J_2 = Q_1$, $K_2 = \bar{Q}_1$

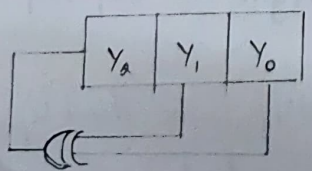
Clock	Present State				Flip Flop Inputs				Next State
	Q_1	$\bar{Q}_1$	Q_2	$\bar{Q}_2$	J_1	K_1	J_2	K_2	
1	0	1	0	1	1	0	0	1	1
2	1	0	0	1	1	0	1	0	1
3	1	0	1	0	0	1	1	0	0
4	0	1	0	1	1	0	0	1	0
5	0	1	0	1	1	0	0	1	0

$\therefore Q_1 = 01100$

Q) 4) A three bit pseudo ~~code~~ random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y three clock cycles is



Ans → The above circuit can be redrawn as →



$Y_2 = Y_1 \oplus Y_0$

Sequence Table:-

Output	Y_2	Y_1	Y_0
Initial	1	1	1
1st Clock	0	1	1
2nd clock	0	0	1
3rd clock	1	0	0

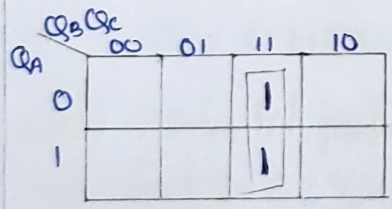
∴ The output in third cycle is 100.

5) Design a MOD 6 counter with T Flip-Flops.

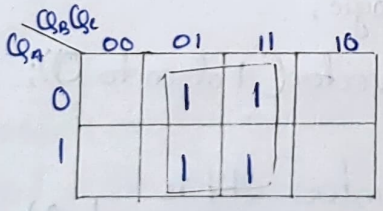
Ans→ By using MOD up

Flip Flop inputs→ T_A T_B T_C & CLK

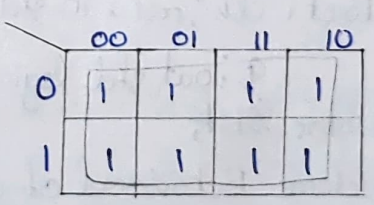
Present State			Next State			Flip Flop Inputs		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



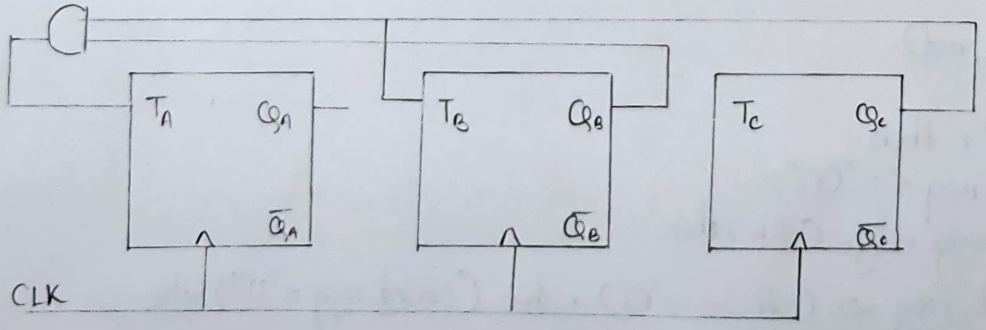
$T_A = Q_B Q_C$



$T_B = Q_C$



$T_C = 1$

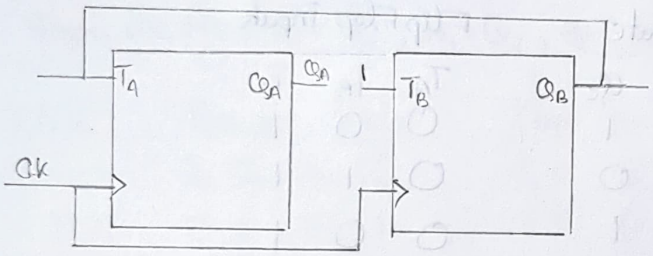


Q>6) Design a 2 bit synchronous up counter with T Flip-Flops and write an HDL behavioural description of the circuit.

Ans → State table with excitation table →

Present State		Next State		Flip Flop	
Q_A	Q_B	Q_A	Q_B	T_A	T_B
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

$T_A = Q_B$, $T_B = 1$



HDL Code →

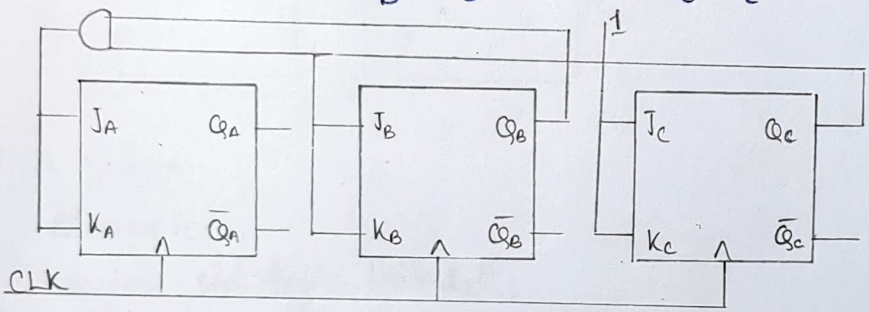
```
library ieee;
use ieee.std_logic_1164.all;
entity counter_2bit is
    Port (clk, rst : in std_logic;
          q : out std_logic_vector(1 down to 0));
end counter_2bit;
architecture Behavioral of counter_2bit is
    signal count_reg : std_logic_vector(1 downto 0) := "00";
begin
    process (clk, rst)
    begin
        if rst = '1' then
            count_reg <= "00";
        elsif rising_edge(clk) then
            count_reg <= (others => '0') when (count_reg = "11") else
                         count_reg + "01";
        end if;
    end process;
    q <= count_reg;
end Behavioral;
```

Q7) Design a 3-bit synchronous up counter with JK Flip-Flop.

Ans → State table →

Present State			Next State			Flip Flop Inputs					
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

$J_A = K_A = Q_B Q_C$ $\quad J_B = K_B = Q_C$, $\quad J_C = K_C = 1$



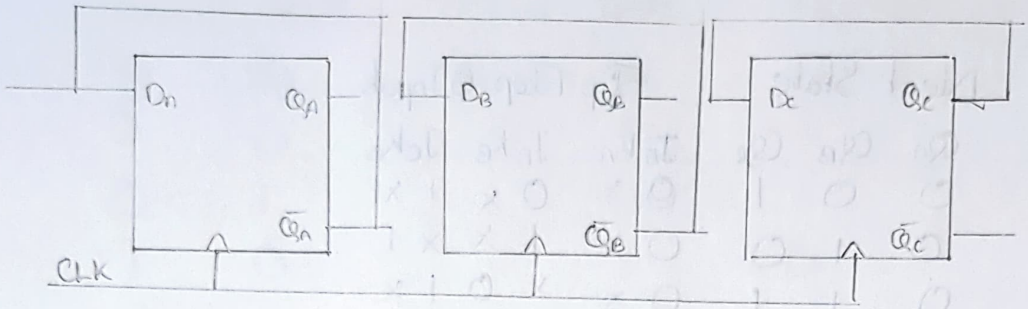
Q8) Design a 3 bit synchronous down counter with D flip flops.

Ans → State Table →

Present State			Next State			Flip Flop Inputs		
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A	D_C	D_B	D_A
0	0	0	1	1	1	1	1	1
0	0	1	1	1	0	1	1	0
0	1	0	1	0	1	1	0	1
0	1	1	1	0	0	1	0	0
1	0	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1	0
1	1	0	0	0	1	0	0	1
1	1	1	0	0	0	0	0	0

~~$D_C = \bar{Q}_C \bar{Q}_B \bar{Q}_C +$~~

$D_C = Q_C$, $D_B = Q_B'$, $D_A = Q_A'$


D_A
Q_A
$\bar{Q}_A$
D_B
Q_B
$\bar{Q}_B$
D_C
Q_C
$\bar{Q}_C$
CLK