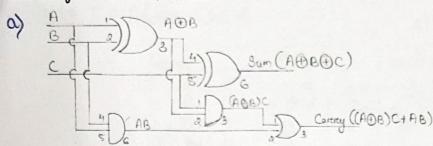
DRE-LAB ->

For Obj. 1: - Full Adder Creait

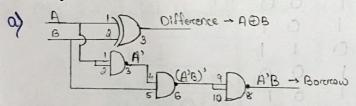


#### b) Truth table -

In	uls		Outputs	Outputs			
	В	C	Cerrorcy	Sun	4		
0	0	0	00	0		0	
0	0	1	0	11			
0	@1	0	0	10		4	
0	1	1		0		9	
1	0	0	100	9 19	0		
1	0	1	011	0		1	
1	1	0	110	0			
1		1	18010	1 1			

e 33 (11)

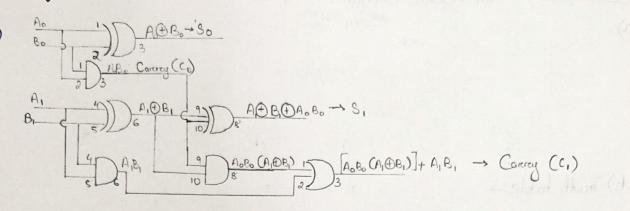
### For Obj-2-> Half-Subtractore Circuit



### b) Truth table >

	Inp	uls	Outputs Borrow Difference			
	AB		Barren	Difference		
	0	0	. 0	0		
1	0	Lata	Ala Lien	11 m		
	1	0	. 0	1 Saldano		
	1	1.	0	.00		
		01 0	Aut.			

# For Obj-3 > 2-bit Parallel Adder Circuit



I	npuls		Outputs			
A.	Ao	BI	Bo	Co	8.	8.
900000000	A00000	0 0	80 0 - 0 - 0 -	0000000	8,	
0	0	0	1	0	0	0
0	0	1	0	0	10	0
0	0	1	ló	0	11	1
0	1	1001	0	0	0	0
0		1		0	1 1	0
0			0		0	
11	0	0	0	0	1	00
1	0000	0	0-0-	-00	14	1
1	0		0	1	0	0
11	0	00011		1	0	1
	1	0	0	0	1	1
1	1	0	1	1	0-00	0
1	1	1	0	1	0	1
	1	1		1	1	0

## III) LAB >

Components Required ->

Sl. No.	Name of the Component	Specification	Quantity
1	7400 1C	Quad of input NAND Grate	10
2	7408 IC	Quad d'input AND Gerte	1
3	7432 TC	Quad 2 input OR Gate	1
4	7486 TC	Quad dinput XOR hate	1
5	Universal Trainer Kit	-	1
6	Connecting Wires	वड ८०५	As neguined

dupled slepe

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observation ->
For Obj 1-> Full Adder Circuit

I	nput		Owlow	Outputs		l Output
A	B	C	Corercy	Sum	Coverey	Sun
0	0	0	00	0	00	0
0	0	0	0	1	0	
0	-	0	0		0	1
1	0	0		0	-	0
1	0	1	1	0	1	0
1	1	0		0	1	0
1	1	1	1	1	1	1

For Obj. 2 > Half - Subtractor Circuit

Inputs		Theoretical Output		Practical Output		
A	В	вотстою	Difference	Borerow	Difference	
0	0	0	0	0	0	
0	1		1	1	ı	
1	0	0	1	0	1	
1	1	0	O	6	0	

For Obj. 3 - 2 - bit Parallel Adder Circuit

T	Input			Theoretical Output			Preac	Practical	
A,	Ao	B	Bo	Box Co	S,	80	Co	8,	80
	0	0	0	0	0	0	0	0	0
0	0	0	1	00	0	1	0	0	0
0	00	1	0	0	1	0	0	1	1
0	0	0	0	0	1	1	0	1	
0		0	1	0	0	9	0	0	0
000000000	1	1	0	0000	1	Ĭ	000	i	1
0	1	1		1	0	0	1	0	0
!!	0	0	0	0	1.	0	0	l	0
1	00	0	3	0	1	1	0	1	1
1	0		0		00	0	1	0	0
1	0	0	0	0	0		0	1	
i	1	0	1	i	0	0	i	0	0
1	1	1	0	1	00	i	i	0	i
1	1	1	1	1	1	0	1	1	0

## Conclusion ->

In this experiment, we implemented Full adder, Half Subtractor & 2-by parcalled adder circuit using basic gates i.e. 7400 IC, 7408 IC, 7432 IC & 7486 IC.

## WPRE-LAB.

(3)1) A Half-addore is chareferised by 2-inputs & 2 outputs.

- 2) A 4-bit pourable ladder can add 2.4-bit binarres numberes.
- 3) Two four bit numbers can be added using two full adders. Yes or No. Justing answer.

Ana + No, we require one half-adder & 3 - full adder to add two four bit numbers.

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