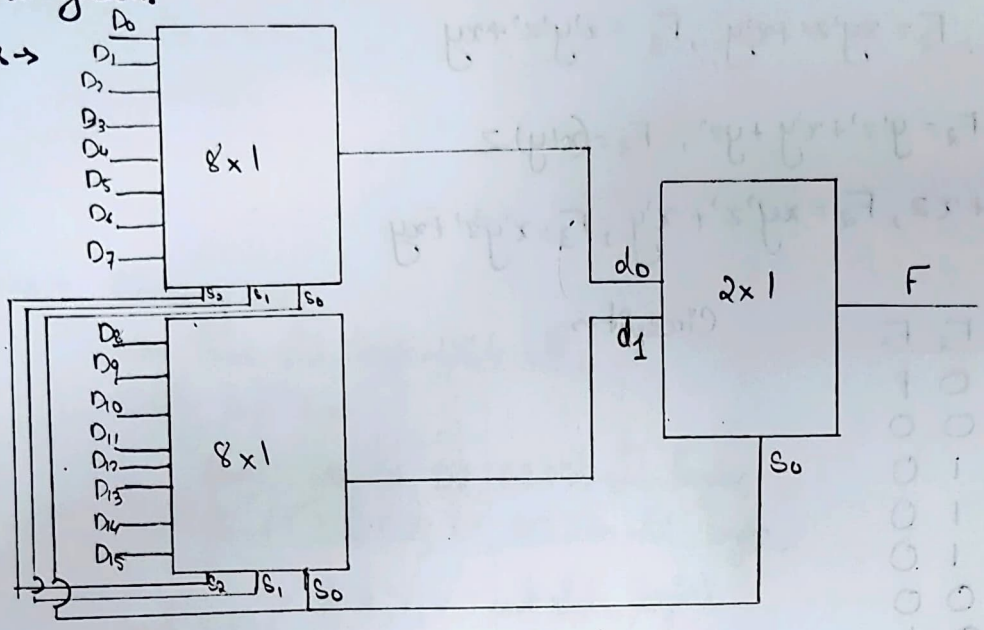
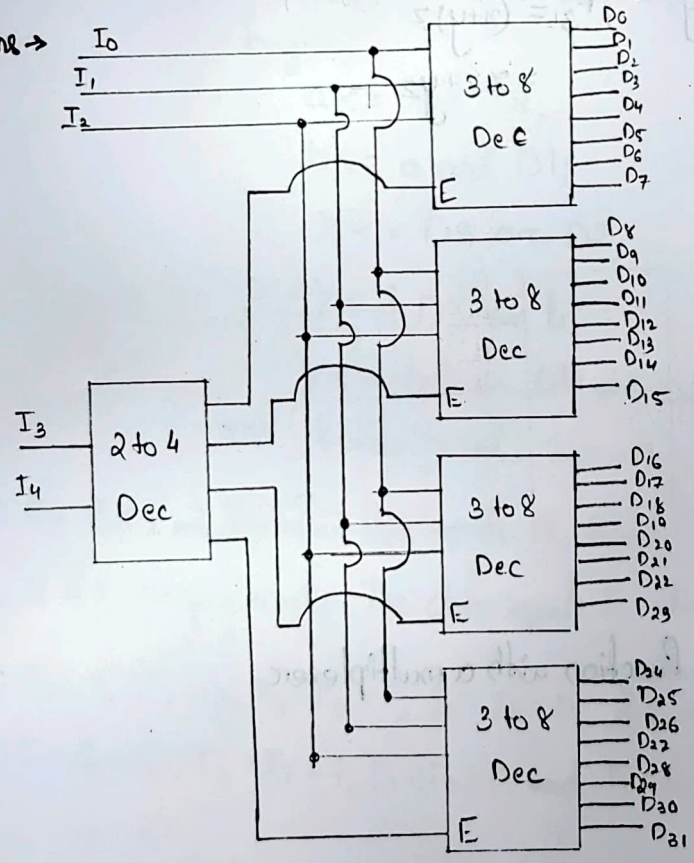
Q1) Construct a 16 x 1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams.

Ans →



Q2) Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and 2 to 4 line decoder. Use block diagrams for the components.

Ans →



Q3) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

a) $F_1 = x'yz' + xz$, $F_2 = xy'z' + x'y$, $F_3 = x'y'z' + xy$

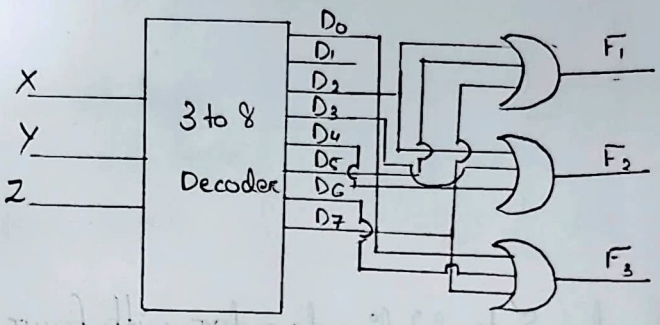
b) $F_1 = (y' + x)z$, $F_2 = y'z' + x'y + yz'$, $F_3 = (x+y)z$

Ans → a) $F_1 = x'yz' + xz$, $F_2 = xy'z' + x'y$, $F_3 = x'y'z' + xy$

Truth table →

	X	Y	Z	F_1	F_2	F_3
D_0	0	0	0	0	0	1
D_1	0	0	1	0	0	0
D_2	0	1	0	1	1	0
D_3	0	1	1	0	1	0
D_4	1	0	0	0	1	0
D_5	1	0	1	1	0	0
D_6	1	1	0	0	0	1
D_7	1	1	1	1	0	1

Circuit →



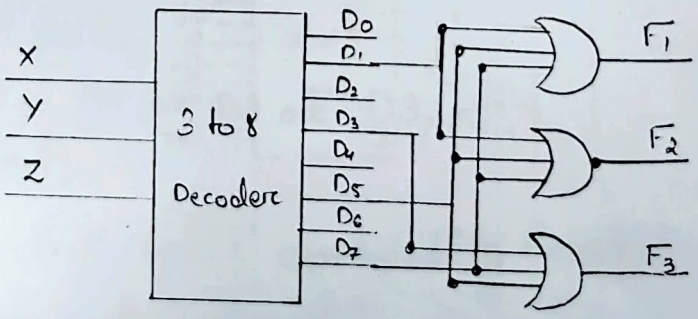
b) $F_1 = (y' + x)z$
$= y'z + xz$

$F_2 = y'z' + x'y + yz'$

$F_3 = (x+y)z$
$= xz + yz$

Truth table →

	x	y	z	F_1	F_2	F_3
D_0	0	0	0	0	1	0
D_1	0	0	1	1	0	0
D_2	0	1	0	0	1	0
D_3	0	1	1	0	1	1
D_4	1	0	0	0	1	0
D_5	1	0	1	1	0	1
D_6	1	1	0	0	1	0
D_7	1	1	1	1	0	1



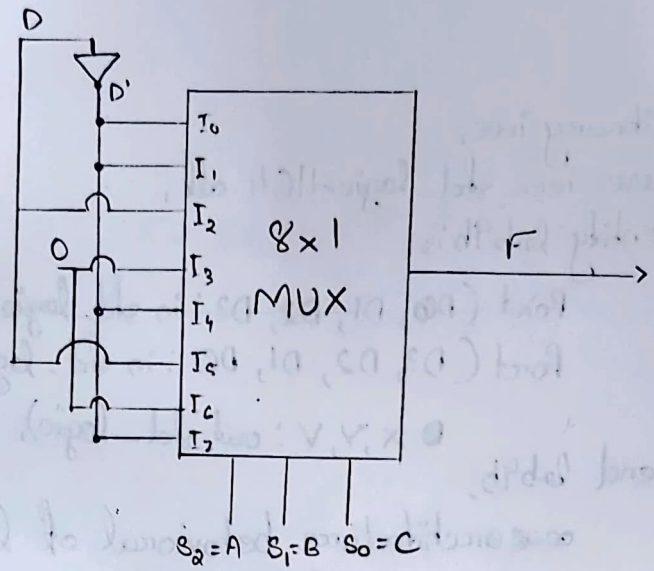
Q4) Implement the following Boolean function with a multiplexer

a) $F(A,B,C,D) = \Sigma(0,2,5,8,10,14)$

b) $F(A,B,C,D) = \Pi(2,6,11)$

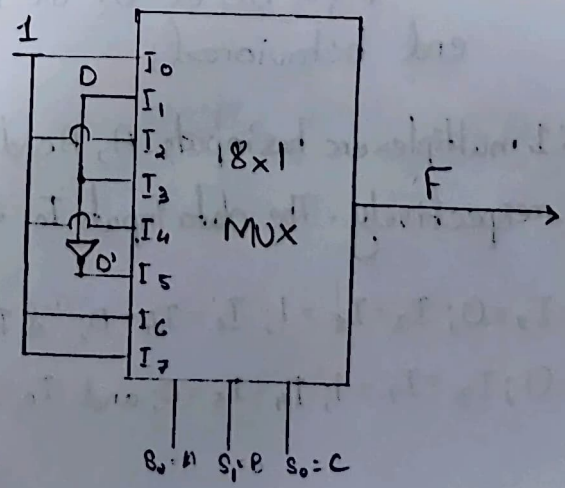
a) $F(A, B, C, D) = \Sigma(0, 2, 5, 8, 10, 14)$

A	B	C	D	F	
0	0	0	0	1	$F = D'$
0	0	0	1	0	
0	0	1	0	1	$F = D'$
0	0	1	1	0	
0	1	0	0	0	$F = D$
0	1	0	1	1	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	1	$F = D'$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	0	$F = 0$
1	1	0	1	0	
1	1	1	0	1	$F = D'$
1	1	1	1	0	

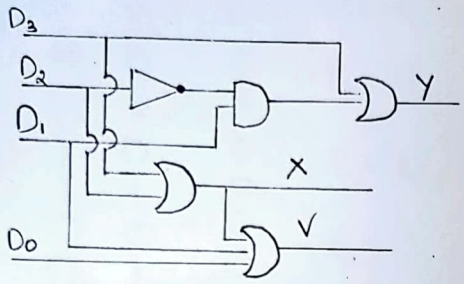


b) $F(A, B, C, D) = \Pi(2, 6, 11)$

A	B	C	D	F	
0	0	0	0	1	$F = 1$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = 1$
0	1	0	1	1	
0	1	1	0	0	$F = D$
0	1	1	1	1	
1	0	0	0	1	$F = 1$
1	0	0	1	1	
1	0	1	0	1	$F = D'$
1	0	1	1	0	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	



Q5) Write the HDL description of 4 bit priority encoder circuit given below.



Ans →

```
Library ieee;
use ieee.std_logic_1164.all;
entity lab9b is
    Port (D3, D2, D1, D0 : in std_logic;
          X, Y, V : out std_logic);
end lab9b;
    architecture behavioral of lab9 is
        signal a, b : std_logic;
    begin
        a <= not D2;
        b <= a and D1;
        X <= D3 or D2;
        Y <= D3 or b;
        V <= D0 or D1 or D2 or D3;
    end behavioral;
```

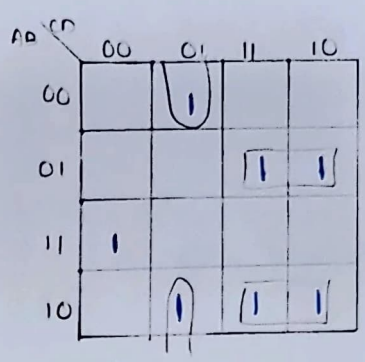
Q6) An 8×1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1 & S_0 respectively. The data inputs I_0 through I_7 are as follows –

a) $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; & $I_6 = D'$

b) $I_1 = I_2 = 0$; $I_3 = I_7 = 1$; $I_4 = I_5 = D$; and $I_0 = I_6 = D'$.

Ans → a) $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; $I_6 = D'$.

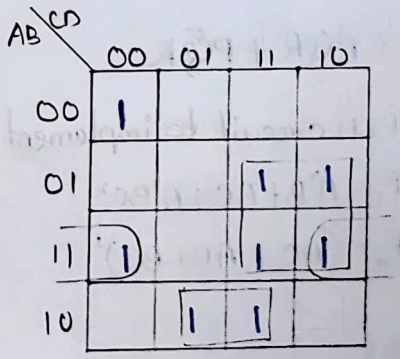
A	B	C	D	F	
0	0	0	0	0	$I_0 = D$
0	0	0	1	1	
0	0	1	0	0	$I_1 = 0$
0	0	1	1	0	
0	1	0	0	0	$I_2 = 0$
0	1	0	1	0	
0	1	1	0	1	$I_3 = 1$
0	1	1	1	1	
1	0	0	0	0	$I_4 = D$
1	0	0	1	1	
1	0	1	0	1	$I_5 = 1$
1	0	1	1	1	
1	1	0	0	1	$I_6 = D'$
1	1	0	1	0	
1	1	1	0	0	$I_7 = 0$
1	1	1	1	0	



$F = ABC'D' + B'C'D + A'BC + AB'C$

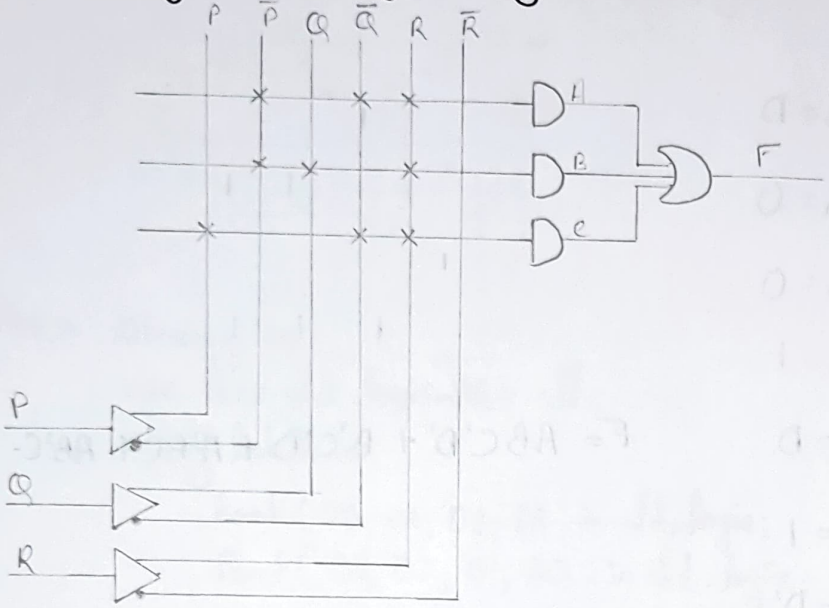
b) $I_1 = I_2 = 0$; $I_3 = I_7 = 1$; $I_4 = I_5 = D$; and $I_0 = I_6 = D'$.

A	B	C	D	F	
0	0	0	0	1	$I_0 = D'$
0	0	0	1	0	
0	0	1	0	0	$I_1 = 0$
0	0	1	1	0	
0	1	0	0	0	$I_2 = 0$
0	1	0	1	0	
0	1	1	0	1	$I_3 = 1$
0	1	1	1	1	
1	0	0	0	0	$I_4 = D$
1	0	0	1	1	
1	0	1	0	0	$I_5 = D$
1	0	1	1	1	
1	1	0	0	1	$I_6 = D'$
1	1	0	1	0	
1	1	1	0	1	$I_7 = 1$
1	1	1	1	1	



$F = A'B'C'D' + ABD' + AB'D + BC$

Q7) A programmable logic array (PLA) is shown in the figure



Ans→ From the above fig.,

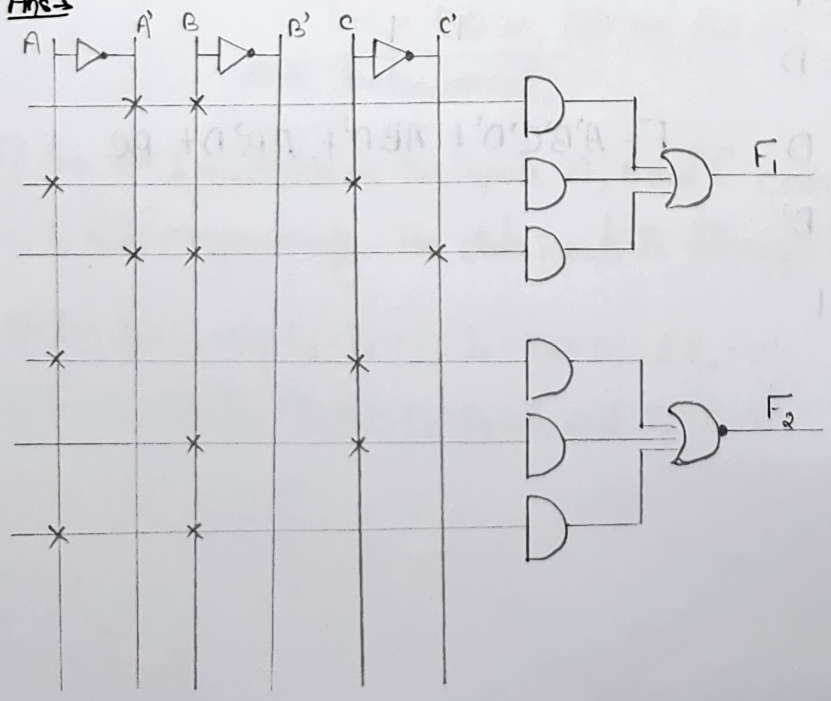
$$A = \bar{P}\bar{Q}R,\ B = \bar{P}Q\cdot R,\ C = P\bar{Q}R$$

$$F = A+B+C$$
$$= \bar{P}\bar{Q}R + \bar{P}QR + P\bar{Q}R$$

Q)8') Draw a PLA circuit to implement the functions

$$F_1 = A'B + AC + A'BC'$$
$$F_2 = (AC + AB + BC)'$$

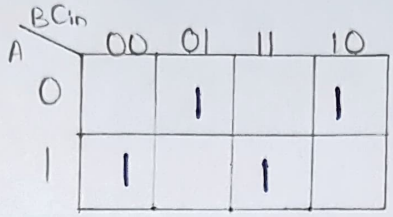
Ans→



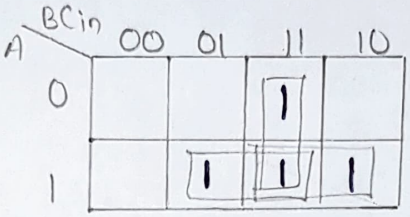
Q>9) Implement full adder using PAL.

Ans →

A	B	C_{in}	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$S = A'B'C_{in} + A'BC_{in}' + AB'C_{in}' + ABC_{in}$



$C = BC_{in} + AC_{in} + AB$