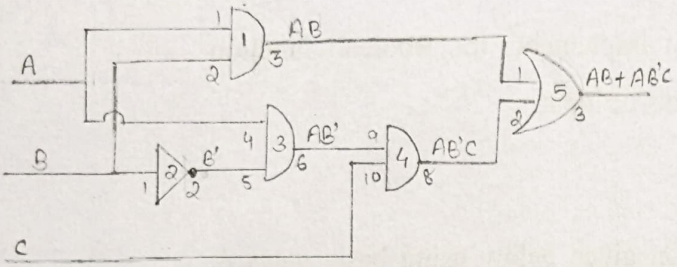
PRE-LAB

1) For Obj. 1 →

$$F = (A, B, C) = AB + AB'C$$

a) Circuit Diagram →



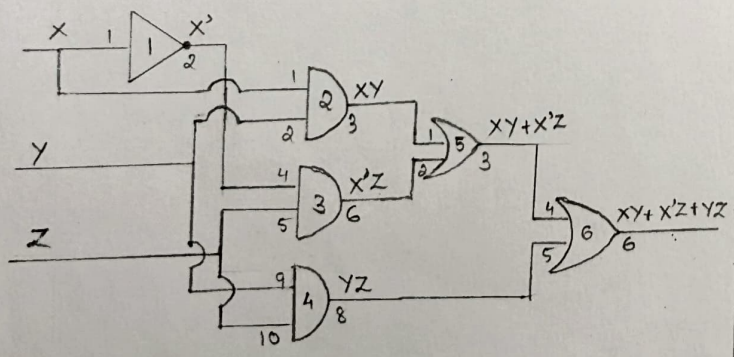
b) Truth tables →

Inputs			Outputs			
A	B	C	B'	AB	AB'C	F= AB+AB'C
0	0	0	1	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	1	0	1	1
1	1	0	0	1	0	1
1	1	1	0	1	0	1

2) For Obj. 2 →

$$F(X, Y, Z) = XY + X'Z + YZ$$

a) Circuit Diagram →



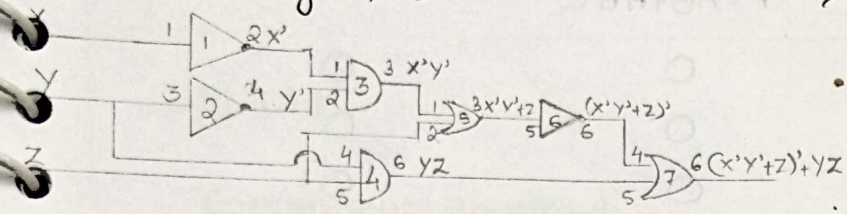
b) Truth Tables →

Inputs			Outputs				
X	Y	Z	x'	XY	X'Z	YZ	F=XY+X'Z+YZ
0	0	0	1	0	0	0	0
0	0	1	1	0	1	0	1
0	1	0	1	0	0	0	0
0	1	1	1	0	1	1	1
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	1	0	0	1
1	1	1	0	1	0	1	1

3) For Obj. 3 →

$F(x, y, z) = (x'y'+z)' + yz$

a) Circuit Diagram →



b) Truth tables →

Inputs			Outputs			
X	Y	Z	X'Y'	YZ	(X'Y'+Z)'	F=(X'Y'+Z)'+YZ
0	0	0	1	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	1	0	1	0	1
1	0	0	0	0	1	1
1	0	1	0	0	0	0
1	1	0	0	0	1	1
1	1	1	0	0	1	1

III) LAB:

Components Required →

Sl. No.	Name of the Component	Specification	Quantity
1	7404 IC	Hex Inverter	1
2	7408 IC	Quad 2 input AND gate	1
3	7432 IC	Quad 2 input OR gate	1
4	Universal Trainer Kit	—	1
5	Connecting Wires	23 SWG	As required

Observation →

⇒ $F(X, Y, Z) = (XY'+Z)' + YZ$

Inputs			Theoritical Output				Practical Output
X	Y	Z	X'Y'	YZ	(X'Y'+Z)'	F=(X'Y'+Z)'+YZ	
0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	1	1
0	1	1	0	1	0	1	1
1	0	0	0	0	1	1	1
1	0	1	0	0	0	0	0
1	1	0	0	0	1	1	1
1	1	1	0	1	1	1	1

a) $F(A, B, C) = AB + AB'C$

Inputs			Theoritical Outputs				Practical Outputs
A	B	C	B'	AB	AB'C	F=AB+AB'C	
0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	1	0	1	1	1
1	1	0	0	1	0	1	1
1	1	1	0	1	0	1	1

b) $F(X, Y, Z) = XY + X'Z + YZ$

Inputs			Theoritical Outputs				Practical Outputs
X	Y	Z	X'	XY	X'Z	YZ	F=XY+X'Z+YZ	
0	0	0	1	0	0	0	0	0
0	0	1	1	0	1	0	1	1
0	1	0	1	0	0	0	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
1	1	0	0	1	0	0	1	1
1	1	1	0	1	0	1	1	1

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

Observation:

Conclusion:

In this experiment implementing Boolean functions using logic gates. Some basics of the logic gates (AND, OR, NOT) in sum of product representation of equation and their implementation using logic gates & also implementation of Boolean expression using Universal gates (NAND or NOR.).

IV. POST LAB:

1. Prove the following equation using truth table:

   (X+Y)(X'+Z)=XZ+X'Y

2. Draw a gate circuit which has an output Z = [BC'+F (E+AD')] '

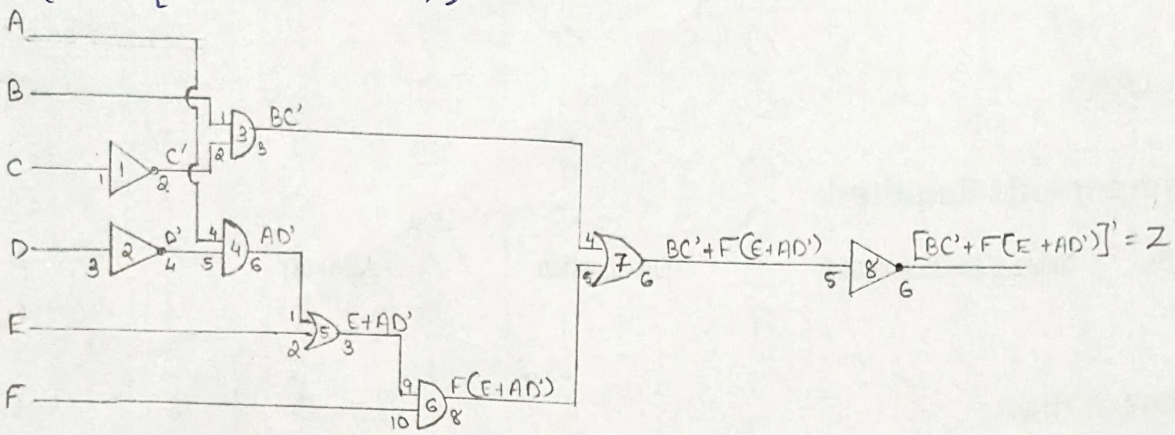
3. Write truth table for the function F=A (B+C') +1

Ans→

1) (X+Y)(X'+Z) = XZ + X'Y

Inputs			Outputs						
X	Y	Z	X'	XZ	X'Y	X+Y	X'Z	(X+Y)(X'+Z)	(XZ+X'Y)
0	0	0	1	0	0	0	1	0	0
0	0	1	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1
1	0	0	0	0	0	1	0	0	0
1	0	1	0	1	0	1	1	1	1
1	1	0	0	0	0	1	0	0	0
1	1	1	0	1	0	1	1	1	1

2) $Z = [BC' + F(E + AD')]'$



3) $F = A(B + C') + 1$

Inputs			Outputs			
A	B	C	C'	B + C'	A(B+C')	F = A(B+C') + 1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
1	0	0	1	1	1	1
1	0	1	0	0	0	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1