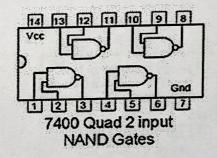
I. OBJECTIVE:

- 1. Investigation of the logic behaviour of various gates:
 - a) 7400 quadruple two-input NAND gates
 - b) 7402 quadruple two-input NOR gates
 - c) 7404 hex inverters
 - d) 7408 quadruple two-input AND gates
 - e) 7432 quadruple two-input OR gates
 - 1) 7486 quadruple two-input XOR gates
- 2. Using a single 7400 IC, connect a circuit that produces
 - a) An inverter.
 - b) A two-input AND.
 - c) A two-input OR.
 - d) A two-input XOR.

II. PRE-LAB

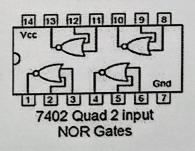
Quad 2-input NAND gate

A	В	F= A.B
0	0	
0	1	
1	0	
	1	0



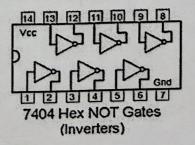
2. Quad 2-input NOR gate

A	В	F= AtB
0	0	
0	e la laca	0
1	0	0
1	1	0



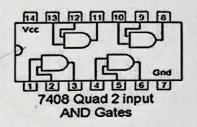
Hex Inverter

A	F= 7
0	
1	0



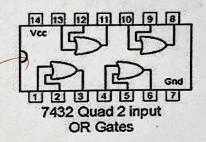
4. Quad 2-input AND gate

A	В	F= A.B
0	0	0
0	1	0
1	0	0
1	0	



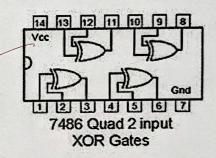
5. Quad 2-input OR gate

A	В	F= A+B	
0	0	0	
0	10		
1	0		
1	1	1	



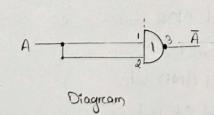
6. Quad 2-input EX-OR gate

Α	В	F= AB+AB	
0	0	0	
0	123		
1 49	0	AND THE PARTY OF T	
1	1	0	



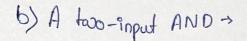
7. Draw the circuit diagram & obtain truth tables for obj. 2

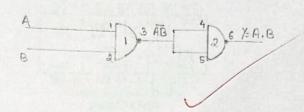
a) An invertere ->



	Inputs	Outpute F=(AB) = A
A	A=B	F=(AB) = A
0	0	
1	1	0

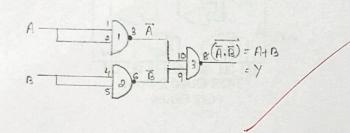
Page:





h table	8 >		
	Tout	puts	
В	A.B	A.B	Y= A.B = A.B
0	0		0
1	0		0
0	0	01	0
1	1	0	
	B	B A.B O O	buts Outputs B A.B A.B O O I I O I

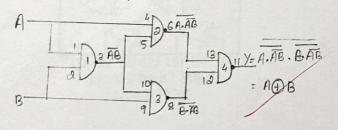
C) A two-input OR >



It Truth tables->

Inputs		n puts Outputs B A B A B A B A B = A+Y=				
A	B	Ā	B	A.B	A.B = A+ Y = Y	
0	0	1	1	1	0	
0		1	0	0	1	
1	0	0	1	0	1	
1	1	0	0	6	1	

d) A two-input XOR->



Treath Tables ->

	Int	outs		Outpu	Js	
-	A	B	AB	Output AAB	B.AB	Y=A.AB.B.AB
	0	0	1	1		0
-	0		1		D	
-	1	0	1	0	61	1
	9 1	1	0	1)	0

II > LAB-

Components Required >>

مرا هران کاران	· cops.
sl. No.	Name of the Component
1	7400 IC
2	7402 IC
3	7404 IC
4	7408 IC
5	7432 IC
6	7486 IC
7	Univerceal Trainera
8	Canachine Were

Specification Quantity Quad & input NAND Gete 1 Quad & input NOR Gete 1

Quad d'input NOR Grete 1

Hex Invertere 1

Quad d'input AND Grete 1

Quad d'input OR Grete 1

Couad d'input XOR grete 1

23 swg Asra

As required

Objective-1 LG No. Output Pins Grate No. Input Pins Remark 7402 Working 1 2,3 (NOR) Working 5,6 4 3 Working 8,9 10 4 Working 13 11,12 7400 CNANO) 1,2 3 Working 4,5 6 Working 10,9 Working 8 13,12 Working 37404 2 Working 2 3 Hex NOT 4 Working 3 5 6 Working 9 8 Working -3 1,2 3 Working 37408 a 4,5 6 - AND Working 3 9,10 8 Working 9 13,12. 11 Working 1,2 3 Working **3**7432 6 45 Working OR Working 9,10 Working 13,12 11 **3**7486 1,2 Worling 4,5 6 Working 2 XOR 9,10 8 Working 13, 12 Working 11

Objective - II

IC No.	Gate No.	Input Pine	Output	Pine Remarch
Inverter using	84.1	2	3	Working
7400 IC	0,2	5	G	Working
	3	12	10	Worling
		100	13	Worling
A two input AND	1	1,2	G	Worling
using 7400 IC	2	8,9	13	Working
A two input OR using 7400 IC	8 1 P	1,4 &	8	Working
A two input xor using 7400 IC	8	ارگ هرا	n	Worling

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III. <u>LAB:</u>

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V

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3

3

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3

3

9

Components Required:

S. No Name of the Component

Specification

Quantity

Observation:

Conclusion:

1) In Obj. 1, we verified the functioning of vourious logic gates.

2) In Obj. 2, we conclude that NAMD gete is a universal gate because we are able to IV. POSTLAB to connect & implement on Inverter, AND, OR and XOR gate with single 7400 IC Gate.

1. What is the voltage range for operation of digital circuits? 2. What is the significance of ground and $V_{\text{\tiny CC}}$ connection?

3. Which gates are known as universal gates & why?

4. What is the minimum number of NAND gates used to realize an EX-OR gate?

Ans > 1) Acceptable input signal voltages range from OV to 0.8 Vo forcalow logic State, & 2 volte to 5 V for a high logic gates state.

2) VCC (Voltage Common Collectore) is the higher voltage with respect to GND Cyround). VCC is the power in put of a device. It may be the or -on-ve with respect to GND. When theonly the power supply is used then VSS means ground or Zero.

3) Auniversal gater is a gate which can implement any Boolean function without need to use any other gates. The NAND or NOR gates are universal gates.

4) An XOR gate circuit can be made from 4 NAND gates.