Q1) List and briefly define the main structural components of a single processor computer?

Ans → The four main structural components of a single processor computer are →

a) CPU: That partition of a computer that patches and executes instruction.

b) Main-memory: A main memory which stores both data and instruction.

c) I/O System: This is the system which relates the input-output of the computer.

d) System bus: Some mechanism that provide for communication among CPU, main-memory & I/O.

Q2) Differentiate between

i) Microprocessor and Microcontroller

ii) Computer Organisation and Computer Architecture

iii) Embedded System and deeply Embedded System

Ans → a)

Micro Processor	Micro Controller
i) It is heart of computer system.	i) It is heart of embedded system.
ii) Cost of entire system in more.	ii) Cost of entire system in low.
iii) Cannot be used in compact system.	iii) Can be used in compact system.
iv) Do not have power saving feature.	iv) have power saving feature.
v) It have less no. of register, hence more operation are memory based.	v) It have more no. of register, hence the program are easier to write.
vi) Since memory and I/O are connected externally the circuit becomes larger.	vi) Since components are connected internally, most operation are internal instruction, hence speed is fast.
vii) Since memory & I/O components are all external each instruction will need external operation hence it is relative power.	viii) Since memory and I/O are present internally the circuit is small.
viii) Used in PC, laptop, etc.	viii) Used in AC, washing machine, etc.

b)

Computer Organisation	Computer Architecture
i) It refers to the operational units and their interconnections that realise the architectural specification.	i) It refers to those attributes of a system that is visible to the program or those attributes that have a direct impact on the logical execution of a program.
ii) It is decided after the architecture is fixed.	ii) It is always decided first.

iii) Organizational attributes includes those hardware details that are transparent to the programmer such as control signals, interface between the computers and the memory technology used.

iv) For e.g. → It is an architectural issue whether the computer will behaving as multiplying instruction.

iii) Architectural attributes includes in instruction sets, the no. of bits used to represent different data types, I/O mechanism & techniques for addressing memory.

iv) For e.g. → It is an organisational issue now to implement that multiplication instruction can be used directly multiplication or repetative addition method.

c)

Embedded System	Deeply Embedded System
i) These are dedicated to fixed function.	i) These are dedicated for single purpose.
ii) Don't have wireless capability.	ii) They have wireless capability and appear in network configaration.
iii) Require large memory time and power consumption.	iii) They have extreme resource control in term of memory, processor size & power consumption.

Q3) List and explain the cloud computing service?

Ans → The 3 types of cloud computing services →

i) Saas → Provides service to customer in the form of software specifically app. running on & accessible in the cloud.

ii) Paas → Provides service to customer in the form of a platform on which the customers application can run.

iii) Iaas → The customer has access to the underlying cloud infrastructure provides.

Q4) Briefly explain the different techniques used to increase the microprocessor speed?

Sol → i) Higher clock frequencies → Increasing the clock speed of the microprocessor allow it to perform more instructions per second.

ii) Multiple Core → Integrating multiple processing cores on to a single microprocessor chip enables parallel processing of instruction.

iii) Instruction Chip → Breakdown the execution of instruction into multiple stage allowing multiple instruction to be processed simoultaneously.

(Q8) Consider two different machine with an instruction set of 100000 instruction both of which have a clock rate of 400MHz.

Instruction Type →	Arithmetic & Logic	Data Transfer	Control Transfer	Others
Instruction mix (%).				
Machine A	50	15	15	20
Machine B	65	15	10	10
Cycles Per Instruction →				
Machine A	2	3	4	2
Machine B	1	4	3	2

Sol? → Machine 1 →

$$CPI = \frac{(2\times 0.5)+(3\times 0.15)+(4\times 0.15)+(2\times 0.2)}{1}$$

$$= \frac{1+0.45+0.6+0.4}{1} = 2.45$$

$$MIPS = \frac{400}{2.45\times 10^6} = 0.00163$$

$$T = Ic \times CPI \times Z$$

$$= \frac{100000\times 2.45}{400\times 10^6} = 0.0006125 \text{ sec}$$

Machine 2 →

$$CPI = \frac{(1\times 0.65)+(4\times 0.15)+(3\times 0.1)+(2\times 0.1)}{1}$$

$$= 0.65+0.6+0.3+0.2$$

$$= 1.75$$

$$MIPS = \frac{400}{1.75\times 10^6} = 0.000228$$

$$T = \frac{10^6\times 1.75}{400\times 10^6} = 0.0004375 \text{ secs.}$$

Q6) A doctor in a hospital observes that an average 6 patients per hour. If there are typically 3 patients in the hospital. Determine the average of time each patient spends in the hospital?

Soln → $L = 3, \lambda = 6$

$$W = \frac{L}{\lambda} = \frac{3}{6} = \frac{1}{2} = 30 \text{ mins.}$$

Q7) Determine the fraction of the execution time in values code that is parallel to achieve an overal speed up 2.25. Assume 15 no. of processors.

Ans → Overall speed = 2.25

$$\text{Speed up} = \frac{1}{(1-f) + \left(\frac{f}{suf}\right)}$$

$$\Rightarrow 2.25 = \frac{1}{(1-f) + \frac{f}{15}}$$

$$\Rightarrow 2.25 = \frac{1}{\frac{15 - 15p + p}{15}}$$

$$\Rightarrow 2.25 = \frac{15}{15 - 14p}$$

$$\Rightarrow 15 - 14p = \frac{15}{2.25}$$

$$\Rightarrow 15 - 14p = 6.75$$

$$\Rightarrow 14p = 15 - 6.75$$

$$\Rightarrow p = \frac{8.24}{14}$$

$$= 0.588.$$

Q8) Two benchmark programs are executed on three computer with following

	Computer A	Computer B	Computer C
Program 1	50	20	10
Program 2	100	200	40

Ans →

	Computer A	Computer B	Computer C
Program 1	0.2	0.5	1
Program 2	0.1	0.05	0.25
A.M	0.15 (3rd)	0.275 (2nd)	0.625 (1st)
H.M	0.133 (2nd)	0.09 (3rd)	0.4 (1st)

Q9) Let a program has 40% of its code enhanced to run 2-3 times faster. Determine the overall speed up of the system.

Ans→ $\text{Speed up} = \frac{1}{(1-f)+\left(\frac{f}{\text{Suf}}\right)} = \frac{1}{(1-0.4)+\frac{0.4}{2.3}}$

$= \frac{1}{0.6+0.1789}$

$= \frac{1}{0.7739} \approx 1.2913$

Q10) Explain different addressing modes of 8086 microprocessor with suitable examples.

Ans→ Different addressing modes are as follows→

i) Immediate Addressing Mode → Operand is a part of the instruction itself

Eg→ Mov Ax, 0005H, ADD Ax, 1234H

ii) Register Addressing Modes → Register in the source of an operand for an instruction

Eg→ Mov Bx, Ax

iii) Direct Addressing Modes → The Effective address of the memory location is written directly.

Eg→ Mov, ax [5000h]

iv) Register Indirect Addressing → The operand memory address is contained in a register.

Eg→ Mov ax, [bx]

v) Indexed Addressing Mode → An index register is added to a base address to calculate the effective address of the operand.

e.g.→ mov ax, [si + 10h]

vi) Base- Relative Addressing Mode → The operand memory address is calculated by adding an offset to a base address stored in a register.

e.g.→ mov ax, [bx + 20h]

Q11) Explain the register organisation of 8086 microprocessor with suitable example.

Ans→ i) General purpose registers → 16 bits sized Ax, Bx, Cx, Dx - Registers

eg→ Mov ax, [1667h]

add ax, bx

ii) Index Registers → Two index registers are source index(SI) & destination index.

e.g. → mov Si, offset

iii) Base & stack pointers → Includes two important pointers : Base pointer (BP) & Stack Pointer (SP)

e.g.→ mov BP, 8000h, mov SP, 8000h

iv) Instruction pointer → Includes the IP (Instruction pointer) register which stores the offset address of the next instruction to be executed.

e.g.→ JMP label_name

v) Segment Registers → It has 4 register i.e. code segment (CS), data segment (DS), stack segment (SS), extra segment (ES);

e.g.→ mov ax, 1234h
mov dS, ax

Q12) a) Write an assembly language program to multiply 40h with 8h using logical instruction of 8086 microprocessor only.

Ans→
```
mov al, 40h
mov bl, 8H
mul bx
```

b) code → Determine the output & its memory location.

Ans→
```
mov ax, 23FOH     → 23FOH coded in ax
mov bx, ax        → value of ax stored in bx
mov [bx] ax       → value of ax stored in the memory location
mov cx, 503FH     → 503fh in cx
mov ax, cx        → copy of cx, stored in ax
sub ax, [bx]      → subtract the value stored in the memory location whose addis saved in
                    Bx from ax.
inc bx
inc bx            → increment bx twice
mov[bx], ax       → store the value of ax into the memory location
hlt               → execution whose address is continued in bx
                    execution halted
```

The final value is (2F4Fh), the value in ax (2F4Fh) is stored all the memory location printed to by bx.