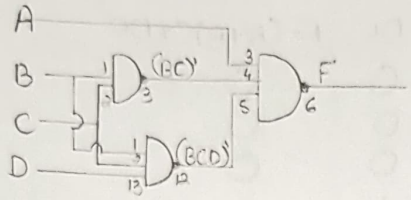
PRE-LAB →

For Obj. 1 → $F = A' + BC + BCD$

a)

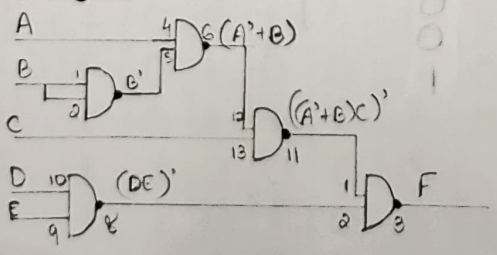


b)

Inputs				Outputs			
A	B	C	D	A'	BC	BCD	F = A' + BC + BCD
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1
0	0	1	0	1	0	0	1
0	0	1	1	1	0	0	1
0	1	0	0	1	0	0	1
0	1	0	1	1	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	0	1	0	1
1	1	1	1	0	1	1	1

For Obj-2 → $F = (A' + B)C + DE$

a)

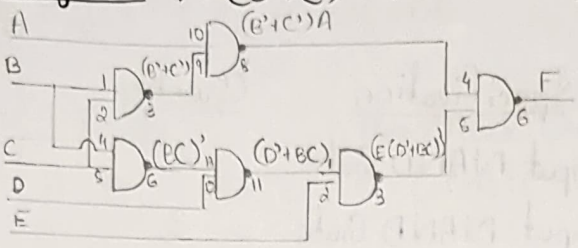


b)

Inputs					Outputs				
A	B	C	D	E	A'	A'+B	(A'+B)C	DE	F = (A'+B)C+DE
0	0	0	0	0	1	1	0	0	0
0	0	0	0	1	1	1	0	0	0
0	0	0	1	0	1	1	0	0	0
0	0	0	1	1	1	1	0	1	1
0	0	1	0	0	1	1	1	0	1
0	0	1	0	1	1	1	1	0	1
0	0	1	1	0	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	0	0	0
0	1	0	0	1	1	1	0	0	0
0	1	0	1	0	1	1	0	0	0
0	1	0	1	1	1	1	0	1	1
0	1	1	0	0	1	1	1	0	1
0	1	1	0	1	1	1	1	0	1
0	1	1	1	0	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	0	1	1	0	0	0	1	1
1	0	1	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0
1	0	1	1	1	0	0	0	1	1
1	1	0	0	0	0	1	0	0	0
1	1	0	0	1	0	1	0	0	0
1	1	0	1	0	0	1	0	0	0
1	1	0	1	1	0	1	0	1	1
1	1	1	0	0	0	1	1	0	1
1	1	1	0	1	0	1	1	0	1
1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	0	1	1	1	1

For Obj. 3 → $F = (B'+C')A + E(D'+BC)$

a)



Inputs					Outputs								
A	B	C	D	E	B'	C'	D'	BC	B'+C'	D'+BC	(B'+C')A	E(D'+BC)	F
0	0	0	0	0	1	1	1	0	1	1	0	0	0
0	0	0	0	1	1	1	1	0	1	1	0	1	1
0	0	0	1	0	1	1	0	0	1	0	0	0	0
0	0	0	1	1	1	1	0	0	1	0	0	1	1
0	0	1	0	0	1	0	1	0	1	1	0	0	0
0	0	1	0	1	1	0	1	0	1	1	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0	0	0
0	0	1	1	1	1	0	0	0	1	0	0	1	1
0	1	0	0	0	0	1	1	0	1	1	0	0	0
0	1	0	0	1	0	1	1	0	1	1	0	1	1
0	1	0	1	0	0	1	0	0	1	0	0	0	0
0	1	0	1	1	0	1	0	0	1	0	0	1	1
0	1	1	0	0	0	1	1	1	1	1	0	0	0
0	1	1	0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	0	0	1	0	1	1	0	0	0	0
0	1	1	1	1	0	1	0	1	1	0	0	1	1
1	0	0	0	0	1	1	1	0	1	1	1	0	1
1	0	0	0	1	1	1	1	0	1	1	1	1	1
1	0	0	1	0	1	1	0	0	1	0	1	0	1
1	0	0	1	1	1	1	0	0	1	0	1	1	1
1	0	1	0	0	1	0	1	0	1	1	1	0	1
1	0	1	0	1	1	0	1	0	1	1	1	1	1
1	0	1	1	0	1	0	0	0	1	0	1	0	1
1	0	1	1	1	1	0	0	0	1	0	1	1	1
1	1	0	0	0	0	1	1	0	1	1	1	0	1
1	1	0	0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	0	0	1	0	0	1	0	1	0	1
1	1	0	1	1	0	1	0	0	1	0	1	1	1
1	1	1	0	0	0	0	1	1	0	1	0	0	0
1	1	1	0	1	0	0	1	1	0	1	0	1	1
1	1	1	1	0	0	0	0	1	0	1	0	0	0
1	1	1	1	1	0	0	0	1	0	1	0	1	1

III) LAB →

Components Required →

Sl. No.	Name of the Components	Specification	Quantity
1	7400 IC	2 input NAND Gate	2
2	7410 IC	3 input NAND Gate	3
3	Universal Trainer Kit	—	1
4	Connecting Wires	23 SWG	As required

Observation →

For Obj. 1 → $F = A' + BC + BCD$

Inputs				Theoritical Output	Practical Outputs
A	B	C	D	$F = A' + BC + BCD$	
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

For Obj.2 → $F = (A'+B)C+DE$

Inputs					Theoritical Outputs	Practical Outputs
A	B	C	D	E	$F = (A'+B)C+DE$	
0	0	0	0	0	0	0
0	0	0	0	1	0	0
0	0	0	1	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	0	1	1	1
0	0	1	1	0	1	1
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	1	0	0
0	1	0	1	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	1	1
0	1	1	0	1	1	1
0	1	1	1	0	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	1	0	0
1	0	0	1	0	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	1
1	0	1	0	1	1	1
1	0	1	1	0	1	1
1	0	1	1	1	1	1
1	1	0	0	0	0	0
1	1	0	0	1	0	0
1	1	0	1	0	0	0
1	1	0	1	1	0	0
1	1	1	0	0	1	1
1	1	1	0	1	1	1
1	1	1	1	0	1	1
1	1	1	1	1	1	1

For Obj. 3 → $F=(B'+C')A+E(D'+BC)$

Inputs					Theoritical Output	Practical Output
A	B	C	D	E	$F=(B'+C')A+E(D'+BC)$	
0	0	0	0	0	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	0	1	0	0
0	0	1	1	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	0
0	1	0	0	1	0	0
0	1	0	1	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	0	0
0	1	1	0	1	0	0
0	1	1	1	0	0	0
0	1	1	1	1	0	0
1	0	0	0	0	1	1
1	0	0	0	1	1	1
1	0	0	1	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	1	1
1	0	1	0	1	1	1
1	0	1	1	0	1	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	0	1	1	1	1
1	1	1	0	0	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	0
1	1	1	1	1	1	1

Conclusion →

This experiment implements Boolean functions using logic gates. Some basics of logic gates (NAND) in sum of product representation of equations & their implementation using logic gate and 7410 IC, 3 input NAND gate is also used.

I. OBJECTIVE:

1. Implement the Boolean function given below using two-level NAND-gate circuit.
   $F = A' + BC + BCD$

2. Implement the following Boolean function using two-input NAND-gates
   $F = (A' + B)\,C + DE$

3. Consider the Boolean function given below:
   $F = (B' + C')\,A + E\,(D' + BC)$
   Implement the function using minimum number of NAND gates.

II. PRE-LAB

For Obj. 1:

a. Draw the circuit diagram for the function F.
b. Obtain the truth table for all input combinations.

For Obj. 2:

a. Draw the circuit diagram for the function F.
b. Obtain the truth table for all input combinations

For Obj. 3:

a. Draw the circuit diagram for the function F.
b. Obtain the truth table for all input combinations

III. LAB:

Components Required:

S. No	Name of the Component	Specification	Quantity

Observation:

Conclusion:

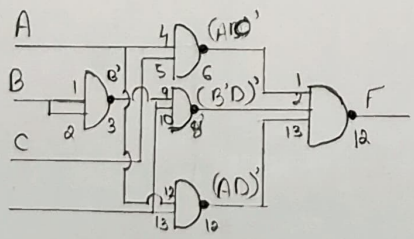
IV. POST LAB:

1. Draw a circuit for the following Boolean function using NAND-gates
   F=AC+AD+B′D

2. Simplify the following Boolean expression and Draw the circuit using NAND gates.
   F= BC′D′ + ABC′ + AC′D + AB′D + A′BD′.

Ans

1) $F = AC + AD + B'D$



2) $F = BC'D' + ABC' + AC'D + AB'D + A'BD'$

$= BC'D'(A+A') + ABC'(D+D') + AC'D(B+B') + AB'D(C+C') + A'BD'(C+C')$

$= ABC'D' + A'BC'D' + ABC'D + ABC'D' + ABC'D + AB'C'D + AB'CD + ABC'D + A'BCD + A'BCD'$

$= ABC'D' + A'BC'D' + ABC'D + AB'C'D + AB'CD + A'BCD'$

$= ABC'(D+D') + A'BD'(C+C') + AB'D(C+C')$

$= ABC' + A'BD' + AB'D$

$= [(ABC' + A'BD' + AB'D)']'$

$= [(ABC')' \cdot (A'BD')' \cdot (AB'D)']' = F_1$