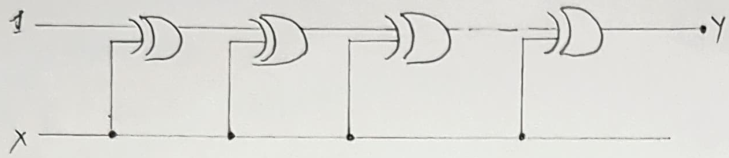
Q1) If the input to the digital circuit of the below figure consisting of a cascade of 20 XOR gates is X, then what is the output Y?

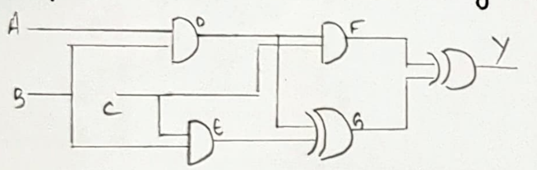


X	Y	O
0	0	0
0	1	1
1	0	1
1	1	0

Ans → When one of the input to an XOR gate is 1, the output is simply the inverted value of the other input. Output of 1st XOR gate will be → $1 \oplus X = \bar{X}$. Then, 2nd output → $\bar{X} \oplus X = 1$

~~Thus~~ ∴ For 20 such gates, the output of Y will be 1.

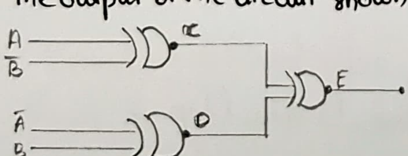
Q2) The output of the combinational circuit given below is



Ans → ~~AB~~ $D = AB$, $E = CB$, $F = DC$, $G = D \oplus E$, $Y = F \oplus G$

$$Y = F \oplus G$$
$$= DC \oplus (D \oplus E)$$
$$= ABC \oplus (AB \oplus CB)$$
$$= ABC \oplus (AB\overline{CB} + \overline{AB}CB)$$
$$= ABC \oplus (AB\bar{C} + \bar{A}BC)$$
$$= ABC\,\overline{(AB\bar{C} + \bar{A}BC)} + \overline{ABC}\,(AB\bar{C} + \bar{A}BC)$$
$$= B(A+C)$$

Q3) The output of the circuit shown in fig. is equal to



Ans → $C = \cancel{A\bar{B}\odot}\; A \odot \bar{B}$, $D = \overline{\bar{A}B} + \bar{A}B$, $\cancel{F = C \odot F}$

$$= \overline{A\bar{B}} + A\bar{B}$$

$$E = C \odot D$$
$$= \overline{CD} + CD$$
$$= \overline{(A\bar{B} + A\bar{B})(\overline{\bar{A}B} + \bar{A}B)} + (\overline{A\bar{B}} + A\bar{B})(\overline{\bar{A}B} + \bar{A}B)$$
$$= 1$$

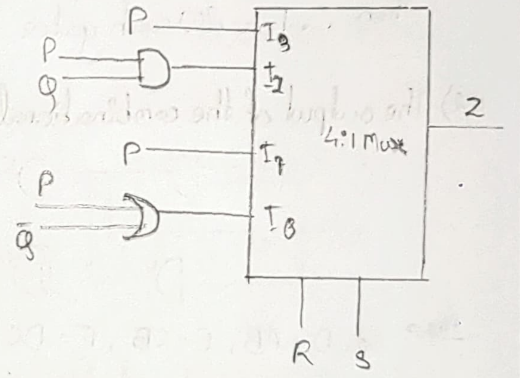
Q4) The number of product terms in the minimised sum-of-product expression obtained through the following k-map is (where, "d" denotes don't care states)

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	d	0	0
11	0	0	d	1
10	1	0	0	1

Ans → $F(A,B,C,D) = B'D' + ACD'$

So, No. of product terms → 2

Q5) For the circuit shown in the following fig., I_0 - I_3 are inputs to the 4:1 multiplexer. R (MSB) and S are control bits →

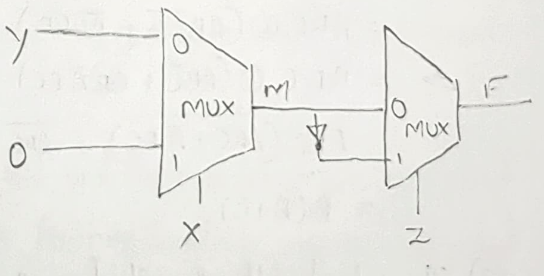


Ans → Truth Table

R	S	Z
0	0	$I_3 = P$
0	1	$I_2 = PQ$
1	0	$I_1 = P$
1	1	$I_0 = P\bar{Q}$

$Z = P\bar{R}\bar{S} + PQ\bar{R}S + PR\bar{S} + P\bar{Q}RS$

Q6) The Boolean expression F implemented by the circuit is →



Ans → $M = X'Y + X \cdot 0 = X'Y$

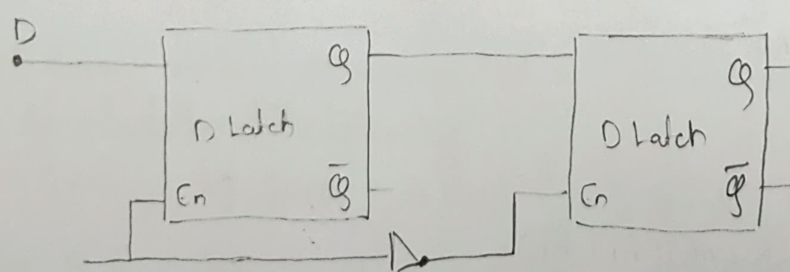
$F = Z'M + ZM'$

$= Z'X'Y + Z(X'Y)'$

$= Z'X'Y + Z(X + Y')$

$= Z'X'Y + ZX + ZY'$

Q7) The circuit shown in the fig. is a → d) Master-Slave D flip-flop

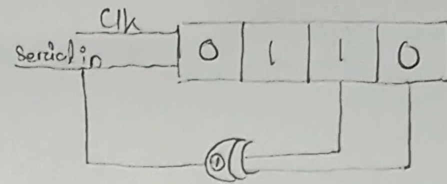


Q8) The initial contents of the 4-bit serial-in-parallel-out, right shift, shift register, shown in the fig. is 0110. After three clock pulses are applied, the contents of the shift Register will be →

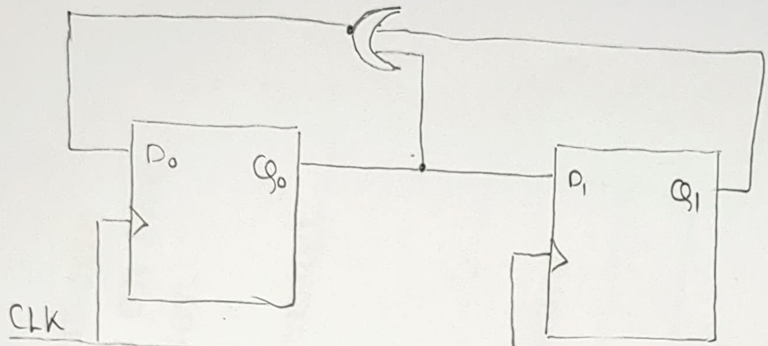
At pulse 1 input, 1 ⊕ 0 = 1
So, contents are 1011

At pulse 2 input, 1 ⊕ 1 = 0
Contents are 0101

At pulse 3 input, 0 ⊕ 1 = 1
So, Contents are <u>1010</u>.



Q9) For the circuit below, the counter state (Q_1, Q_0) follows the sequence



b) 00, 01, 10, 00, 01, ...

Q10) Briefly explain the following representations: sign magnitude, two's complement, biased.

Ans→ Sign Magnitude → The leftmost bit is the sign bit, and the remaining bits represent the represent the magnitude. A 0 represents a positive number, and a 1 represents a negative number.

Two's complement → The leftmost bit is the sign bit, and the remaining bits represent as the two's complement of their absolute values. Positive numbers are represented the same way as in sign magnitude.

Biased → A fixed value, called the bias, is added to the integer. The leftmost bit stores the sign of the number, with 0 representing positive & 1 representing negative.

Q12) Assume numbers are represented in 8-bit two's complement representation. Show the calculation of the following:

a) 6 + 13   b) -6 + 13   c) 6 - 13   d) -6 - 13

Ans→ a) 6 → 00000110
13 → + 00001101
00010011 (19)

b) -6 → 11111010
13 → + 00001101
00000111 (7)

c) 6 → 00000110
13 → - 00001101
11111011 (-7)

d) $-6 \rightarrow 11111010$

$-13 \rightarrow 00001101$

$\overline{}$

1110111 (-19)