CS1050-Computer organization and digital design

Lab 5 – Counters

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1. Introduction
    - Lab task

    In this lab, we designed a 3-bit counter, a slowdown clock and a D flip-flop. The 3-bit counter was developed using slowdown clock and D flip-flop. The 3- bit counter counts clockwise and anti-clockwise direction based on an external input.

    - Excitation tables

Excitation table of D flip-flop: -

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(Clk=1)

For the 3-bit counter: -

Q_t			Button (B)	Q_{t+1}			D_2	D_1	D_0
Q_2	Q_1	Q_0		Q_2	Q_1	Q_0			
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	0	0	X	X	X	X	X	X
0	1	0	1	X	X	X	X	X	X
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	1	0	0	1	0
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	1	0	1
1	0	1	0	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X
1	1	0	0	0	0	1	0	0	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	0	1	1	0	1
1	1	1	1	1	1	0	1	1	0

- K-maps & simplified Boolean expressions for D_0, D_1, D_2

$D_2 = Q_1B' + Q'_0B$

Q_2Q_1					
Q_0B		00	01	11	10
	00	0	X	1	0
	01	1	X	1	1
	11	0	0	0	X
	10	0	1	1	X

$D_1 = Q_2B + Q_0B'$

Q_2Q_1					
Q_0B		00	01	11	10
	00	0	X	0	0
	01	0	X	1	1
	11	0	0	1	X
	10	1	1	1	X

$D_0 = Q_1B + Q'_2B'$

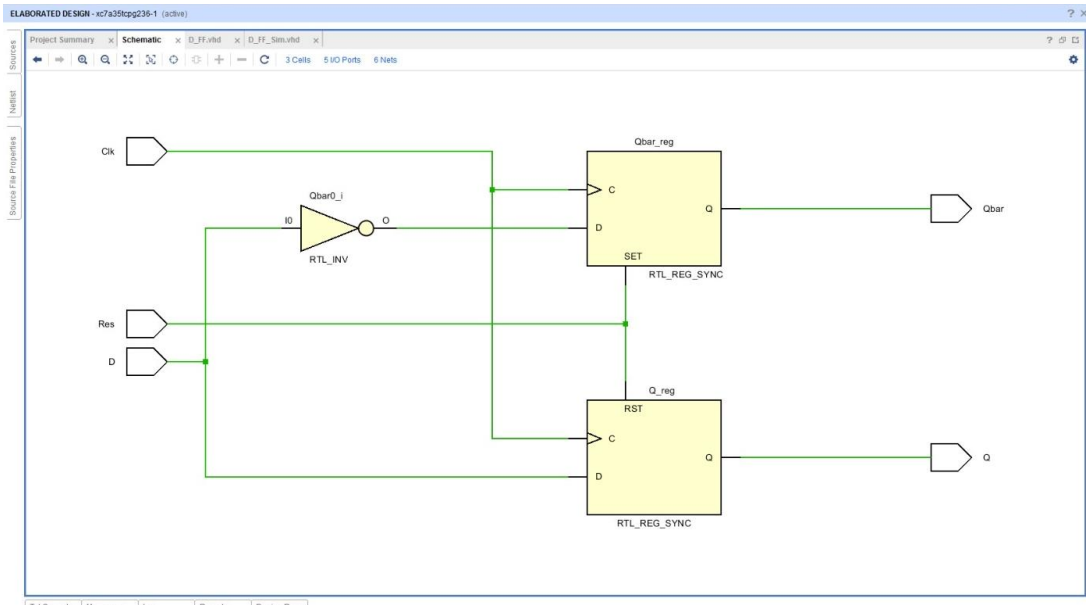
Q_2Q_1					
Q_0B		00	01	11	10
	00	1	X	0	0
	01	0	X	1	0
	11	0	1	1	X
	10	1	1	0	X

2. D flip-flop
    - Design source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/07/2024 11:56:08 AM
-- Design Name:
-- Module Name: D_FF - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
----------------------------------------------------------------------------------
-
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;




entity D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end D_FF;

architecture Behavioral of D_FF is
begin

   process (Clk) begin
        if (rising_edge(Clk)) then
            if Res = '1' then
                Q <= '0';
                Qbar <= '1';
```

```
            else
                Q <= D;
                Qbar <= not D;
            end if;
        end if;
    end process;
end Behavioral
```

- Elaborated design schematic



- Simulation source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/07/2024 12:01:20 PM
-- Design Name:
-- Module Name: D_FF_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF_Sim is
--  Port ( );
end D_FF_Sim;

architecture Behavioral of D_FF_Sim is

component D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end component;

signal D, Res, Q, Qbar : STD_LOGIC;
signal Clk : STD_LOGIC := '0';

begin

UUT : D_FF
    PORT MAP(
        D=>D,
        Res=>Res,
        Clk=>Clk,
        Q=>Q,
        Qbar=>Qbar);
```

```
PROCESS
BEGIN
    Clk<=NOT(Clk);
    WAIT FOR 20 NS;
END PROCESS;

PROCESS
BEGIN
    Res<='1';
    D<='0';
    WAIT FOR 50 NS;

    Res<='0';
    D<='0';
    WAIT FOR 50 NS;

    D<='1';
    WAIT FOR 50 NS;

    D<='0';
    WAIT FOR 50 NS;

END PROCESS;

end Behavioral;
```

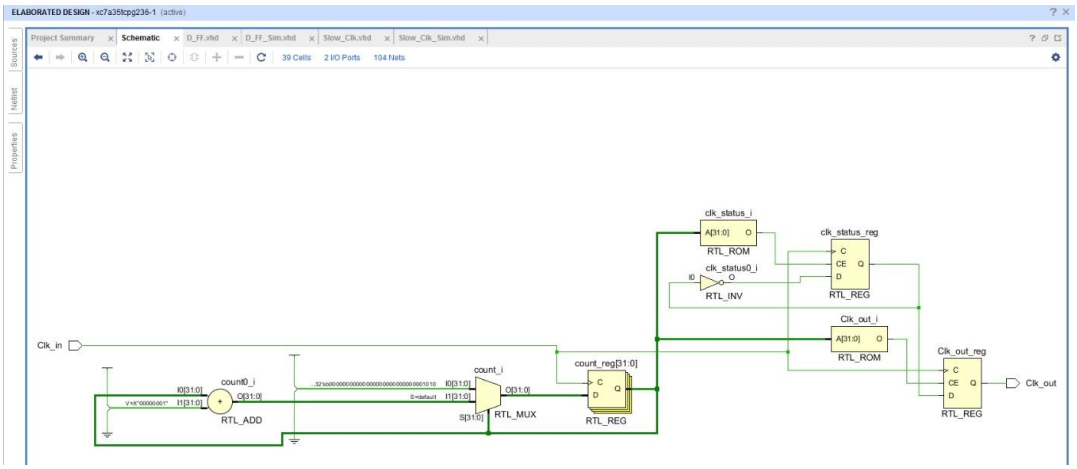
- Timing diagram

3. Slow clock
    - Design source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/07/2024 12:39:32 PM
-- Design Name:
-- Module Name: Slow_Clk - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count : integer := 1;
signal clk_status : std_logic := '0';
```

```
begin

    process (Clk_in) begin
        if (rising_edge(Clk_in)) then
            count <= count+1;
            if(count= 5) then
                clk_status <= not clk_status;
                Clk_out <= clk_status;
                count <= 1;
            end if;
        end if;
    end process;


end Behavioral;
```

- Elaborated design schematic

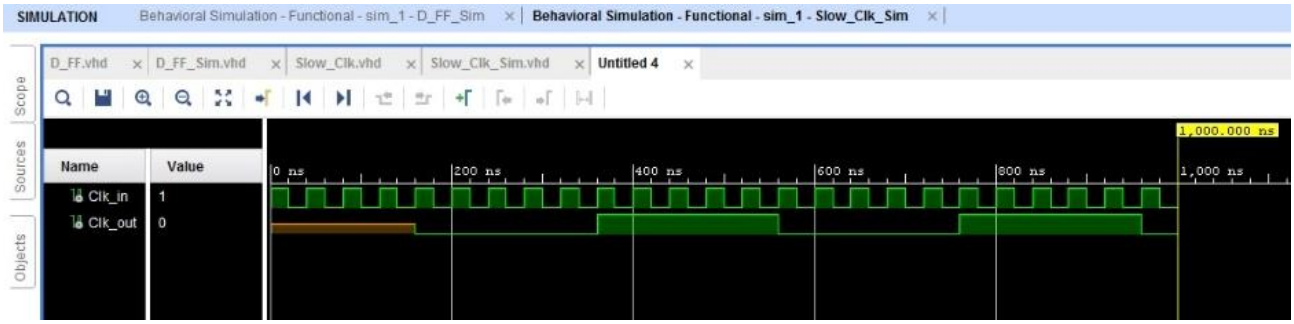


- Simulation source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/07/2024 12:55:42 PM
-- Design Name:
-- Module Name: Slow_Clk_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
```

```
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk_Sim is
--  Port ( );
end Slow_Clk_Sim;

architecture Behavioral of Slow_Clk_Sim is

component Slow_Clk
    port (Clk_in : in std_logic;
          Clk_out : out std_logic);
end component;

signal Clk_in : std_logic :='0';
signal Clk_out : std_logic;

begin

UUT : Slow_Clk
    port map (
        Clk_in=>Clk_in,
        Clk_out=>Clk_out);

process
    begin
        Clk_in<= not Clk_in;
        wait for 20 ns;
end process;
end Behavioral;
```

- Timing diagram



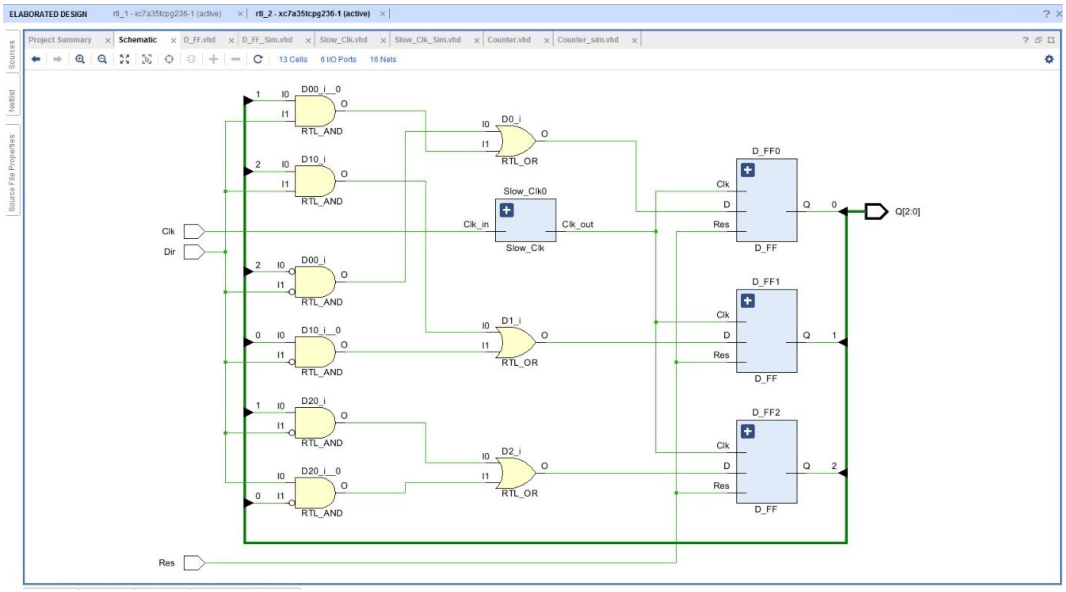
4. Counter
    - Design source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/07/2024 01:35:50 PM
-- Design Name:
-- Module Name: Counter - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
```

```
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end Counter;

architecture Behavioral of Counter is

component D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end component;

component Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end component;

-- add your signal declarations here

signal D0,D1,D2:std_logic;
signal Q0,Q1,Q2:std_logic;
signal Clk_slow:std_logic;

begin

Slow_Clk0:Slow_clk
    port map(
    Clk_in=>Clk,
    Clk_out=>Clk_slow
    );


D_FF0 : D_FF
PORT MAP(
     D=>D0,
     Res=>Res,
```

```
     Clk=>Clk_slow,
     Q=>Q0
    );
D_FF1 : D_FF
PORT MAP(
     D=>D1,
     Res=>Res,
     Clk=>Clk_slow,
     Q=>Q1
);
D_FF2 : D_FF
PORT MAP(
     D=>D2,
     Res=>Res,
     Clk=>Clk_slow,
     Q=>Q2
    );

D0<=((not Q2) and (not Dir)) or (Q1 and Dir);
D1<=(Q2 and Dir) or (Q0 and (not Dir));
D2<=(Q1 and (not Dir)) or (Dir and (not Q0));

Q(0)<=Q0;
Q(1)<=Q1;
Q(2)<=Q2;


end Behavioral;
```

- Elaborated design schematic



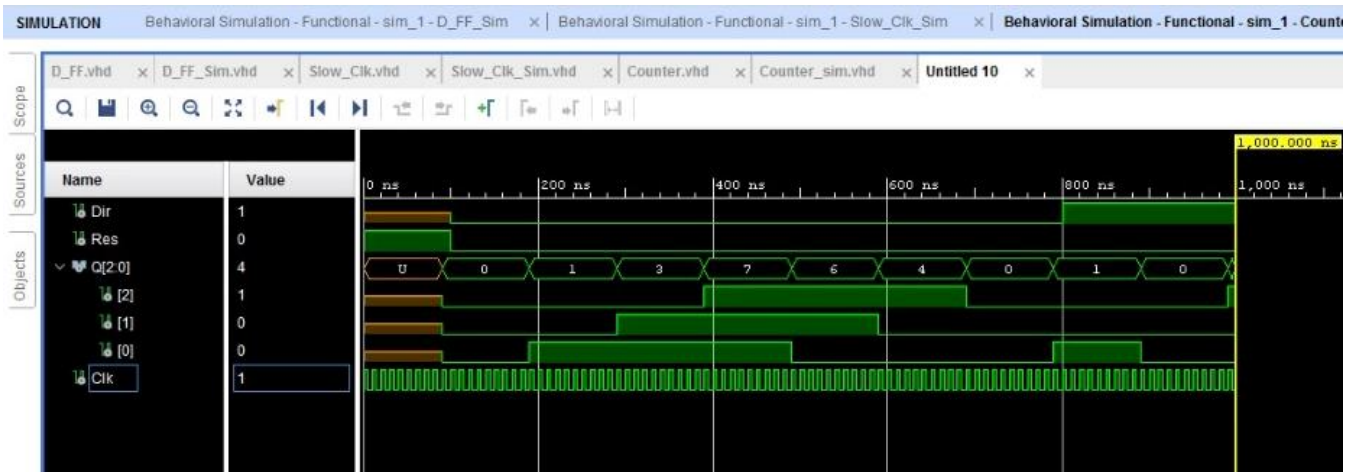
- Simulation source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/07/2024 01:42:01 PM
-- Design Name:
-- Module Name: Counter_sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
```

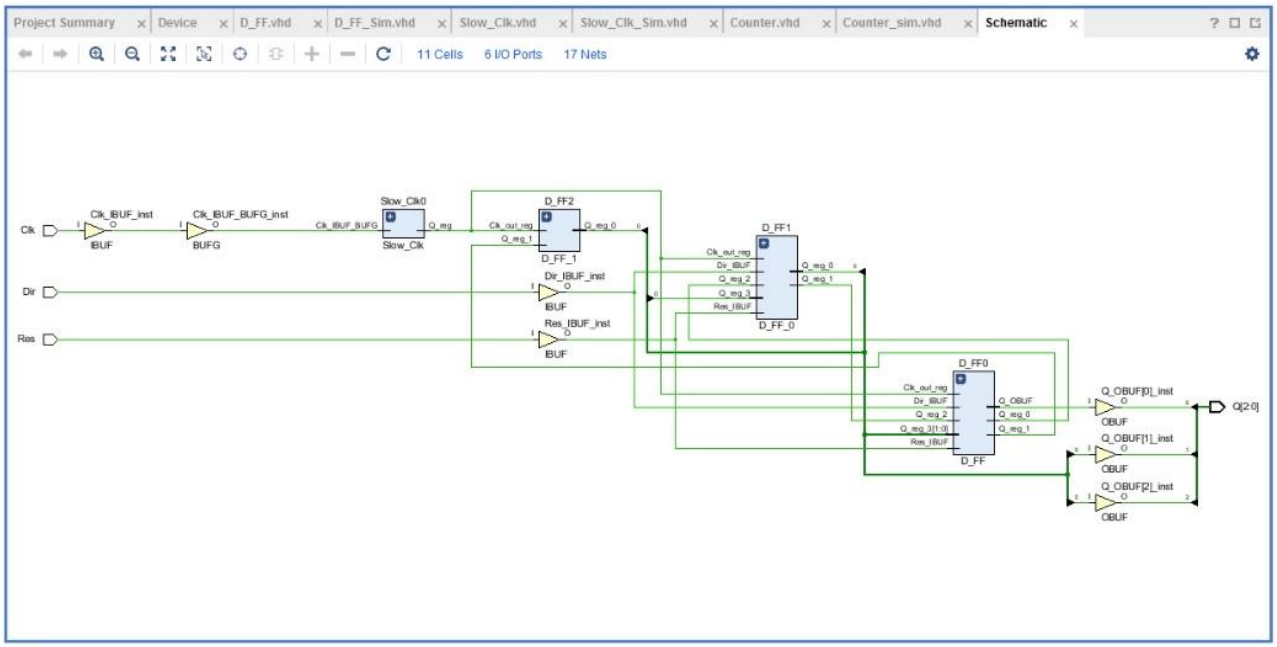
```
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Counter_sim is
--  Port ( );
end Counter_sim;

architecture Behavioral of Counter_sim is
component Counter is
    Port ( Dir : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC_VECTOR (2 downto 0));
end component;

signal Dir, Res: std_logic;
signal  Q : std_logic_vector(2 downto 0);
signal Clk : std_logic:='0';

begin

UUT : Counter
    port map(
    Clk => Clk,
    Dir=>Dir,
    Res=>Res,
    Q=>Q);

process
    begin
        Clk <= not Clk;
        wait for 5 ns;
end process;

process
begin

    Res <= '1';
    wait for 100 ns;

    Res <= '0';
```

```
    Dir <= '0';
    wait for 700 ns;

    Res <= '0';
    Dir <= '1';
    wait for 700 ns;
end process;


end Behavioral;
```

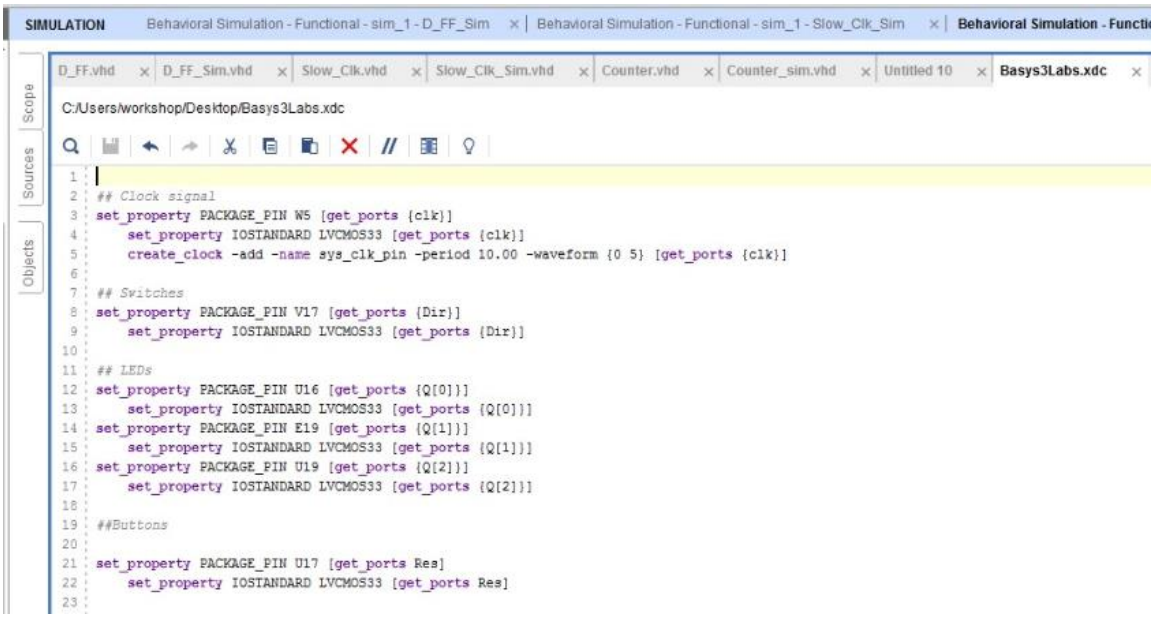
- Timing diagram



- Implemented design schematic



- Constraints file



5. Conclusion

   In this lab we used D flip-flops to design the counter. But we can also use JK flip-flops to design the counter. We used ‘Dir’ switch to change the direction of the counter. We can verify the functionality of the circuit via simulation and on the development board.