**CS1050-Computer organization and digital design**

**Lab 7 – 7-Segment Display**

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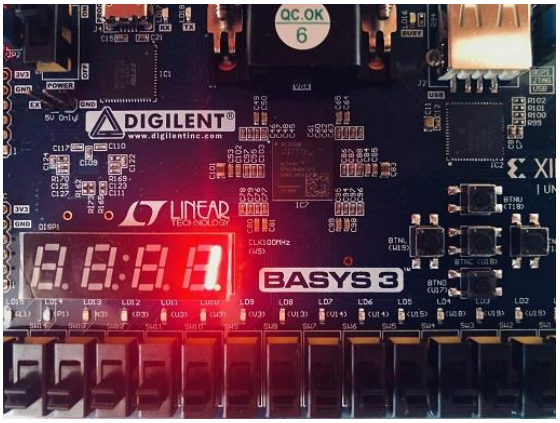
## 1. Introduction

### 1.1. Introduce the lab task

Main task of this lab is to design 7-Segment Display which is a simple electronic device that is used to display decimal numerals and some alphabetic characters. In this lab we designed a 7-segments display to display the output of our 4-bit arithmetic unit (developed in lab 6) as a hexadecimal number.

For that first we developed a lookup table using ROM. It was used to map the 4-bit sum to the 7-segments on the display. Finally, we verified the functionality of the circuit via simulation and on the development board.



(a picture of a 7-segment display)

### 1.2. Table of segments to switch on

| Output from RCA | | | | | Segment to switch on | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S3 | S2 | S1 | S0 | Hex. value | A | B | C | D | E | F | G |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 7 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | A | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | B | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | C | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | E | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | F | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

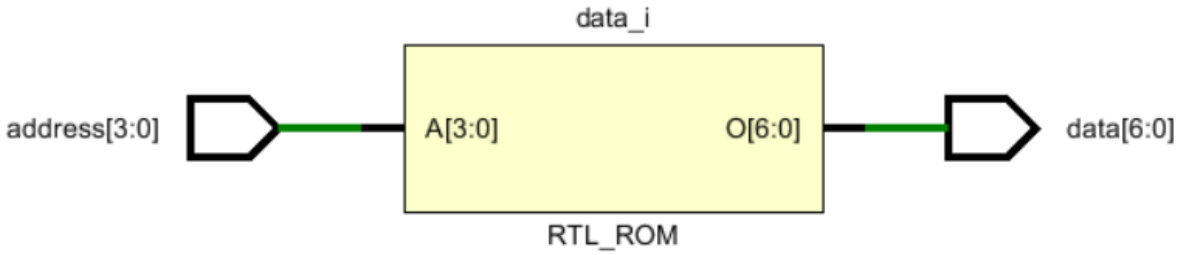
## 2. Lookup Tables

### 2.1. Design source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/21/2024 02:35:11 PM
-- Design Name:
-- Module Name: LUT_16_7 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity LUT_16_7 is
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end LUT_16_7;

architecture Behavioral of LUT_16_7 is

type rom_type is array (0 to 15) of std_logic_vector(6 downto 0);

 signal sevenSegment_ROM : rom_type := (
         "1000000", --0
         "1111001", --1
         "0100100", --2
         "0110000", --3
         "0011001", --4
         "0010010", --5
         "0000010", --6
         "1111000", --7
         "0000000", --8
         "0010000", --9
         "0001000", --a
         "0000011", --b
         "1000110", --c
         "0100001", --d
         "0000110", --e
         "0001110"  --f );

begin

data <= sevenSegment_ROM(to_integer(unsigned(address)));

end Behavioral;
```

### 2.2. Elaborated design schematic




### 2.3. Simulation source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 03/21/2024 03:11:06 PM
-- Design Name:
-- Module Name: LUT_16_7_Sim - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
```

```
entity LUT_16_7_Sim is
--  Port ( );
end LUT_16_7_Sim;

architecture Behavioral of LUT_16_7_Sim is

component LUT_16_7
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

signal address : STD_LOGIC_VECTOR (3 downto 0);
signal data :  STD_LOGIC_VECTOR (6 downto 0);

begin
uut: LUT_16_7
    port map(
        address=>address,
        data=>data);

process
begin

address<="0010";
wait for 100ns;

address<="0010";
wait for 100ns;

address<="0000";
wait for 100ns;

address<="0000";
wait for 100ns;

address<="1001";
wait for 100ns;

address<="1000";
wait for 100ns;

address<="1100";
wait;
end process;
end Behavioral;
```

### 2.4. Timing diagram


## 3. 7-Segment Display

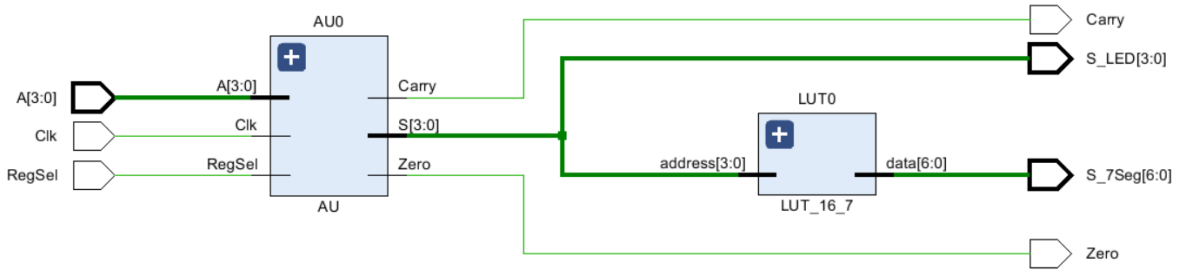
### 3.1. Design source file

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 03/21/2024 03:43:50 PM
-- Design Name:
-- Module Name: AU_7_seg - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
```

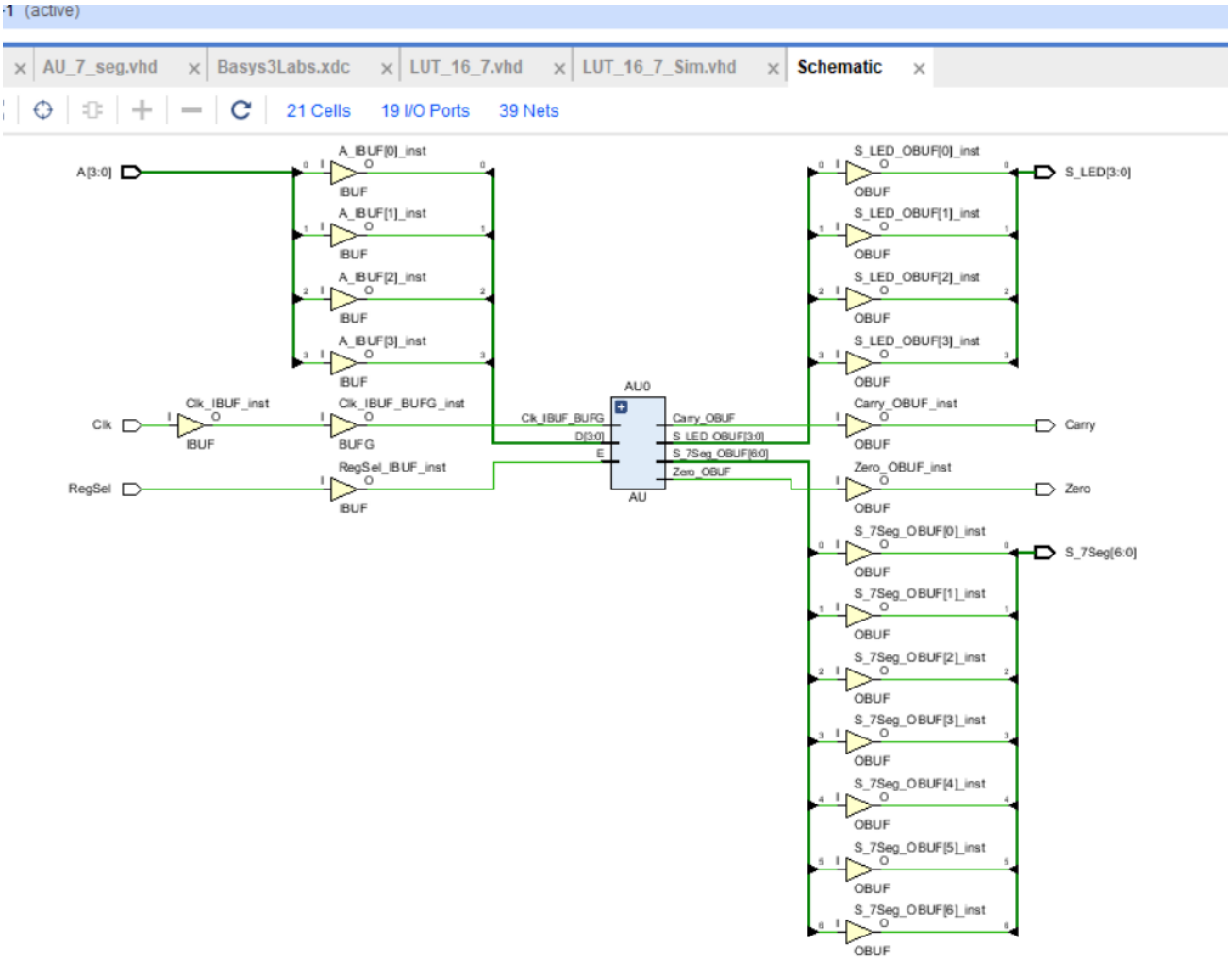
```
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity AU_7_seg is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           Clk : in STD_LOGIC;
           RegSel : in STD_LOGIC;
           S_LED : out STD_LOGIC_VECTOR (3 downto 0);
           S_7Seg : out STD_LOGIC_VECTOR (6 downto 0);
           Carry : out STD_LOGIC;
           Zero : out STD_LOGIC);
end AU_7_seg;

architecture Behavioral of AU_7_seg is

component AU
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           RegSel : in STD_LOGIC;
           Clk : in STD_LOGIC;
           S : out STD_LOGIC_VECTOR (3 downto 0);
           Zero : out STD_LOGIC;
           Carry : out STD_LOGIC);
end component;

component LUT_16_7
    Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
           data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

signal sum : std_logic_vector(3 downto 0);
```

```
begin
AU0: AU
    port map(
        A=>A,
        RegSel=>RegSel,
        Clk=>Clk,
        S=>sum,
        Zero=>Zero,
        Carry=>Carry);

LUT0: LUT_16_7
    port map(
        address=>sum,
        data=>S_7Seg);

S_LED<=sum;
end Behavioral;
```

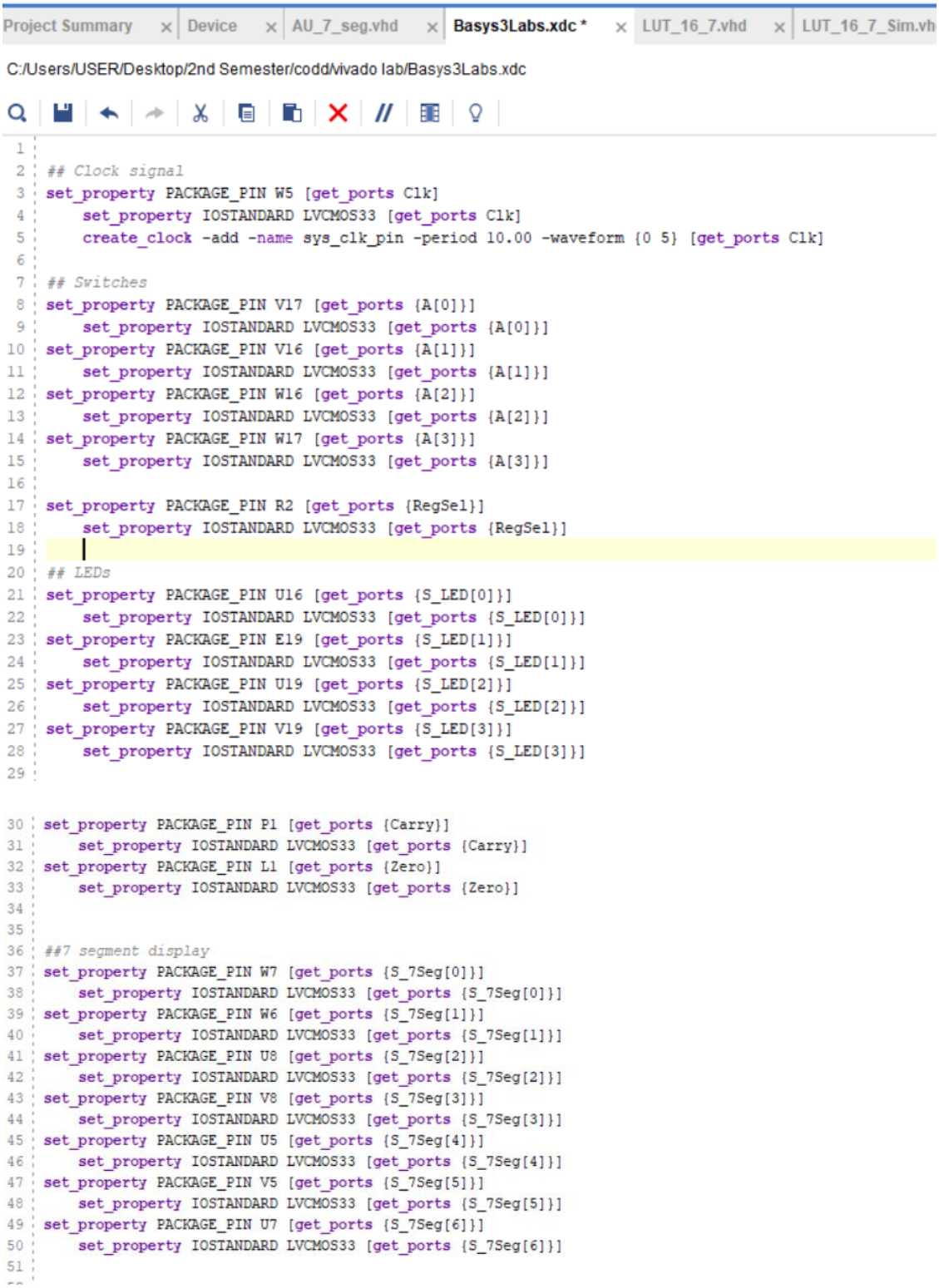
### 3.2. Elaborated design schematic



### 3.3. Implemented design schematic



## 3.4. Constraints file




```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
    set_property IOSTANDARD LVCMOS33 [get_ports Clk]
    create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports Clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {A[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property PACKAGE_PIN V16 [get_ports {A[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property PACKAGE_PIN W16 [get_ports {A[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property PACKAGE_PIN W17 [get_ports {A[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]

set_property PACKAGE_PIN R2 [get_ports {RegSel}]
    set_property IOSTANDARD LVCMOS33 [get_ports {RegSel}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {S_LED[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[0]}]
set_property PACKAGE_PIN E19 [get_ports {S_LED[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[1]}]
set_property PACKAGE_PIN U19 [get_ports {S_LED[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[2]}]
set_property PACKAGE_PIN V19 [get_ports {S_LED[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_LED[3]}]


set_property PACKAGE_PIN P1 [get_ports {Carry}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Carry}]
set_property PACKAGE_PIN L1 [get_ports {Zero}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Zero}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {S_7Seg[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {S_7Seg[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {S_7Seg[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {S_7Seg[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {S_7Seg[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {S_7Seg[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {S_7Seg[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S_7Seg[6]}]
```

## 4. Conclusion

This lab focused on designing a 7-segment display interface for a 4-bit Arithmetic Unit. By utilizing a ROM-based lookup table, the 4-bit sum generated by the Arithmetic Unit was mapped to the appropriate segments for hexadecimal display. Through simulation, we gained practical insights into digital design, ROM usage, and circuit interfacing.