CS1050-Computer organization and digital design

Lab 3 – Ripple Carry Adder

Student Name: De Silva A.D.D.T.

Index Number: 220098C

Group Number: 33

Task

First task is to build a Half Adder (HA), then a Full Adder (FA) and finally the 4-bit Ripple Carry Adder (RCA).

First step of the task is finding Boolean expressions for HA and FA.

Second step of the task is creating new project in Xilinx Vivado to build a HA using basic logic gates.

Third step is building a FA using HAs and basic logic gates.

Final step is to build 4-bit RCA using multiple FAs and check its functionality.

Half Adder

Truth table: -

A	B	C	S
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(A, B=inputs, C= carry bit, S=sum)

Boolean expressions: -

$S=A'B + AB' = A \oplus B$

$C=AB$

HA VHDL file (HA.VHD): -

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 02/13/2024 02:24:46 PM
-- Design Name:
-- Module Name: HA - Behavioral
-- Project Name: LAB 3
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity HA is
   Port ( A : in STD_LOGIC;
          B : in STD_LOGIC;
          S : out STD_LOGIC;
          C : out STD_LOGIC);
end HA;

architecture Behavioral of HA is
```

```
begin
   S<= (A AND (NOT B)) OR ((NOT A) AND B);
   C<= A AND B;

end Behavioral;
----------------------------------------------------------------------------------------------------
```

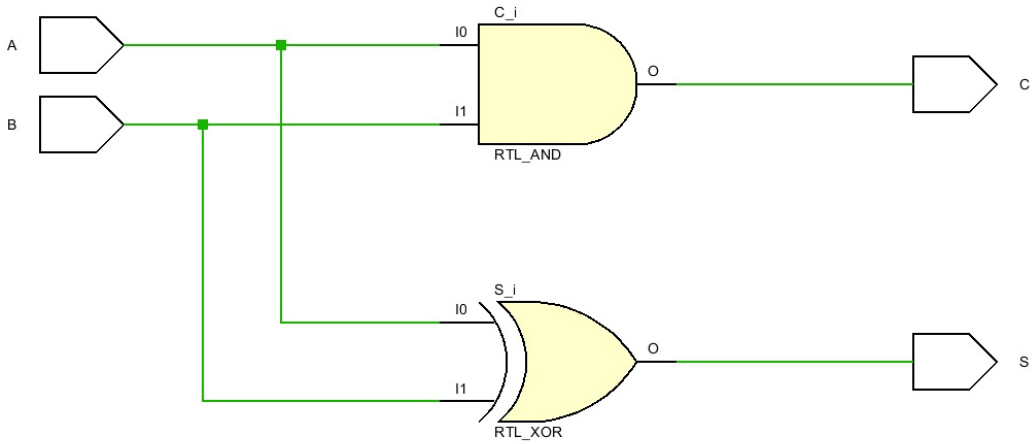
HA test bench code (TB_HA.VHD): -

```
----------------------------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 02:41:16 PM
-- Design Name:
-- Module Name: TB_HA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_HA is
--  Port ( );
end TB_HA;

architecture Behavioral of TB_HA is
   COMPONENT HA
```

```
        PORT(   A,B: IN STD_LOGIC;
                C,S: OUT STD_LOGIC);
    END COMPONENT;

    SIGNAL A,B :STD_LOGIC;
    SIGNAL C,S :STD_LOGIC;

begin
    UUT: HA PORT MAP(
        A=>A,
        B=>B,
        C=>C,
        S=>S

    );
    PROCESS
    BEGIN
        A<='0';
        B<='0';

        WAIT FOR 100 NS;
        B<='1';

        WAIT FOR 100 NS;
        A<='1';
        B<='0';

        WAIT FOR 100 NS;
        B<='1';

        WAIT;
    END PROCESS;
end Behavioral;
```

HA simulation results (timing diagrams): -

HA schematic diagram: -



Full Adder

Truth Table: -

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(A, B, C_{in} =inputs, S=sum, C= carry bit)

Boolean expression: -

$S = A'B'C_{in} + A'BC_{in} + AB'C_{in}' + ABC_{in}$

$S = A'(B'C_{in} + BC_{in}') + A(B'C_{in}' + B'C_{in}')$

$S = A'(B \oplus C_{in}) + A(B \oplus C_{in})$

$S = A \oplus B \oplus C_{in}$

$C_{out} = A'B\ C_{in} + AB'\ C_{in} + AB\ C_{in}' + AB\ C_{in}$

$C_{out} = AB(\ C_{in} + C_{in}') + C_{in}(A'B + A\ B')$

$C_{out} = AB + C_{in}\ (A \oplus B)$

$C_{out} = AB + BC_{in} + AC_{in}$

FA VHDL file (FA.vhd): -

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: De Silva A D D T
--
-- Create Date: 02/13/2024 03:03:47 PM
-- Design Name:
-- Module Name: FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity FA is
    Port ( A : in STD_LOGIC;
```

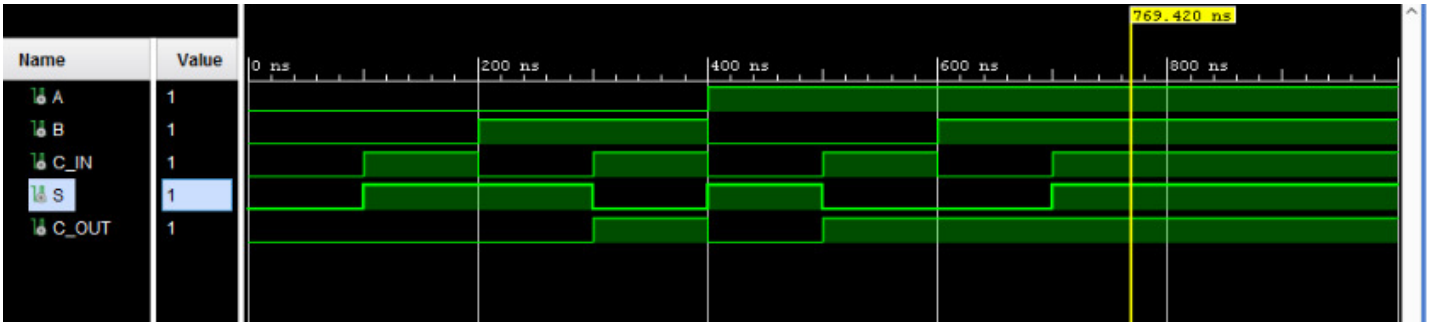
```
        B : in STD_LOGIC;
        C_IN : in STD_LOGIC;
        S : out STD_LOGIC;
        C_OUT : out STD_LOGIC);
end FA;


architecture Behavioral of FA is

component HA
port (
            A: in std_logic;
            B: in std_logic;
            S: out std_logic;
            C: out std_logic);
end component;

SIGNAL HA0_S, HA0_C, HA1_S, HA1_C : std_logic;
begin
   S<= A XOR B XOR C_IN;
   C_OUT<=(A AND B) OR (B AND C_IN) OR (A AND C_IN);

 HA_0 : HA

 port map (
            A => A,
            B => B,
            S => HA0_S,
            C => HA0_C);

 HA_1 : HA

 port map (
             A => HA0_S,
             B => C_in,
            S => HA1_S,
            C => HA1_C);


end Behavioral;
----------------------------------------------------------------------------------------------
```

FA Test Bench Code (TB_FA.vhd): -

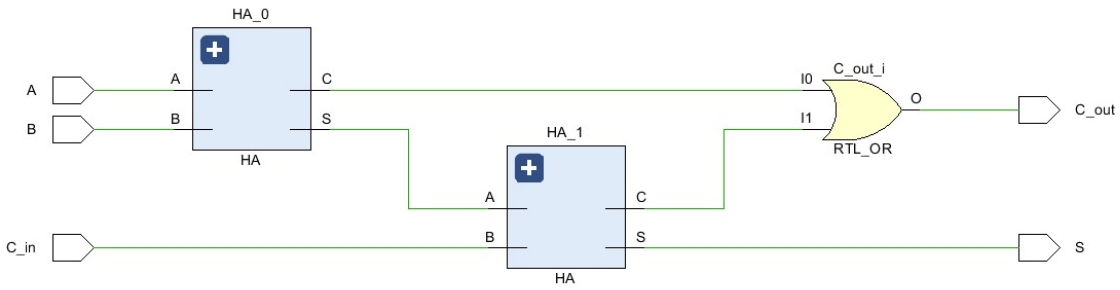
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/13/2024 03:22:20 PM
-- Design Name:
-- Module Name: TB_FA - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_FA is
--  Port ( );
end TB_FA;

architecture Behavioral of TB_FA is

COMPONENT FA
   PORT(   A,B,C_IN : IN STD_LOGIC;
           S,C_OUT : OUT STD_LOGIC);
END COMPONENT;

SIGNAL A,B,C_IN: STD_LOGIC;
```

```
SIGNAL S, C_OUT: STD_LOGIC;

begin
UUT: FA PORT MAP(
      A=>A,
      B=>B,
      C_IN=>C_IN,
      S=>S,
      C_OUT=>C_OUT
);

PROCESS
BEGIN
   A<='0';
   B<='0';
   C_IN<='0';

   WAIT FOR 100 NS;
   C_IN<='1';

   WAIT FOR 100 NS;
   B<='1';
   C_IN<='0';

   WAIT FOR 100 NS;
   C_IN<='1';

   WAIT FOR 100 NS;
   A<='1';
   B<='0';
   C_IN<='0';

   WAIT FOR 100 NS;
   C_IN<='1';

   WAIT FOR 100 NS;
   B<='1';
   C_IN<='0';

   WAIT FOR 100 NS;
   C_IN<='1';

   WAIT;
END PROCESS;


end Behavioral;
```

FA simulation results (timing diagrams): -



FA schematic diagram: -



Ripple Carry Adder

4-Bit-RCA VHDL file (RCA_4.vhd): -

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: De Silva A D D T
--
-- Create Date: 02/13/2024 04:34:40 PM
-- Design Name:
-- Module Name: RCA_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity RCA_4 is
   Port ( A0 : in STD_LOGIC;
          A1 : in STD_LOGIC;
          A2 : in STD_LOGIC;
          A3 : in STD_LOGIC;
          B0 : in STD_LOGIC;
          B1 : in STD_LOGIC;
          B2 : in STD_LOGIC;
          B3 : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S0 : out STD_LOGIC;
          S1 : out STD_LOGIC;
          S2 : out STD_LOGIC;
          S3 : out STD_LOGIC;
          C_out : out STD_LOGIC);
end RCA_4;

architecture Behavioral of RCA_4 is

component FA
port (
A: in std_logic;
B: in std_logic;
C_in: in std_logic;
S: out std_logic;
C_out: out std_logic);
end component;
```

```
SIGNAL FA0_S, FA0_C, FA1_S, FA1_C, FA2_S, FA2_C, FA3_S, FA3_C
   : std_logic;

begin

FA_0 : FA
port map (
A => A0,
B => B0,
C_in => '0', -- Set to ground
S => S0,
C_Out => FA0_C);

FA_1 : FA
port map (
A => A1,
B => B1,
C_in => FA0_C,
S => S1,
C_Out => FA1_C);

FA_2 : FA
port map (
A => A2,
B => B2,
C_in => FA1_C,
S => S2,
C_Out => FA2_C);

FA_3 : FA
port map (
A => A3,
B => B3,
C_in => FA2_C,
S => S3,
C_Out => C_out);

end Behavioral;
```

4-Bit-RCA Tech Bench code (RCA_4_TB.vhd): -

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 02/13/2024 04:48:11 PM
-- Design Name:
-- Module Name: TB_4_RCA - Behavioral
-- Project Name: lAN 3
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_4_RCA is
--  Port ( );
end TB_4_RCA;

architecture Behavioral of TB_4_RCA is

COMPONENT RCA_4
   PORT(
   A0,A1,A2,A3,B0,B1,B2,B3,C_in :IN STD_LOGIC;
   S0,S1,S2,S3,C_out : OUT STD_LOGIC);
END COMPONENT;
```

```
   SIGNAL A0,A1,A2,A3,B0,B1,B2,B3,C_in : STD_LOGIC;
   SIGNAL S0,S1,S2,S3,C_out : STD_LOGIC;



begin

UUT: RCA_4 PORT MAP(
   A0=>A0,
   A1=>A1,
   A2=>A2,
   A3=>A3,
   B0=>B0,
   B1=>B1,
   B2=>B2,
   B3=>B3,
   C_in=>C_in,
   S0=>S0,
   S1=>S1,
   S2=>S2,
   S3=>S3,
   C_out=>C_out
);

PROCESS
BEGIN
      A0<='0';
      A1<='1';
      A2<='0';
      A3<='0';
      B0<='0';
      B1<='0';
      B2<='1';
      B3<='1';
      C_in<='0';

WAIT FOR 100 NS;
   A0<='1';
   A1<='1';
   A2<='0';
   A3<='1';
   B0<='1';
   B1<='0';
   B2<='1';
   B3<='0';
   C_in<='0';

WAIT FOR 100 NS;
```

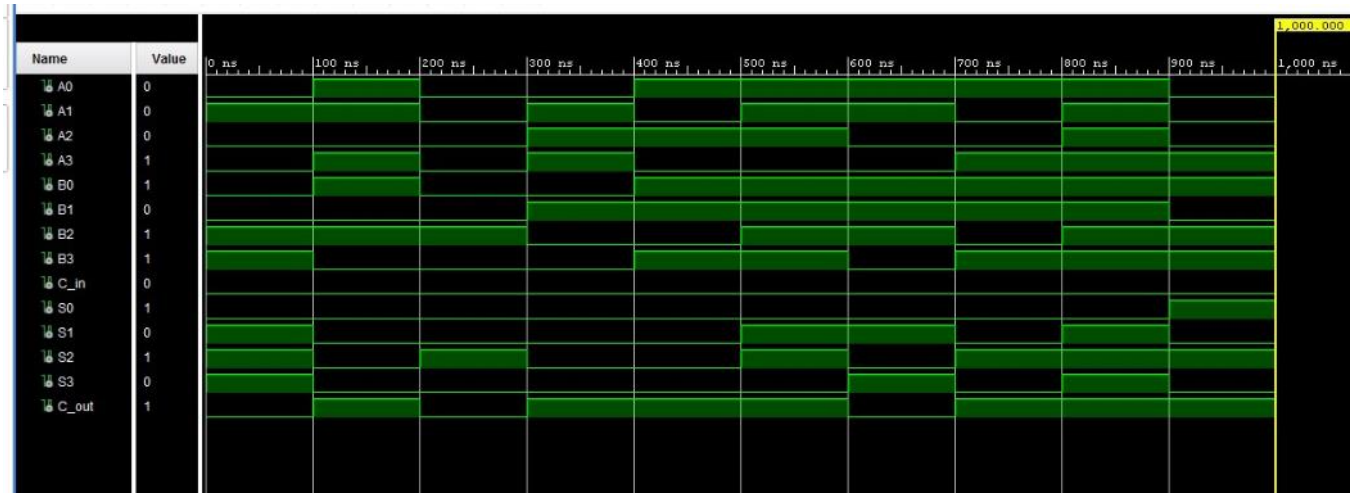
```
    A0<='0';
    A1<='0';
    A2<='0';
    A3<='0';
    B0<='0';
    B1<='0';
    B2<='1';
    B3<='0';
    C_in<='0';

WAIT FOR 100 NS;
    A0<='0';
    A1<='1';
    A2<='1';
    A3<='1';
    B0<='0';
    B1<='1';
    B2<='0';
    B3<='0';
    C_in<='0';

WAIT FOR 100 NS;
    A0<='1';
    A1<='0';
    A2<='1';
    A3<='0';
    B0<='1';
    B1<='1';
    B2<='0';
    B3<='1';
    C_in<='0';

WAIT FOR 100 NS;
    A0<='1';
    A1<='1';
    A2<='1';
    A3<='0';
    B0<='1';
    B1<='1';
    B2<='1';
    B3<='1';
    C_in<='0';

WAIT FOR 100 NS;
    A0<='1';
    A1<='1';
    A2<='0';
    A3<='0';
```

```
    B0<='1';
    B1<='1';
    B2<='1';
    B3<='0';
    C_in<='0';

  WAIT FOR 100 NS;
    A0<='1';
    A1<='0';
    A2<='0';
    A3<='1';
    B0<='1';
    B1<='1';
    B2<='0';
    B3<='1';
    C_in<='0';

  WAIT FOR 100 NS;
    A0<='1';
    A1<='1';
    A2<='1';
    A3<='1';
    B0<='1';
    B1<='1';
    B2<='1';
    B3<='1';
    C_in<='0';

  WAIT FOR 100 NS;
    A0<='0';
    A1<='0';
    A2<='0';
    A3<='1';
    B0<='1';
    B1<='0';
    B2<='1';
    B3<='1';
    C_in<='0';
  WAIT;
  END PROCESS;

end Behavioral;
```

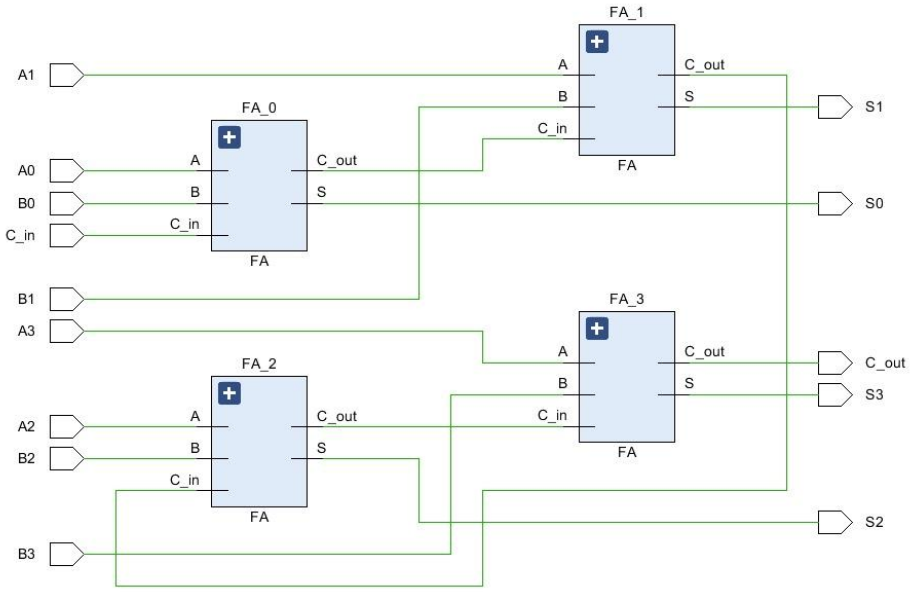
Input & Output Results Of RCA_4:-

B3	B2	B1	B0	A3	A2	A1	A0	C_{out}	S3	S2	S1	S0
0	0	1	0	1	1	0	0	0	1	1	1	0
0	1	0	1	1	0	1	1	1	0	0	0	0
0	0	0	0	0	1	0	0	0	0	1	0	0
1	1	1	0	0	0	1	0	1	0	0	0	0
0	1	0	1	1	0	1	1	1	0	0	0	0
0	1	1	1	1	1	1	1	1	0	1	1	0
0	0	1	1	0	1	1	1	0	1	0	1	0
1	0	0	1	1	0	1	1	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
1	0	0	0	1	1	0	1	1	0	1	0	1

RCA_4 simulation results (timing diagrams): -



RCA_4 schematic diagram: -



Discussion

- Why some of the input combinations results in outputs that cannot be represented using LED LD0-LD3.?

In a 4-bit Ripple Carry Adder (RCA), when the final carry out bit is 1, it indicates an overflow condition, meaning the result of the addition operation exceeds the maximum representable value (15 for unsigned integers). As a result, the output cannot be fully displayed using only the four LEDs (LD0-LD3), which are limited to representing values up to 15 in decimal (1111 in binary). Therefore, in overflow situations, the LEDs will show the maximum representable value (1111), signaling that the actual result is beyond their display range.

- What is the role of LD15 ?

In a ripple carry adder, LD15 is an additional LED used to indicate whether there is a carry out from the most significant bit position during addition. It visually shows if the addition result exceeds the maximum representable value for the given number of bits, aiding in detecting overflow conditions.