CS1050-Computer organization and digital design

Lab 4 – Combinational circuits

Student Name: De Silva A.D.D.T.

Index Number: 220098C

Group Number: 33

---

1. Introduction

Objective of this lab is to design a decoder and a multiplexer. Decoders and multiplexers are 2 of the key components of a microprocessor.

Decoder is a multi-input, multi-output logic circuit which decodes n inputs into 2^n possible output. In this lab we are going to design 2 to 4 decoder and a 3 to 8 decoder.

A multiplexer is a digital electronic device that selects one of several input signals and forwards it to a single output. We are going to design 8 to 1 multiplexer using previously created decoders.

2. 2-to-4 decoder

2.1 Truth tables and Boolean expressions

E	I0	I1	Y0	Y1	Y2	Y3
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	0	1	1	0	0	0

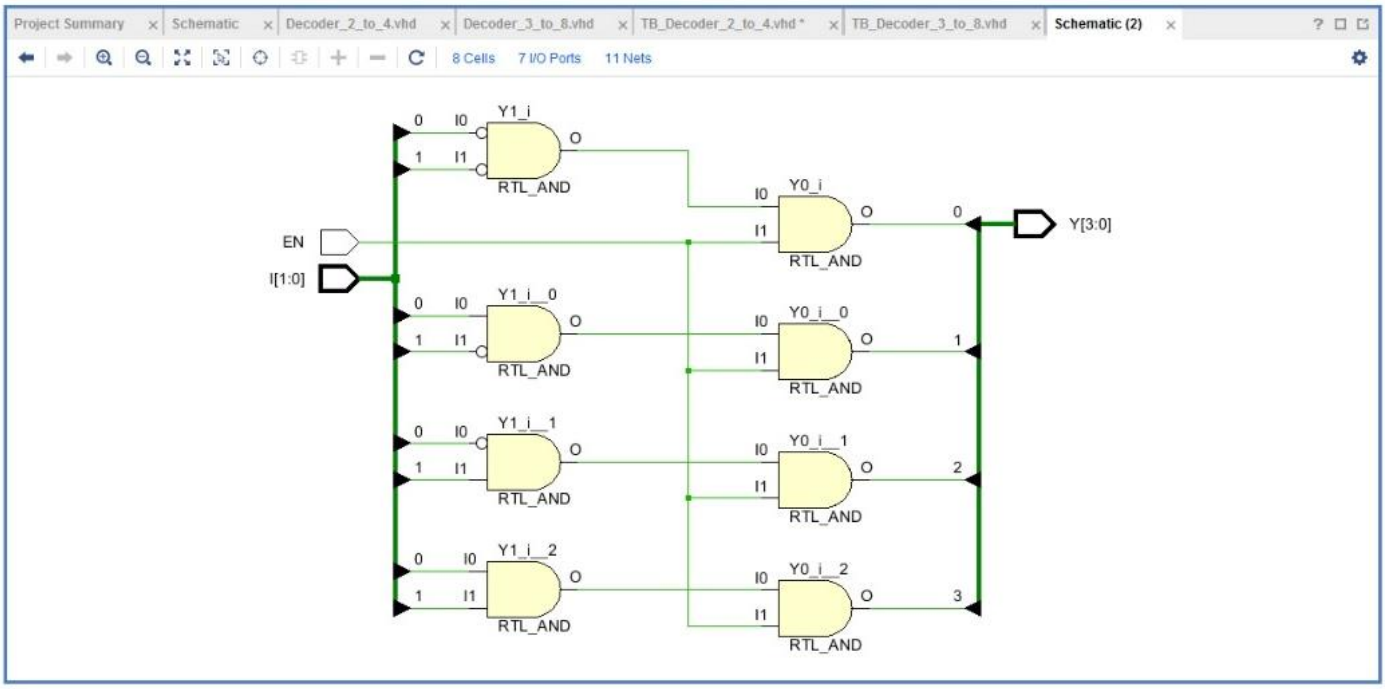
Y0=I0.I1
Y1=I0.I1’
Y2=I0’.I1
Y3=I0’.I1’

2.2 Design source file

```
3. ----------------------------------------------------------------------------
   ---------
4. -- Company:
5. -- Engineer:
6. --
7. -- Create Date: 02/20/2024 02:26:01 PM
8. -- Design Name:
```

```
9. -- Module Name: Decoder_2_to_4 - Behavioral
10.      -- Project Name:
11.      -- Target Devices:
12.      -- Tool Versions:
13.      -- Description:
14.      --
15.      -- Dependencies:
16.      --
17.      -- Revision:
18.      -- Revision 0.01 - File Created
19.      -- Additional Comments:
20.      --
21.      ----------------------------------------------------------------------
   --------------
22.      library IEEE;
23.      use IEEE.STD_LOGIC_1164.ALL;
24.
25.      -- Uncomment the following library declaration if using
26.      -- arithmetic functions with Signed or Unsigned values
27.      --use IEEE.NUMERIC_STD.ALL;
28.
29.      -- Uncomment the following library declaration if instantiating
30.      -- any Xilinx leaf cells in this code.
31.      --library UNISIM;
32.      --use UNISIM.VComponents.all;
33.
34.      entity Decoder_2_to_4 is
35.          Port ( I : in STD_LOGIC_VECTOR (1 downto 0);
36.                 EN : in STD_LOGIC;
37.                 Y : out STD_LOGIC_VECTOR (3 downto 0));
38.      end Decoder_2_to_4;
39.
40.      architecture Behavioral of Decoder_2_to_4 is
41.
42.      begin
43.          Y(0)<=(NOT I(0)) AND (NOT I(1)) AND EN;
44.          Y(1)<=I(0) AND (NOT I(1)) AND EN;
45.          Y(2)<=(NOT I(0)) AND I(1) AND EN;
46.          Y(3)<=I(0) AND I(1) AND EN;
47.      end Behavioral;
```

2.3 Elaborated design schematic



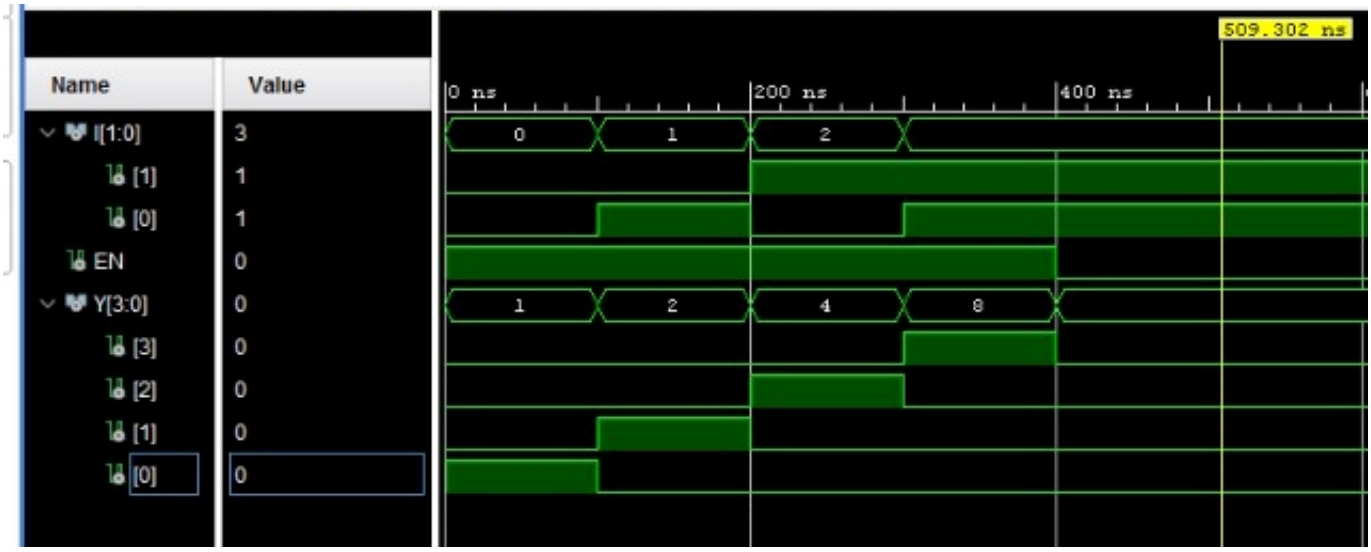
2.4 Simulation source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 02/20/2024 02:58:45 PM
-- Design Name:
-- Module Name: TB_Decoder_2_to_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Decoder_2_to_4 is
--  Port ( );
end TB_Decoder_2_to_4;

architecture Behavioral of TB_Decoder_2_to_4 is

COMPONENT Decoder_2_to_4
    Port ( I : in STD_LOGIC_VECTOR (1 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (3 downto 0));
END COMPONENT;

    SIGNAL I: STD_LOGIC_VECTOR(1 downto 0);
    SIGNAL EN: STD_LOGIC;
    SIGNAL Y: STD_LOGIC_VECTOR(3 downto 0);

begin

    UUT:Decoder_2_to_4 PORT MAP(
    I=>I,
    EN=>EN,
    Y=>Y
    );

PROCESS
BEGIN
    I<="00";
    EN<='1';

    WAIT FOR 100 NS;
    I<="01";
```

```
    EN<='1';

    WAIT FOR 100 NS;
    I<="10";
    EN<='1';

    WAIT FOR 100 NS;
    I<="11";
    EN<='1';

    WAIT FOR 100 NS;
    EN<='0';
    WAIT;

END PROCESS;


end Behavioral
```

2.5 Timing diagram



3. 3-to-8 Decoder

3.1 Truth tables and Boolean expressions

EN	I0	I1	I2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0
0	x	x	x	0	0	0	0	0	0	0	0

Y0 = I0.I1.I2

Y1 = I0.I1.I2’

Y2 = I0.I1’.I2

Y3 = I0.I1’.I2’

Y4 = I0’.I1.I2

Y5 = I0’.I1.I2’

Y6 = I0’.I1’.I2

Y7 = I0’.I1’.I2’

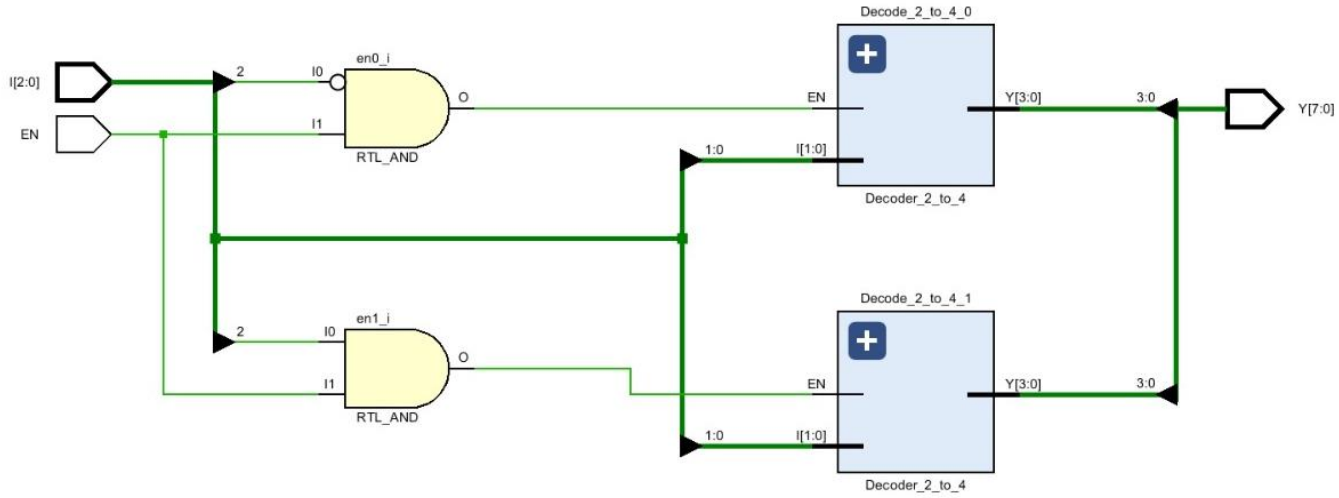
3.2 Design source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer:
--
-- Create Date: 02/20/2024 04:14:59 PM
-- Design Name:
-- Module Name: Decoder_3_to_8 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
```

```
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Decoder_3_to_8 is
    Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Decoder_3_to_8;

architecture Behavioral of Decoder_3_to_8 is

component Decoder_2_to_4
     port(
         I: in STD_LOGIC_VECTOR;
         EN: in STD_LOGIC;
         Y: out STD_LOGIC_VECTOR );
end component;

     signal I0,I1 : STD_LOGIC_VECTOR (1 downto 0);
     signal Y0,Y1 : STD_LOGIC_VECTOR (3 downto 0);
     signal en0,en1, I2 : STD_LOGIC;

begin

 Decode_2_to_4_0 : Decoder_2_to_4
     port map(
         I => I0,
         EN => en0,
         Y => Y0 );
```

```
 Decode_2_to_4_1 : Decoder_2_to_4
     port map(
         I => I1,
         EN => en1,
         Y => Y1 );

 en0 <= NOT(I(2)) AND EN;
 en1 <= I(2) AND EN;
 I0 <= I(1 downto 0);
 I1 <= I(1 downto 0);
 I2 <= I(2);
 Y(3 downto 0) <= Y0;
 Y(7 downto 4) <= Y1;



end Behavioral
```

3.3 Elaborated design schematic



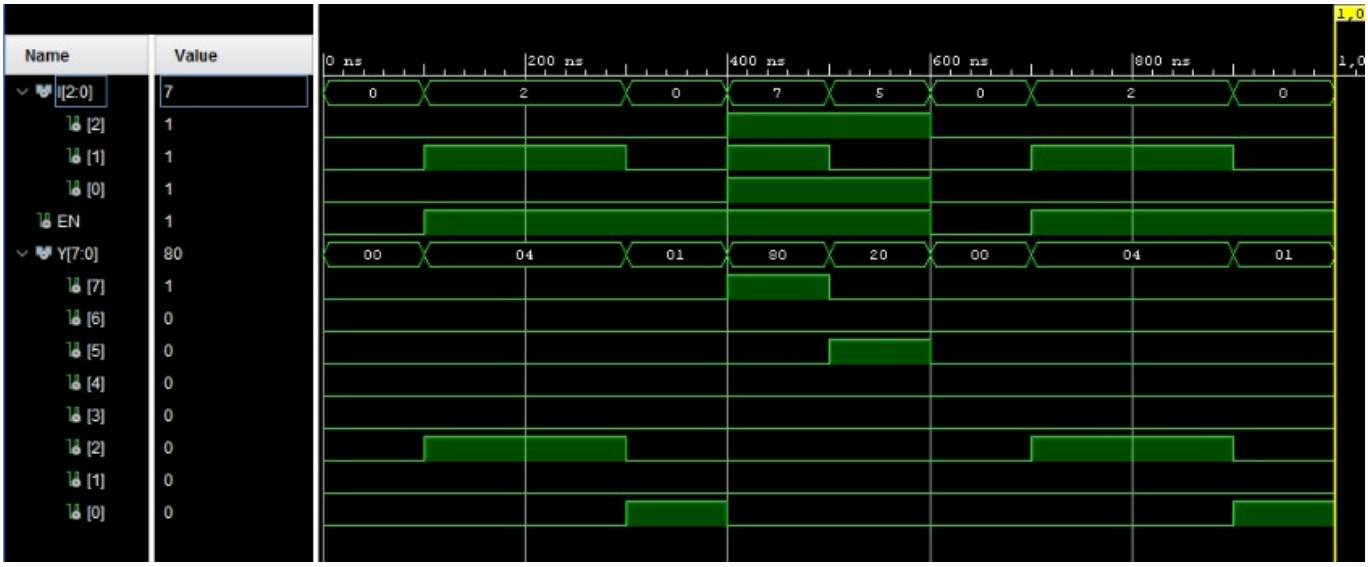
3.4 Simulation source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 02/20/2024 04:23:59 PM
-- Design Name:
-- Module Name: TB_Decoder_3_to_8 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Decoder_3_to_8 is
--  Port ( );
end TB_Decoder_3_to_8;

architecture Behavioral of TB_Decoder_3_to_8 is

component Decoder_3_to_8
     Port (  I : in STD_LOGIC_VECTOR (2 downto 0);
             EN : in STD_LOGIC;
```

```
            Y : out STD_LOGIC_VECTOR (7 downto 0));
end component;

    SIGNAL I: STD_LOGIC_VECTOR(2 downto 0);
    SIGNAL EN: STD_LOGIC;
    SIGNAL Y: STD_LOGIC_VECTOR(7 downto 0);

begin
    UUT:Decoder_3_to_8 PORT MAP(
        I=>I,
        EN=>EN,
        Y=>Y
        );

PROCESS
BEGIN
        I(0)<='0';
        I(1)<='0';
        I(2)<='0';
        EN<='0';
    WAIT FOR 100 NS;
        I(0)<='0';
        I(1)<='1';
        I(2)<='0';
        EN<='1';

    WAIT FOR 100 NS;
        I(0)<='0';
        I(1)<='1';
        I(2)<='0';
    WAIT FOR 100 NS;
        I(0)<='0';
        I(1)<='0';
        I(2)<='0';
    WAIT FOR 100 NS;
        I(0)<='1';
        I(1)<='1';
        I(2)<='1';
    WAIT FOR 100 NS;
        I(0)<='1';
        I(1)<='0';
        I(2)<='1';
    WAIT FOR 100 NS;
        I(0)<='0';
        I(1)<='1';
```

```
        I(2)<='1';
END PROCESS;

end Behavioral;
```

3.5 Timing Diagram



4. 8-1-Multiplexer

4.1 Truth tables and Boolean expressions

EN	S2	S1	S0	Y
1	0	0	0	D0
1	0	0	1	D1
1	0	1	0	D2
1	0	1	1	D3
1	1	0	0	D4
1	1	0	1	D5
1	1	1	0	D6
1	1	1	1	D7
0	x	x	x	0

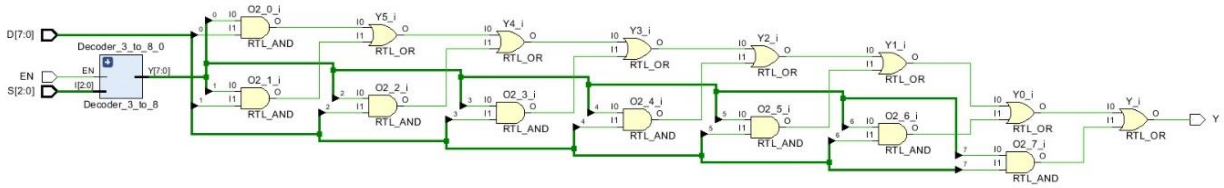
Y = S2’.S1’.S0 + S2’.S1’.S0 + S2’.S1.S0’ + S2’.S1.S0 + S2.S1’.S0’ + S2.S1’.S0 + S2.S1.S0’ + S2.S1.S0

4.2 Design source file

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer: de silva a d d t
--
-- Create Date: 02/20/2024 05:12:25 PM
-- Design Name:
-- Module Name: Mux_8_to_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Mux_8_to_1 is
    Port ( S : in STD_LOGIC_VECTOR (2 downto 0);
           D : in STD_LOGIC_VECTOR (7 downto 0);
           EN : in STD_LOGIC;
           Y : out STD_LOGIC);
end Mux_8_to_1;

architecture Behavioral of Mux_8_to_1 is
    COMPONENT Decoder_3_to_8
```

```
    Port (  I : in STD_LOGIC_VECTOR (2 downto 0);
                EN : in STD_LOGIC;
                Y : out STD_LOGIC_VECTOR (7 downto 0));
    END COMPONENT;

    SIGNAL O1,O2: STD_LOGIC_VECTOR(7 downto 0);

begin
    Decoder_3_to_8_0 : Decoder_3_to_8
    port map(
        I=>S,
        EN=>EN,
        Y => O1 );

    O2(0) <= O1(0) AND D(0);
    O2(1) <= O1(1) AND D(1);
    O2(2) <= O1(2) AND D(2);
    O2(3) <= O1(3) AND D(3);
    O2(4) <= O1(4) AND D(4);
    O2(5) <= O1(5) AND D(5);
    O2(6) <= O1(6) AND D(6);
    O2(7) <= O1(7) AND D(7);

    Y<= O2(0) OR O2(1) OR O2(2) OR O2(3) OR O2(4) OR O2(5) OR O2(6) OR O2(7)
;

end Behavioral;
```

4.3 Elaborated design Schematic



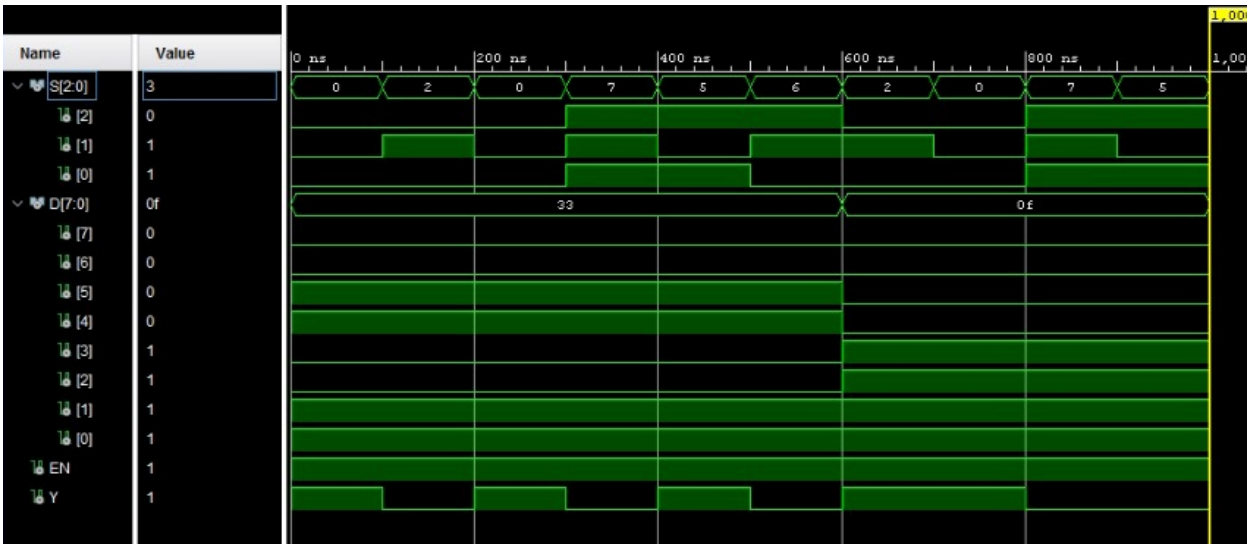
4.4 Simulated Source File

```
----------------------------------------------------------------------------------
-
-- Company:
-- Engineer: DE SILVA A D D T
--
-- Create Date: 02/21/2024 11:04:01 AM
-- Design Name:
-- Module Name: TB_Mux_8_to_1 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
-


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity TB_Mux_8_to_1 is
--  Port ( );
end TB_Mux_8_to_1;

architecture Behavioral of TB_Mux_8_to_1 is

COMPONENT Mux_8_to_1
           Port ( S : in STD_LOGIC_VECTOR (2 downto 0);
                  D : in STD_LOGIC_VECTOR (7 downto 0);
```

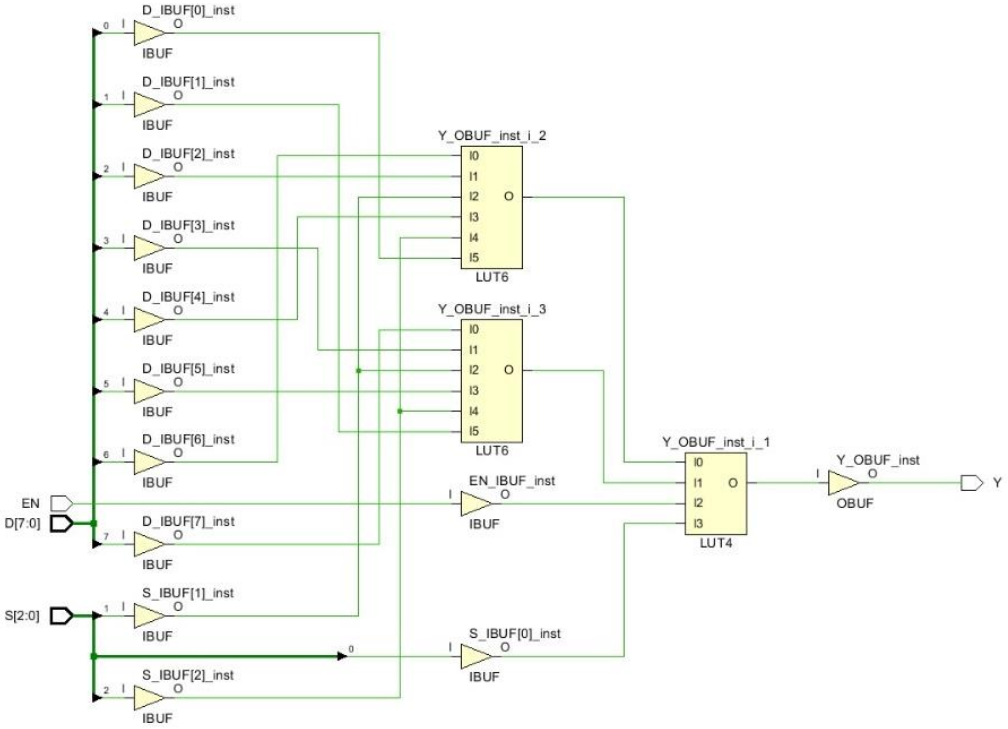
```
                  EN : in STD_LOGIC;
                  Y : out STD_LOGIC);
END COMPONENT;

        SIGNAL S : STD_LOGIC_VECTOR (2 downto 0);
        SIGNAL  D : STD_LOGIC_VECTOR (7 downto 0);
        SIGNAL  EN : STD_LOGIC;
        SIGNAL  Y : STD_LOGIC;

begin

UUT: Mux_8_to_1 PORT MAP(
    S=>S,
    D=>D,
    EN=>EN,
    Y=>Y
    );
PROCESS
BEGIN
        D<="00110011";
        S<="000";
        EN<='1';

        WAIT FOR 100NS;
        S<="010";

        WAIT FOR 100NS;
        S<="000";

        WAIT FOR 100NS;
        S<="111";

        WAIT FOR 100NS;
        S<="101";

        WAIT FOR 100NS;
        S<="110";

        WAIT FOR 100NS;
        D<="00001111";
        S<="010";

        WAIT FOR 100NS;
        S<="000";
```

```
        WAIT FOR 100NS;
        S<="111";

        WAIT FOR 100NS;
        S<="101";

        WAIT FOR 100NS;
        S<="011";

        WAIT;

END PROCESS;

end Behavioral;
```

4.5 Timing diagram



4.6 Implented design schematic



4.7 Constraints file

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top
level signal names in the project
## Switches
set_property PACKAGE_PIN V17 [get_ports {D[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[0]}]
set_property PACKAGE_PIN V16 [get_ports {D[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[1]}]
set_property PACKAGE_PIN W16 [get_ports {D[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[2]}]
set_property PACKAGE_PIN W17 [get_ports {D[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[3]}]
set_property PACKAGE_PIN W15 [get_ports {D[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[4]}]
set_property PACKAGE_PIN V15 [get_ports {D[5]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[5]}]
set_property PACKAGE_PIN W14 [get_ports {D[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[6]}]
set_property PACKAGE_PIN W13 [get_ports {D[7]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {D[7]}]
```

```
set_property PACKAGE_PIN U1 [get_ports {S[0]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[0]}]
set_property PACKAGE_PIN T1 [get_ports {S[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[1]}]
set_property PACKAGE_PIN R2 [get_ports {S[2]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {S[2]}]


## LEDs
set_property PACKAGE_PIN U16 [get_ports {Y}]
    set_property IOSTANDARD LVCMOS33 [get_ports {Y}]



##Buttons
set_property PACKAGE_PIN U18 [get_ports EN]
    set_property IOSTANDARD LVCMOS33 [get_ports EN]
```

5. Conclusion

First we designed a 2-to-4 decorder, 3-to-8 decorder. Then we designed 8-to-1 multiplexer using two 3-to-8 decorders. Finally we verified their functionality by simulating these components.