

Review Paper on AMD's Ryzen Zen architecture based Processor

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1 Introduction

Advanced Micro Devices, Inc. (AMD) is a Silicon Valley based multinational semiconductor company that develops computer processors and related technologies for business and consumer markets. While it initially manufactured its own processors, the company later outsourced its manufacturing, a practice known as going fabless, after Global Foundries was spun off in 2009. AMD's main products include microprocessors, motherboard chip sets, embedded processors and graphics processors for servers, workstations, personal computers and embedded system applications.

Ryzen is a brand^[1] of x86-64 microprocessors designed and marketed by Advanced Micro Devices (AMD) for desktop, mobile, server, and embedded platforms based on the Zen microarchitecture. It consists of central processing units (CPUs) marketed for mainstream, enthusiast, server, and workstation segments and accelerated processing units (APUs) marketed for mainstream and entry-level segments and embedded systems applications.

2 History and the Evolution

x86-64, also known as AMD64 is a 64-bit version of the x86 instruction set, first released in 1999. AMD64 was created as an alternative to the radically different IA-64 architecture designed by Intel and Hewlett-Packard, which was backward-incompatible with IA-32, the 32-bit version of the x86 architecture. Originally announced in 1999 with a full specification available in August 2000, the AMD64 architecture was positioned by AMD from the beginning as an evolutionary way to add 64-bit computing capabilities to the existing x86 architecture while supporting legacy 32-bit x86 code, as opposed to Intel's approach of creating an entirely new 64-bit architecture with IA-64.

Until Ryzen's initial launch in the spring of 2017, Intel's market dominance over AMD would only continue to increase with "Intel Core" CPU and branding, was the successful roll out of their well-known "tick-tock" CPU release strategy. This then brand new release strategy was most famous for alternating between a new CPU microarchitecture and a new fabrication node each and every year; with it being something that over time would become a release cadence they'd eventually manage to stick to for almost an entire decade specifically lasting from Intel Core's initial summer 2006 launch with 65 nm Conroe, all the way until their 14 nm Broadwell desktop CPUs were delayed a year from a planned 2014 launch out to summer 2015 instead. This would necessitate a refresh of their pre-existing 22 nm Haswell CPU lineup in the form of "Devil's Canyon", and thus officially end "tick-tock" as a practice.^{[2][3]} And it's for these same exact reasons that this became incredibly important for AMD, as Intel's inability to further sustain "tick-tock" past around 2014 would prove absolutely critical, if not downright essential in providing both the initial and continually growing market openings for their Ryzen CPUs and the Zen CPU microarchitecture in general to succeed.

Ryzen is the consumer-level implementation of the newer Zen microarchitecture, a complete redesign that marked the return of AMD to the high-end CPU market, offering a product stack able to compete with Intel at every level.^[4] Having more processing cores, Ryzen processors offer greater multi-threaded performance at the same price point relative to Intel's Core processors.^[5] The Zen architecture delivers

more than 52% improvement in instructions per cycle (clock) over the prior-generation Bulldozer AMD core, without raising power use.[6] The changes to instruction set also makes it binary-compatible with Intel’s Broadwell, smoothing the transition for users. Since the release of Ryzen, AMD’s CPU market share has increased while Intel’s appears to have stagnated or regressed.[7]

1999	•	x86-64, also known as AMD64 is a 64-bit version of the x86 instruction set, first released
1999	•	AMD Announced the AMD64 architecture
August 2000	•	Full specification of the AMD64 architecture was made available
		This was the first iteration of Zen utilized Global Foundries’ 14nm manufacturing process.[8] Ryzen and the fundamental Zen CPU microarchitecture was a completely new design and marked AMD’s return to the high-end CPU market after a decade of near-total absence since 2006.[9] This is because AMD’s primary competitor Intel had largely dominated this market segment starting from the 2006 release of their Core microarchitecture (marketed as ”Core 2”), after abandoning the Pentium 4’s extremely uncompetitive Netburst microarchitecture (with AMD’s Athlon XP in terms of price and efficiency and Athlon 64 & 64 X2 basically across the board) for an upgraded version of the prior Pentium 3, which notably continues to underpin Intel’s CPU designs to this very day.[10]
13 December 2016	•	AMD officially announced its Ryzen series of processors during the <i>New Horizon Summit</i>
February 2017	•	introduced Ryzen 1000 series processors (codenamed Summit Ridge)
2 March 2017	•	Launched Ryzen commercially [11]
E3 2016	•	Zen-based preview system was demonstrated and was first substantially detailed at an event hosted a block away from the Intel Developer Forum 2016.
Early March 2017	•	First Zen based CPUs reached the market
June 2017	•	Launch of Zen-derived Epyc server processors (codenamed ”Naples”)
November 2017	•	Launch of Zen-based APUs (codenamed ”Raven Ridge”) [12]
		This was the first iteration of Zen utilized Global Foundries’ 14nm manufacturing process. [8]

Table 1: Timeline of the Evolution and Development of the AMD Zen based Ryzen Processor

The first Ryzen 7 (1700, 1700X, and 1800X) processors debuted in early March 2017 and were generally well received by hardware reviewers.[13] Ryzen was the first brand new architecture from AMD in five years, and without very much initial fine-tuning or optimization, it ran generally well for reviewers. Initial Ryzen chips ran well with software and games already on the market, performing exceptionally well in workstation scenarios, and well in most gaming scenarios. Compared to Piledriver-powered FX chips, Zen-powered Ryzen chips ran cooler, much faster, and used less power. IPC uplift was eventually gauged to be 52% higher than Excavator, which was two full generations ahead of the architecture still being used in AMD’s FX-series desktop predecessors like the FX-8350 and FX-8370. Though Zen fell short of Intel’s Kaby Lake in terms of IPC, and therefore single-threaded throughput, it compensated by offering more cores to applications that can use them. Power consumption and heat emission were found to be competitive with Intel, and the included Wraith coolers were generally competitive with higher-priced aftermarket units. Ryzen 1800X’s multi-threaded performance, in some

cases while using Blender or other open-source software, was around four times the performance of the FX-8370, or nearly double that of the i7 7700K.[14] One reviewer found that Ryzen chips would usually outperform competing Intel i7 processors for a fraction of the price when all eight cores are used.[14] However, one complaint among a subset of reviewers was that Ryzen processors lagged their Intel counterparts when running older games, or some newer games at mainstream resolutions such as 720p or 1080p.[15] AMD acknowledged the gaming performance deficit at low resolutions during a Reddit "Ask Me Anything" thread, where it explained that updates and patches were being developed.[16] Subsequent updates to Ashes of the Singularity: Escalation and Rise of the Tomb Raider increased frame rates by 17–31% on Ryzen systems.[17][18] In April 2017, developer id Software announced that, in the future, its games would exploit the greater parallelism available on Ryzen CPUs.[19]

3 Processor Architecture, Structure and Classification

The Zen microarchitecture is used in the commercially branded Ryzen CPU and APU. It makes use of the AMD64(x86-64) instruction set and is discussed in further sections.

3.1 Fabrication Process

The Zen microarchitecture uses 14nm FinFet[20] [21] (Fin Field Effect Transistors) process whereas Intel and other competitors use the bulldozer architecture. This technology ensures power efficiency and larger instructions per cycle rate. The latter variants such as Zen 2 and 3 use a 7nm transistor. Smaller transistors ensure less current consumption at the same voltage or frequency compared earlier 28nm architecture used in AMD's Excavator.

3.2 Memory Hierarchy

The Zen based processors support DDR4 memory up to 8 channels and Error Correction Code (ECC).[22]

Cache Organization

- **L0 μ OP cache** : 2,048 μ OPs, 8-way set associative
- **L1I Cache** : 64 KiB 4-way set associative
- **L1D Cache** : 32 KiB 8-way set associative
- **L2 Cache** : 512 KiB 8-way set associative
- **L3 Cache** : Victim Cache

L1 Cache follows write back policy.

3.3 Core Engine

The Zen architecture suggests 2-4 cores for mobile and 4-8 cores for desktop microprocessors, while supporting 32+ cores for servers. Each core can decode four instructions per clock cycle and has an micro-op cache that feeds into two schedulers one for floating point and other for integer segments. Simultaneous Multithreading was introduced in this architecture, which allows each core to have 2 threads. This was an improvement on previous AMD architecture designs with larger op cache, larger schedulers and improved branch prediction.[23]

3.4 Pipeline

Each Ryzen core has 1 floating point and integer unit. The integer unit has 6 pipes, 4 ALU'S (Arithmetic and Logical Unit) and 2 AGU'S (Address Generation Unit). The AGU'S can perform two 16 byte load and one 16 bit store operation in each clock cycle using the L1 cache. Two of the floating point units are adders, two multiply-adders.[24]

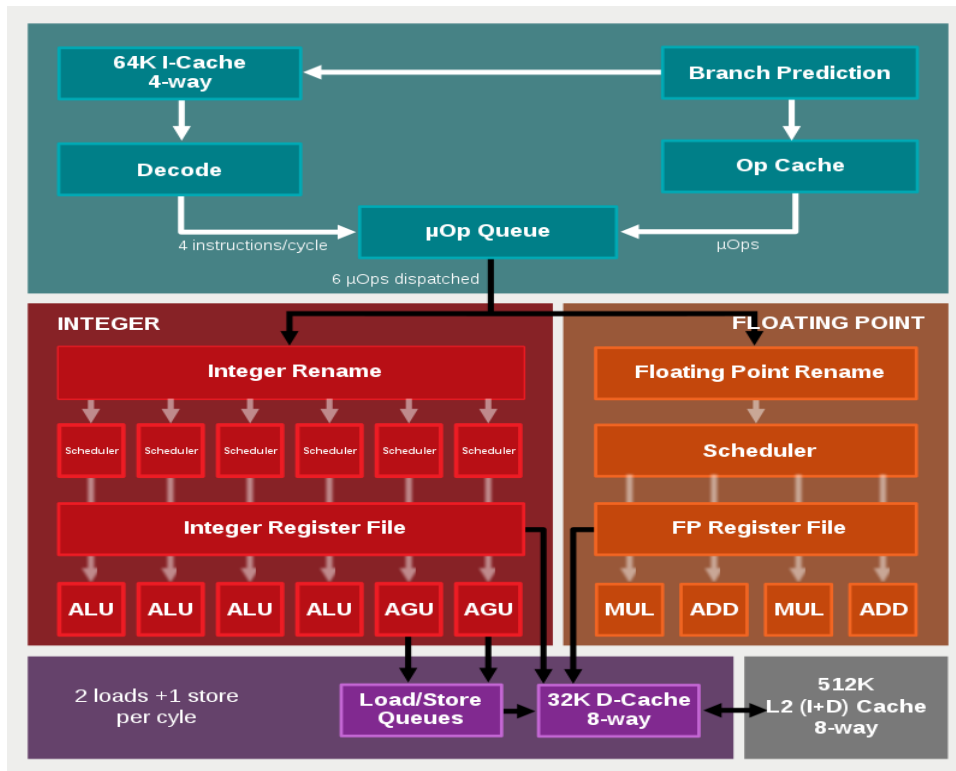


Figure 1: Image showing a single Zen architecture's core organization

3.5 Clock Domains

Zen microarchitecture is divided into various clock domains as follows, operating at various frequencies.[25]

- **UMC Clock:** The frequency at which Unified Memory Controller operates. The value is close to memory clock.
- **Link Clock:** The frequency at which Input and Output Hub controller operates with the chip.
- **Fabric Clock:** The frequency at which data fabric operates at and is similar to the memory clock.
- **Memory Clock:** Internal and External memory clock.
- **Core Clock:** Frequency at which CPU Core and Cache operate.

3.6 Sockets and Connectivity

The CPU's which run on Zen microarchitecture supports the AM4 socket, TR4 socket and SP3 socket.[23] The use of AM4 socket ensures DDR4 support. The server processors range uses the SP3 socket to support 8 channel DDR4. The zen architecture is based on the SoC (System on chip) design. The USB, SATA and memory controllers are integrated on the same chip site.[23]

4 Instruction Set

AMD Ryzen is built on AMD's 64-bit technology which includes the x86-64-bit architecture, which is a 64-bit extension of the x86-architecture.

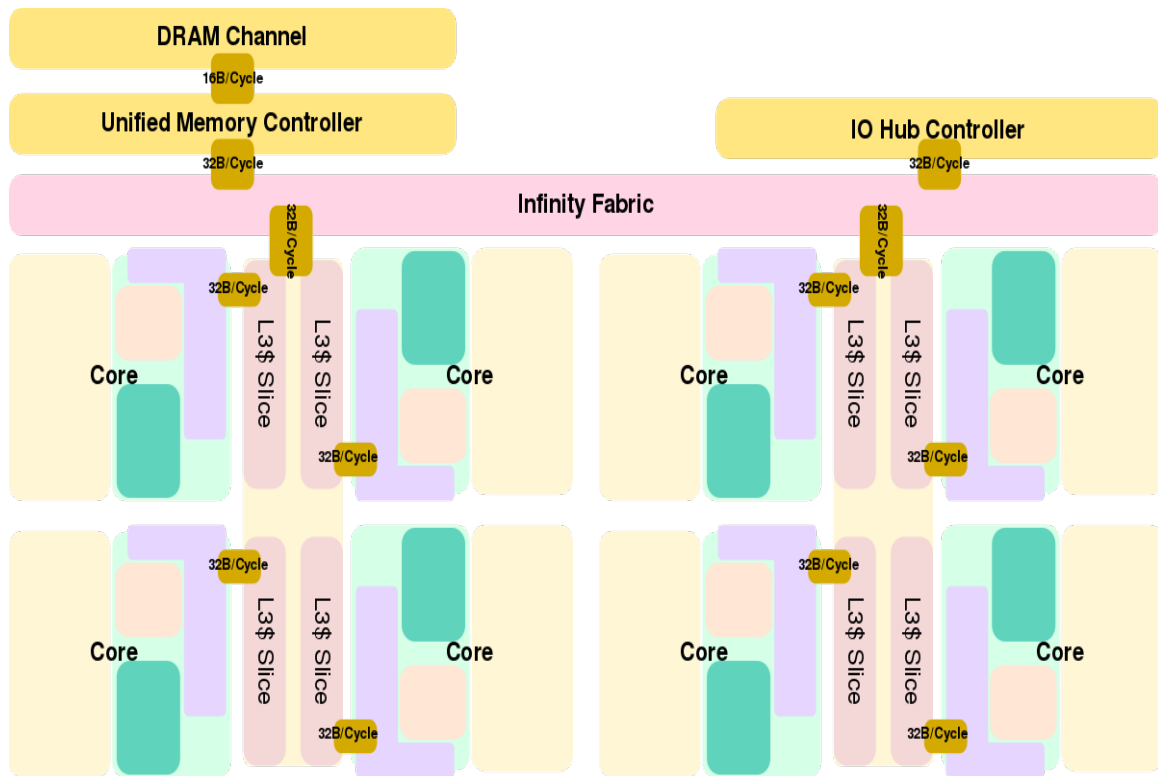


Figure 2: Image showing SoC (System on Chip) block of Zen architecture

4.1 General Purpose Programming

4.1.1 Registers

The AMD64 architecture has a total of 16 general purpose registers (upgraded from the existing 8) which may be used in the legacy 8 bit and 16 bit mode (addressed as AL and AX respectively), the 32 bit compatibility mode or the original mode (addressed as EAX or RAX respectively).

4.1.2 Flags Register and CMP instruction

The 64 bit RFLAGS register is visible to software. The CMP instruction performs subtraction of the second operand (source) from the first operand (destination), like the SUB instruction, **but it does not store the resulting value in the destination operand**. It leaves both operands intact. The only effect of the CMP instruction is to set or clear the arithmetic flags (OF, SF, ZF, AF, CF, PF) according to the result of subtraction.

Code Sample 1

```

1      cmp ecx, 5 ; test if
    ecx equals 5
2      jnz Continue ; test
    condition and skip if not met
3      mov eax, ebx ; move
4      Continue: ;
    continuation
5

```

```

1      cmp ecx, 5 ; test if
    ecx equals to 5
2      cmovz eax, ebx ; test
    condition and move
3

```

This example elucidates use of the compare statement in conjunction with the RFLAGS register and of the conditional move (CMOVcc) statements. The advantage of CMOVcc statements, apart

register encoding		high 8-bit	low 8-bit	16-bit	32-bit
0		AH (4)	AL	AX	EAX
3		BH (7)	BL	BX	EBX
1		CH (5)	CL	CX	ECX
2		DH (6)	DL	DX	EDX
6		SI		SI	ESI
7		DI		DI	EDI
5		BP		BP	EBP
4		SP		SP	ESP
		31	16 15		0
		31			0
		FLAGS		FLAGS	EFLAGS
		IP		IP	EIP
		31			0

Figure 3: General Registers in Legacy and Compatibility Modes (Figure 3-2. [26])

from cleaner code is it avoids branch prediction penalties caused by conditional jumps.

4.1.3 Stack Operations

The POP, POPA (POP all to GPR), POPAD (POP all to GPR double words), PUSH, PUSHA, PUSHAD statements are used to pop values from the stack and store them into the GPRs (General Purpose Registers) and push them from the GPRs to the stack. rBP and rSP registers are used as the stack base pointer and the stack reference pointers respectively.

4.1.4 Data Conversion

The **ASCII Adjust Instructions** AAA, AAD, AAM, AAS (ASCII Adjust after addition, division, multiplication and subtraction) apply corrections on non packed BCD values (i.e., when the BCD is stored in a byte register) such as passing the carry of one digit to the next digit. The **BCD** counterparts perform corrections (addition and subtraction only - DAA and DAS) on packed BCD values (thetwo nibbles in a byte represent two digits).

1. The *MUL* instruction takes only one operand (multiplicand) which is a factor and the result is stored in the same register which is treated as an accumulator. Note that AL, AX and rAX refer to the same GPR and use a different combination of its bits. One will be required to initialise AX (AL or rAX) with the first factor before beginning the multiplication operations.
2. Division is the slowest of all integer arithmetic operations and should be avoided wherever possible. Possibly by replacing $i/j/k$ with $i/(j * k)$

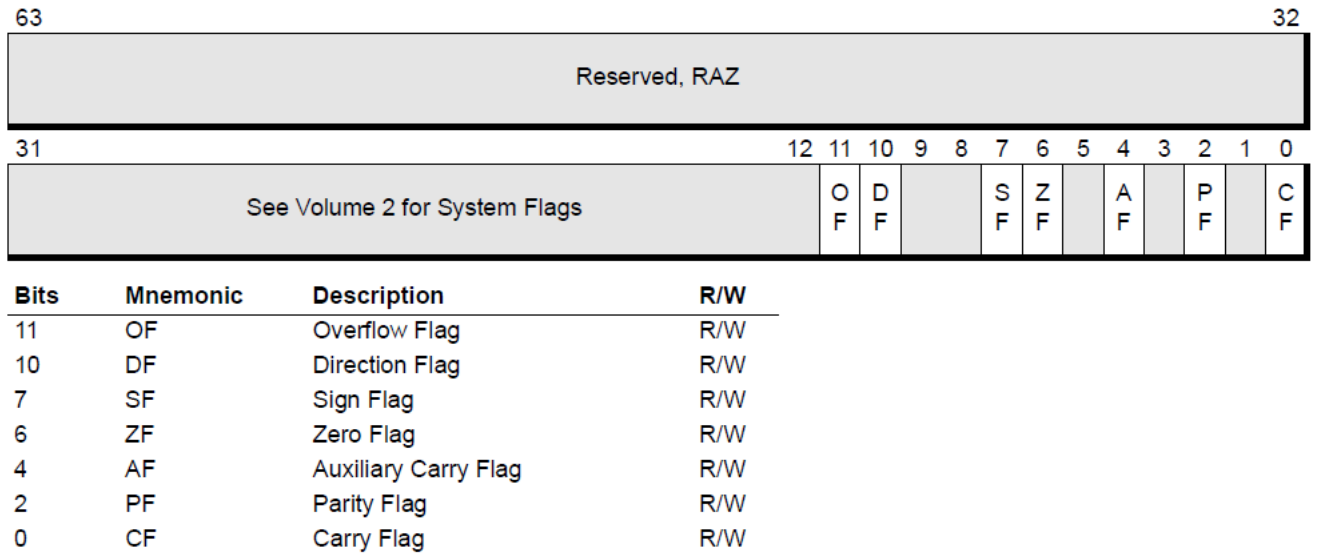


Figure 4: rFLAGS Register—Flags Visible to Application Software (Figure 3-5. [26])

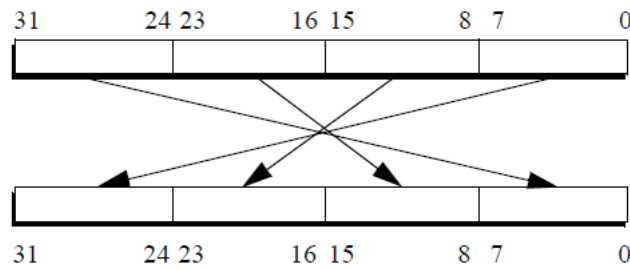


Figure 5: BSWAP Doubleword Exchange used in converting between Little Endian and Big Endian, Figure 3-8. [26]

3. The increment (INC) and decrement (DEC) instructions are identical to the ADD and SUB instructions except in that they do not affect the Carry flag (0 bit of the RFLAGS register).
4. The **Rotate (and Shift)** instructions perform cyclic (or non-cyclic) rotations of the operand by *count* number of bits. The last bit to be rotated out is stored in the *Carry Flag - CF*. In single left bit rotates, the *Overflow flag - OF* is set to *CF XOR (MSB of result)*. In single right bit rotates, the *Overflow flag - OF* is set to *2nd MSB of result XOR (MSB of result)*. Bit rotations are used in character conversion including cryptography techniques. SAR (shift Arithmetic Right) ignores (preserves) the MSB and flushes out the (2nd MSB) instead.

4.1.5 Bit Manipulation

Bit manipulation instructions manipulate individual bits in a register for purposes such as controlling low-level devices, correcting algorithms, and detecting errors.

1. BEXTR (Bit Field extract) is used to extract a contiguous field of bits

4.1.6 SETcc - Conditional SET

The conditional set instructions set the byte operand to 0 or 1 depending on the condition (by reading the RFLAGS bits) based on conditions as can be found in Table 3-5 in [26].

Operand size	Multiplicand	Result
Byte	AL (8 bit)	AX (16 bit)
Word	AX	rDX and rAX (64 bits each)
Doubleword	AX	rDX and rAX
Quadword	AX	rDX and rAX

Table 2: The register reference used for the MUL instruction based on the operand size

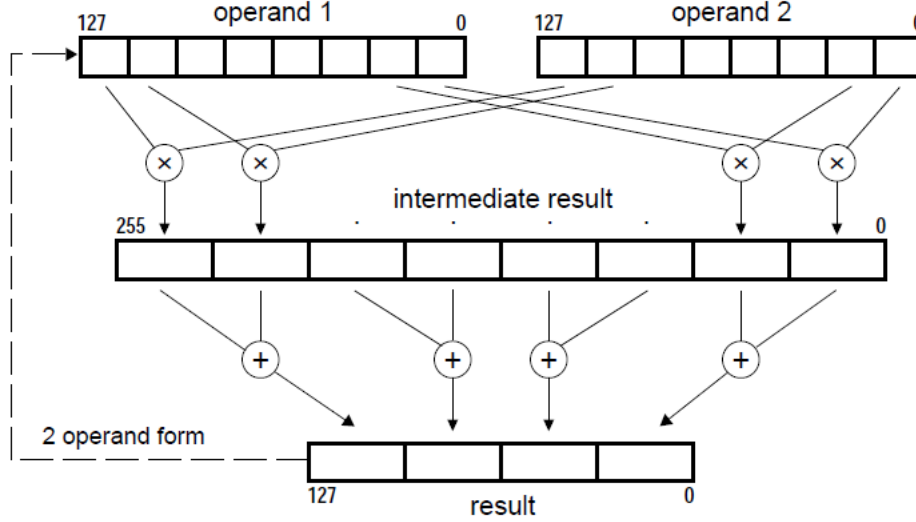


Figure 6: (V)PMADDWD Multiply-Add Operation (Figure 4-35. [26])

4.1.7 Cache and Memory Management

The (L/S/M)FENCE (load/store/memory) instructions force orders on memory access.

4.2 SSE Instructions

The Streaming SIMD (Single Instruction Multiple Data) instructions speed up common operations by passing multiple byte data into a single 128-bit XMM or 256-bit YMM register and executing a single instruction on these. An example is the dot product (VPMADDWD - Vector Packed Multiply Words and Add Doublewords) shown below. This computes the dot product of 8 2-vectors with X coordinates in YMM0 and Y coordinates in YMM1 and stores in the destination (first) operand.

Code Sample 2

```

1  MOV YMM0, 0x11112222333344445555666677778888
2  MOV YMM1, 0x11112222333344445555666677778888
3  VPMADDWD YMM0, YMM1

```

The following code multiplies 8 32-bit integers of the 8-tuple YMM0 with the corresponding entries of the YMM1.

```

1  MOV YMM0, 0x11112222333344445555666677778888
2  MOV YMM1, 0x11112222333344445555666677778888
3  VPMULLD YMM0, YMM1

```


5 Applications

5.1 Specific Application

AMD's Ryzen chips are popularly used in the domain of gaming. While the GPU accelerates the creation and rendering of images, videos and animations, the CPU handles the I/O operations, basic arithmetic and logic. The CPU is just as vital to gaming as the GPU, and a CPU bottleneck could occur when the processor isn't powerful enough to handle the incoming data from a powerful GPU.[27] [28]

Clock speed, cores and threads are the main considerations to look for in a CPU before using it for gaming. Clock speed tells how fast the CPU can complete tasks. The higher it is, the computer completes tasks faster. Cores are basically processors, and allow the flow of information to move faster, the higher in number they are, and thereby give greater performance. Virtual components that divide the cores within a processor are called threads, which allow them to share the workload between them and thus speed up performance.[27] [28]

Ryzen processors offer plenty of threads and great gaming performance while being cost-effective. They are grouped into 4 distinct series, namely, Ryzen 3, Ryzen 5, Ryzen 7 and Ryzen 9. Each of them have their own specialities and use cases based on their specifications.[29]

Ryzen 3 is a budget-friendly model of the processor. These are quad-core processors, and can be used for low intensity (casual) gaming, and can handle basic use cases with ease.[29]

Ryzen 5 is a mid-range processor which does better at gaming owing to the fact that it is equipped with 6 cores and 12 threads.[29]

The Ryzen 7 and Ryzen 9 are top tier processors that can support hardcore gaming with upto 12 cores and 24 threads. Paired with high end GPUs, they can reach clock speeds upto 4.5 GHz and 4.7 GHz respectively.[29]

Applications well-suited to the SSE programming model include a broad range of audio, video, and graphics programs apart from gaming. For example, music synthesis, speech synthesis, speech recognition, audio and video compression (encoding) and decompression (decoding), 2D and 3D graphics, streaming video (up to high-definition TV), and digital signal processing (DSP) kernels are all likely to experience higher performance using SSE instructions than using other types of instructions in AMD64 architecture. [26]

The SSE instructions also support a broad spectrum of scientific applications. For example, their ability to operate in parallel on double-precision floating-point vector elements makes them well suited to computations like dense systems of linear equations, including matrix and vector-space operations with real and complex numbers. In professional CAD applications, for example, high-performance physical-modeling algorithms can be implemented to simulate processes such as heat transfer or fluid dynamics. [26]

As an example, "It (the Vector packed multiply and add instruction) can also be used together with a vector-add operation to accumulate dot product results (also called inner or scalar products), which are used in many media algorithms such as those required for finite impulse response (FIR) filters, one of the commonly used DSP algorithms." [26]

5.2 Support for existing 32-bit and 16-bit applications

The Ryzen processors employ a 64 bit architecture which runs on a long mode with two submodes: the 64-bit mode with a flat 64-bit address space and a compatibility. Existing 32-bit application binaries run without recompilation in the 64 bit mode. The compatibility mode allows 64-bit operating systems

to run 16-bit and 32-bit applications without recompilation Legacy x86 instruction prefixes toggle between 16-bit and 32-bit address and operand sizes. As with 64-bit mode, compatibility mode is enabled by the operating system on an individual codesegment basis.

6 Discussions and Conclusion

The AMD processor family dominates the gaming processor market and the AMD Ryzen processors are the flagship product of AMD processor range. The architecture allows for better and faster cache access and better power efficiency. The increased number of cores and simultaneous multithreading give it a greater performance and have set a standard for the gaming industry. As is evident from the vast instruction sets, the processors serve a variety of use cases and are rightly categorised as General Purpose Processors in all price ranges. It also forced competitors such as Intel to improve their technologies and pushed the competition ahead, thus improving the future of processor technologies.

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