RESUME

Sagar Shah

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Professional Experience:

- 3 years of experience in ASIC Verification.
- Functional Verification of design at IP level using SV-UVM.
- Experience of developing Verification IP (VIP).
- Experience of dynamic low power verification using UPF.

Professional Skills:

HDL	:	Verilog, VHDL.
HVL	:	System Verilog
Methodology	:	UVM
Programming Language	:	C, C++.
Protocol knowledge	:	SATA(DL), MIPI D-PHY, I2C, MIPI SLIMbus
Power intent standard	:	UPF
Scripting	:	Shell
EDA Tools	:	VCS-MX, Questa-sim, NCSIM
Operating System	:	Windows, Linux.
Revision Control Tool	:	CVS, SVN, Perforce

Experience:

- Working as an ASIC Verification Trainee Engineer at eInfochips From December 2013 to June 2014.
- Working as an ASIC Verification Engineer at eInfochips From June 2014 to September 2016.
- Working as an ASIC Senior Verification Engineer (Level 1) at eInfochips since October 2016.

Projects:

Project #1

Project	**MIPI SLIMbus (v2.0) VIP Development**
Role	Team Member
Platform	System Verilog, UVM
Tool	VCS-MX, Questa-sim, NCSIM
Duration	Since May, 2016

Responsibility:

- Created verification environment structure.
- Created top module files for different topologies and including dynamic change/pause of clock and active framer handover support.
- Created basic transaction sequences and generic APIs for
  - Messages
  - Transport protocols
- Developed Test-plan for Frame layer, Message protocol and Transport protocols (Isochronous, Pushed, Pulled and Asynchronous).
- Implemented test-cases for all mentioned categories mentioned above and debugged it.

Project #2

Project	**Dynamic Low Power Verification**
Role	Team Member
Team Size	4
Platform	UPF, System Verilog, VHDL
Tool	VCS-MX (MVSIM/NLP)
Duration	6 Months

Responsibility:

- Developed Test-plan for below mentioned categories for Verilog design and MX design.
  - Isolation
  - Retention
  - Corruption
  - Different design attributes
  - Port attributes
- Implemented test-cases for all mentioned categories mentioned above and debugged it.

Project #3

Project	**SATA VIP Development**
Role	Team Member
Team Size	8
Platform	System Verilog, UVM
Tool	Questa-Sim
Duration	10 Months

Responsibility:

- Created basic verification environment structure.
- Developed packet creation logic from sampled data stream.
- Physical Layer:
  - Implement power mode features.
  - Defining functional coverage and achieve agreed coverage.
- Link Layer:
  - Coded FSM for Link layer (Primitive support).
  - Implemented Power mode features.
  - Implemented Error injection support.
  - Defining Test-plan for Link layer (which covers all Primitive) and Power mode.
  - Test-case writing and verification of Link layer; also to verify erroneous scenarios.
- Defining functional coverage and achieve agreed functional coverage.

Project #4

Project	**Microblaze processor based SoC verification**
Role	Team Member
Team Size	5
Platform	System Verilog, UVM
Tool	Questa-Sim
Duration	4 Months

Responsibility:

- Creating Environment for Unit Level Testing.
- I2C Unit Level Verification:
  - Defining Test plan, which covers basic scenarios of I2C protocol.
  - Defined Verification Architecture.
  - Developed verification environment.
  - Developed test-cases and debugged the RTL using it.
  - Implemented and Achieved agreed functional coverage.
  - Achieve agreed code coverage.

Project #5

Project	**MIPI D-Phy VIP Development**
Role	Team Member
Team Size	4
Platform	System Verilog, UVM
Tool	VCS
Duration	4 Months

Responsibility:

- Creating basic verification Environment structure.
- Developed test-cases and debugged the VIP using it.
- VIP Component Development:
  - Transaction Class,
  - Configuration Class,
  - Scoreboard.
- Developed Shell script and Makefile for test-case run-flow.
- Handling regression management.

Educational Qualification:

- **Bachelor of Engineering** in **Electronics & Communication**, from Vishwakarma Government Engineering College, Ahmedabad, Gujarat Technological University (2009 - 2013) with CGPA of 8.31 (7.78 CPI).
- **H.S.C** with 83% (89% merit) from G.S.E.B (2009)
- **S.S.C** with 84.92% from G.S.E.B (2007)

Personal Information:

Full Name	:	Sagar Shashikant Shah
Date of Birth	:	5th Feb, 1992
Nationality	:	Indian
Sex	:	Male
Marital Status	:	Married
Linguistics known	:	Gujarati, Hindi, English
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Hometown	:	Ahmedabad