NC State University

Department of Electrical and Computer Engineering

ECE 463/563: Fall 2019

Project #3: Dynamic Instruction Scheduling

by

SIDHARTH MEHTA

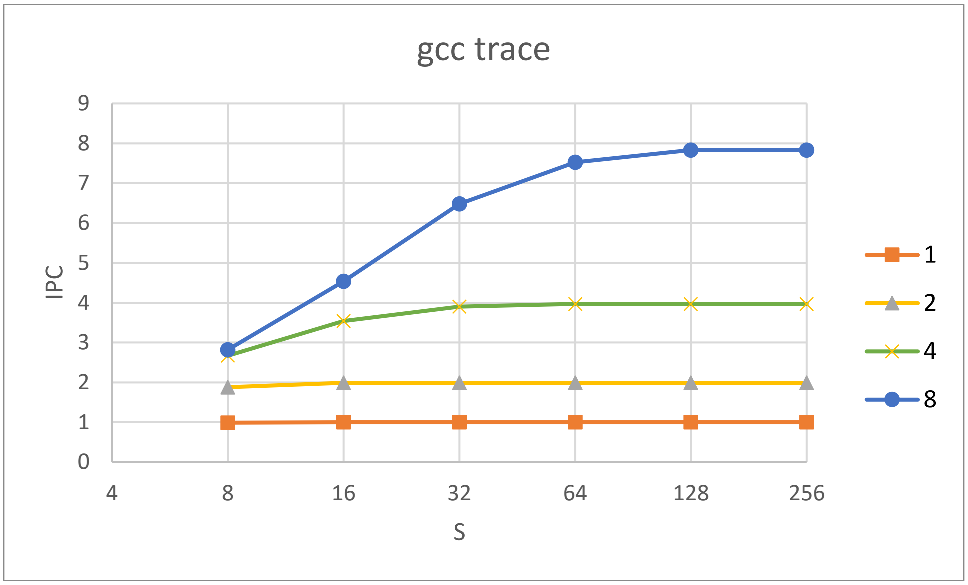
NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: __Sidharth Mehta_____________

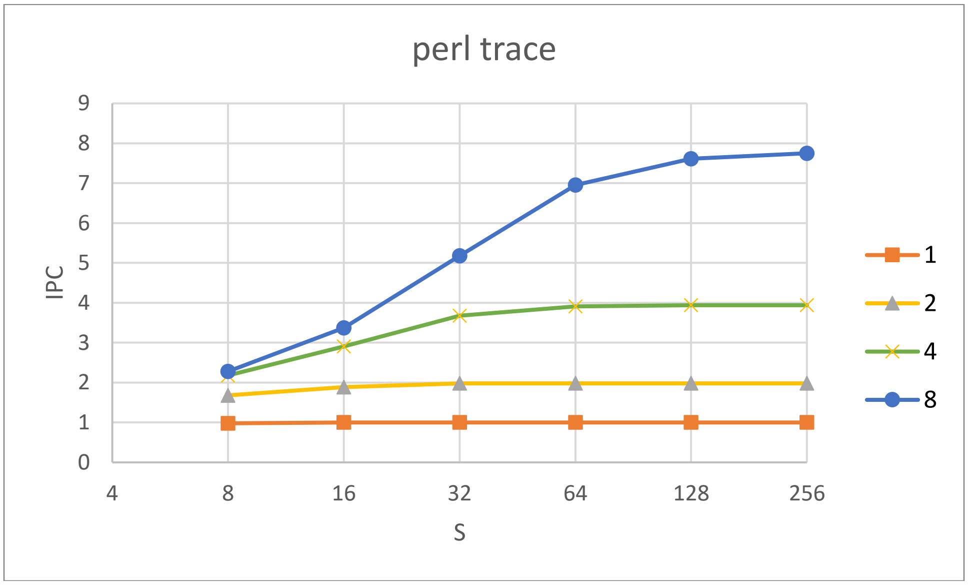
Course number: ______563___________

Graphs

GCC Trace



PERL Trace



Trends

1. Increasing N results in an increased IPC. This is mainly due to a greater number of instructions that are fetched and hence scheduled in a cycle.
2. N > S gives no benefit in IPC as scheduling queue becomes bottleneck.
3. Increasing S results in an increased IPC till a point after which results are diminished. Diminishing returns are due to the fixed number (N) of instructions that can be fetched in a cycle. And the maximum IPC achieved is equal to N.
4. Suppose only 1 instruction can be dispatched in a cycle and only 1 instruction can begin execution in a cycle. An instruction can take a maximum of 5 cycles to execute. Let the instruction which enters in the scheduling queue be a dependent instruction. To achieve peak performance, it must be ensured that 1 instruction is executed every cycle. For this we must ensure that the scheduling queue is sufficiently large. Thus, S should be 5 times (/execution latency) N for peak performance.

GCC Trace v/s PERL Trace

GCC Trace has a higher IPC than Perl Trace at lower values of N which suggests that PERL Trace has larger number of dependent instructions.