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Dinesh Gaitonde

Executive Summary

- Over 20 years experience in the semiconductor industry
- Several patents and publications in
  - FPGA Fabric and NoC Architecture
  - EDA algorithms for physical design in ASICs and FPGAs
  - Static Timing Analysis, Delay Calcuation
  - Performance Evaluation of fabric and fabric adjacent SoC blocks

Employment Experience

AMD (Senior Fellow, 2022/06 - present)

- Next Generation Fabric Architectures – Microarchitecture and performance evaluation
- Reducing pessimism in methodologies to squeeze more PPA from products
- Extending performance evaluation to more heterogenous platforms and newer workloads
- Toolchains to manage the heterogenous integration at device and package levels of next gen platforms
- Define market leading product offerings at next generation in terms of PPA
- Align architectures with future algorithm and other tool capabilities
- Predict architecture capabilities with better accuracy, and close the loop with product deliverables
- Permit competitive use of FPGAs in more domains via heterogenous integrations

Xilinx (Distinguished Engineer, 2015/01 - 2022/06)

- Managed teams across geographies responsible for
  - AMD/Xilinx FPGA fabric architectures and its PPA since Virtex7 (28nm)
  - Routability estimation, congestion alleviation, robust architecture definition
  - Industry first product programmable Network on Chip in Xilinx's Versal ACAP
  - Algorithms for routing over a NoC with minimal congestion
  - Performance characteristics of network over programmable NoC
  - Defining algorithms for large capacity FPGAs implemented using 2.5D integration

Xilinx (Principal Engineer, 2005/08 - 2015/01)

- Part of team that rearchitected Xilinx's design suite into current toolsuite Vivado
- Introduced state-of-the-art physical design algorithms into Xilinx implementation suite
- Responsible for congestion estimation and alleviation during implementation

Synopsys (Sr. Staff Software Engr, 2003/10 - 2005/08)

- Part of the original team for physically aware synthesis - DC-Topo product

Monterey Design Systems (MTS, 1998/04 - 2003/10)

- Placement, Physical Synthesis
- Design Analysis

Motorola Inc. (Staff Software Engineer, 1995 - 1998)

- Power estimation and optimization
- Library characterization
- Delay calculation
- Static noise analysis

Educational Qualifications

Ph.D. Electrical Engineering (Carnegie Mellon, 1995)

- Yield optimizat1ion & prediction. Design for manufacturability.

M.Tech. Electrical Engineering (IIT Bombay, 1990)

- Graph algos for efficient circuit simulation. Numerical algorithms.

B.Tech. Electrical Engineering (IIT Bombay, 1988)

Patents & Publications

Google Scholar Profile Link