CSCI 592
LAB ASSIGNMENT – 10

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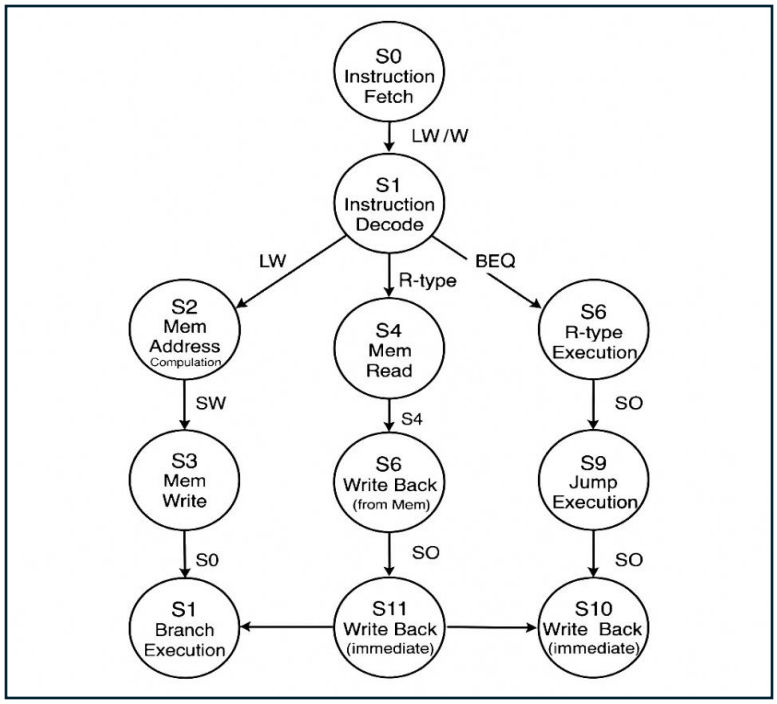
Finite State Machine Diagram



Control Signals for Each State:

State	PCWrite	MemRead	MemWrite	IRWrite	RegDst	MemtoReg	RegWrite	ALUSrcA	ALUSrcB	ALUOp	PCSource
S0 (Instruction Fetch)	1	1	0	1	X	X	0	0	01	00	00
S1 (Instruction Decode)	0	0	0	0	X	X	0	0	11	00	00
S2 (Memory Address Computation)	0	0	0	0	X	X	0	1	10	00	00
S3 (Memory Read - LW)	0	1	0	0	X	X	0	0	00	00	00
S4 (Memory Write - SW)	0	0	1	0	X	X	0	0	00	00	00
S5 (Memory Read → Register Write - LW)	0	0	0	0	0	1	1	0	00	00	00
S6 (Execute ALU Operation - R-type)	0	0	0	0	X	X	0	1	00	10	00
S7 (Write-back ALU Result - R-type)	0	0	0	0	1	0	1	0	00	00	00
S8 (Branch Completion - BEQ)	0	0	0	0	X	X	0	1	00	01	01

State	PCWrite	MemRead	MemWrite	IRWrite	RegDst	MemtoReg	RegWrite	ALUSrcA	ALUSrcB	ALUOp	PCSource
S9 (Jump Completion - JUMP)	1	0	0	0	X	X	0	0	00	00	10
S10 (Immediate Execution - ADDI)	0	0	0	0	X	X	0	1	10	00	00
S11 (Immediate Write-Back - ADDI)	0	0	0	0	0	0	1	0	00	00	00

Control signals to Boolean equations

Control Signal	Boolean Equation
PCWrite	(State = S0) + (State = S9)
MemRead	(State = S0) + (State = S3)
MemWrite	(State = S4)
IRWrite	(State = S0)
RegDst	(State = S7)
MemtoReg	(State = S5)
RegWrite	(State = S5) + (State = S7) + (State = S11)
ALUSrcA	(State = S2) + (State = S6) + (State = S8) + (State = S10)
ALUSrcB[1]	(State = S1) + (State = S2) + (State = S10)
ALUSrcB[0]	(State = S0) + (State = S1) + (State = S2)
ALUOp[1]	(State = S6)
ALUOp[0]	(State = S8)
PCSource[1]	(State = S9)
PCSource[0]	(State = S8)

State Equations:

State	y3 y2 y1 y0
S0 (Instruction Fetch)	0000
S1 (Instruction Decode)	0001
S2 (Mem Address Computation)	0010
S3 (Mem Read)	0011
S4 (Mem Write)	0100
S5 (Mem Read → Register Write)	0101
S6 (Execute ALU - R-type)	0110
S7 (Write-Back R-type)	0111

State	y3 y2 y1 y0
S8 (Branch Completion)	1000
S9 (Jump Completion)	1001
S10 (Execute Immediate)	1010
S11 (Write-Back Immediate)	1011

Programmable Logic Array diagram