

# Allegro Design Entry CIS L Tutorial

Rochester Institute of Technology

Digital Electronics EEEE-380

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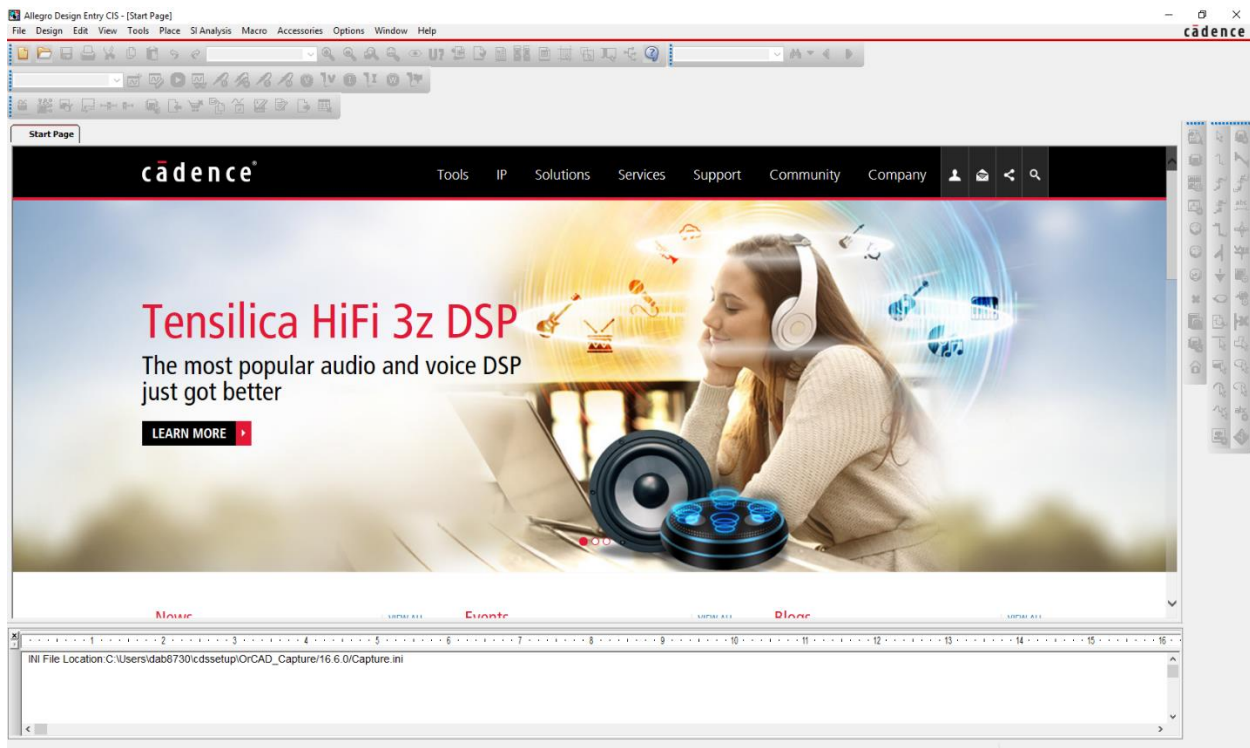
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## Overview:

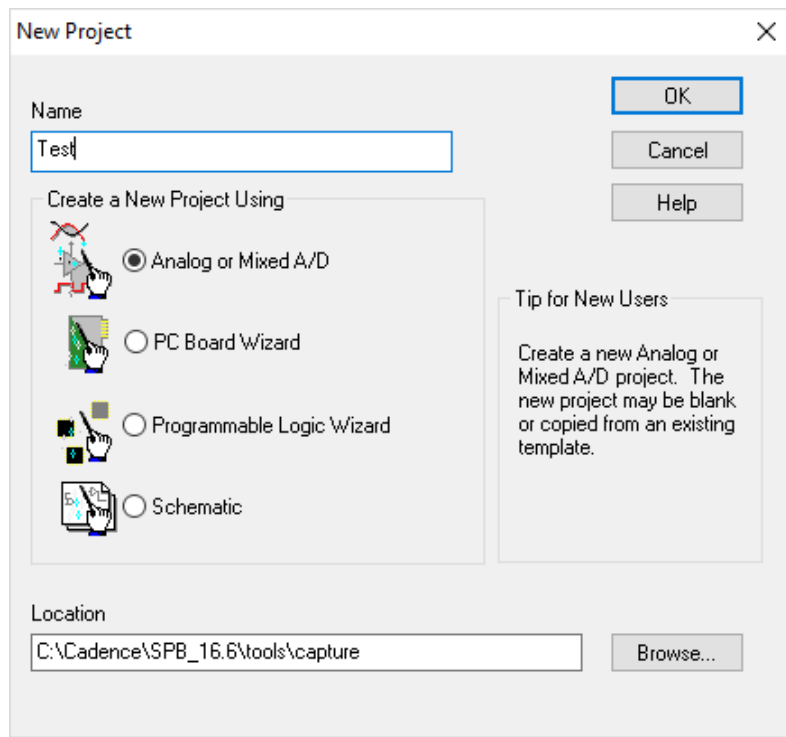
Cadence Allegro Design Entry CIS integrates a proven schematic-design-entry system with a robust component information system (CIS). Whether used to design a new analog circuit, revise a schematic diagram for an existing PCB, or design a digital block diagram with an HDL module, Allegro Design Entry CIS allows designers to enter, modify, and verify the PCB design. It also promotes reuse of preferred components and known good-part data.

## System setup:

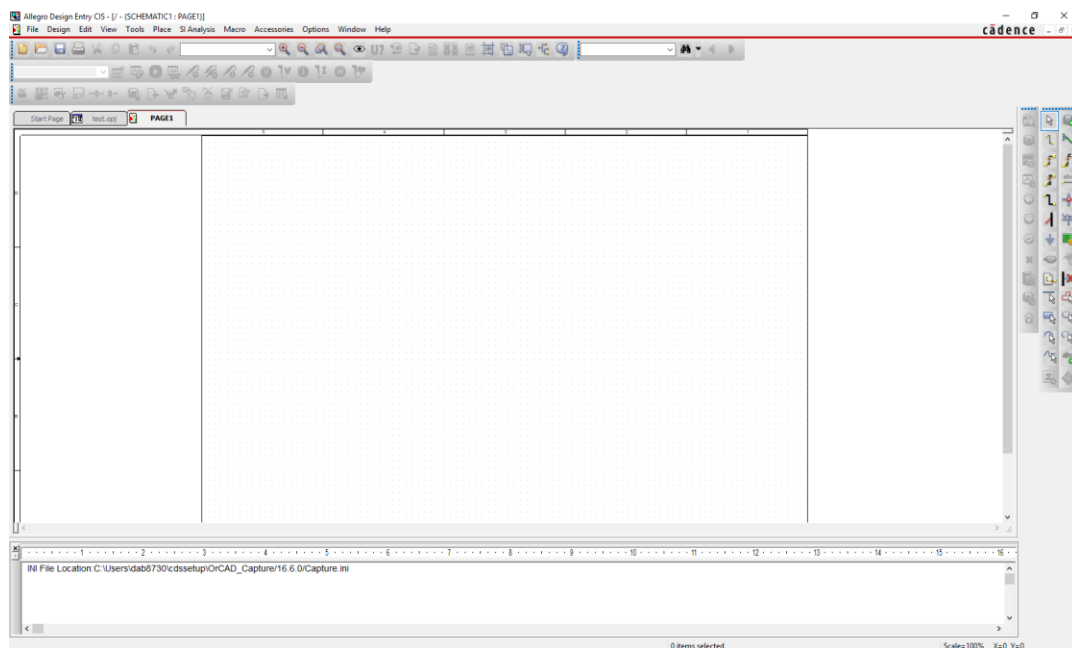
- To open allegro please follow the steps, (Start) ==> Cadence ==> Design Entry CIS ==> Allegro PCB Design CIS L.



- Select File-> new-> new project -> Analog or Mixed A/D. Enter the name of the project and click OK.



- You will be directed to your workspace.



- You can find all the required components here, Place-> Pspice Components.

- 1- Passive ( R,L,C)
- 2- Discrete (Diode families)
- 3- Source ( V/I source )
- 4- Digital ( Gates, Flip Flops)

Note: You can find ground in, Place -> ground or press “G”. Never forget to add ground to your circuit.

- To edit the properties of the components, select the component and Right click-> Edit properties. Change the required value in the “value “, save and close it.

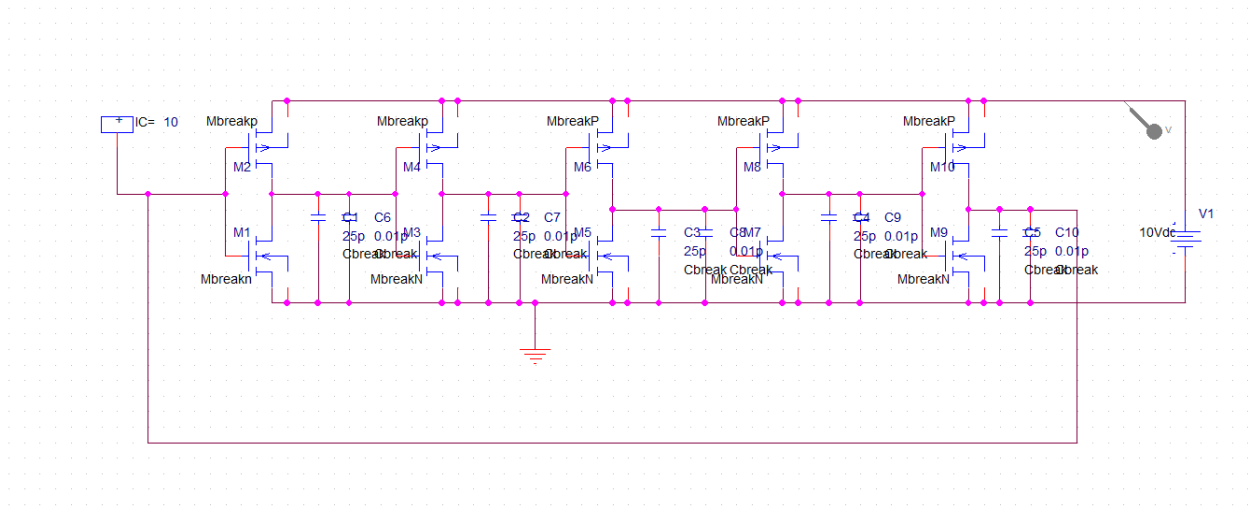
New Property...
Apply
Display...
Delete Property
Pivot
Filter by: < Current properties >

	<b>A</b>
	<b>+ SCHEMATIC1 : PAGE1</b>
Color	Default
Designator	
DIST	FLAT
Graphic	R.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	<none>
Location X-Coordinate	410
Location Y-Coordinate	210
MAX_TEMP	RTMAX
Name	INS61
Part Reference	R1
PCB Footprint	AX/RC05
POWER	RMAX
Power Pins Visible	<input type="checkbox"/>
Primitive	DEFAULT
PSpiceTemplate	R^@REFDES %1 %2 ?TOL
Reference	R1
SLOPE	RSMAX
Source Library	C:\ICADENCE\SPB_16. ....
Source Package	R
Source Part	R.Normal
TC1	0
TC2	0
TOLERANCE	
Value	10k
VOLTAGE	RVMAX

## Simple Circuit and Simulation:

### Schematic:

This simulation is only for testing purpose. So, let's an oscillator where we have odd number of inverters to get the frequency oscillating. The example is done using 5 but you can choose your own number of inverters as long it is odd number.



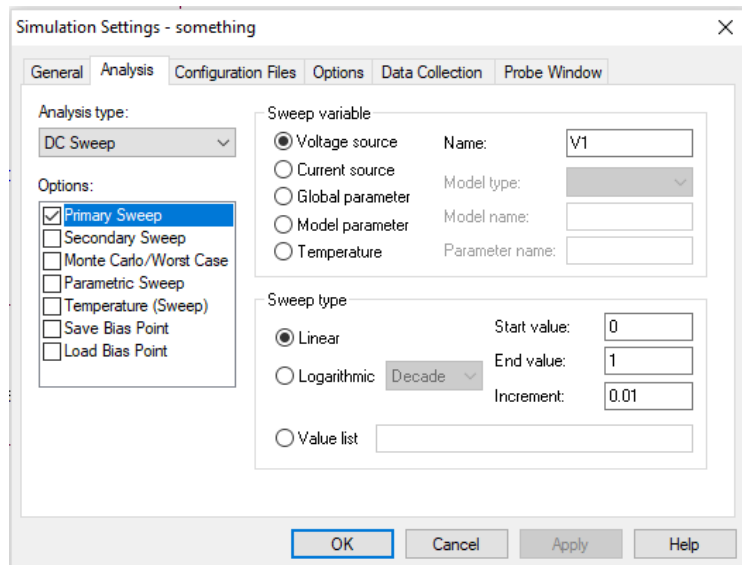
The load between two inverter is couple of capacitor, the operating voltage is 10V DC. Please don't forget to use ground.

### Simulation:

To simulate the circuit, select Pspice-> Edit Simulation Profile/New Simulation Profile.

This tool can perform few simulation,

- 1- Time Domain
- 2- DC analysis
- 3- AC analysis
- 4- Bias( Passing DC to control the circuit )



Select DC sweep for DC analysis, set the value for V and hit ok. To run the circuit, press F11 or Pspice->run or Click Run button in Toolbar.



After you run the simulation, you can probe the voltage and study the characteristics.