Rochester Institute of Technology

EE620 — Project1 Assignment Design of Digital systems

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INTRODUCTION:

This project is all about CMOS design for various combinations of basic gates. Design of inverter, NAND, NOR, XOR, 2input OAI (OR-AND-INVERTER) and Transmission 2:1 multiplexer is designed in this project. This is done using a 45nm CMOS technology in the cadence virtuoso. The software provides an excellent base to test the design in user defined way considering the rules that has to be followed for ideal design. The ultimate aim of the project is to provide knowledge regarding the issues faced in designing a CMOS circuit with respect to various factors from start of design until the desired output is reached. The technology used is 45nm which provides the limitation to size of transistors that apparently leads to scaling them down. Once the layout is designed, the variation in rise/fall time can be computed which

directly shows how fast the design was made. It also gives a chance to compare the switching time for different combination of circuits.

Discussions:

The specified base reference size for NMOS is 12λ/2λ which sets the size as 270nm/45nm and for PMOS is x2 size of NMOS which ends in 540nm/45nm.The technology used is 45nm, fingers are used to break down the size and construct multiple transistors to have an equivalent specification. In order to maintain the equivalent resistance across the PMOS and NMOS the width is adjusted respectively. The mobility in PMOS/NMOS is constant but the resistance in PMOS is twice that of NMOS, in order to maintain equal charging and discharging the resistance has to be maintained at "R", for which the width of the transistor are adjusted accordingly. Generally, wider transistors have more resistance. This gives a chance to view the behavior of transistor when we change the width. When the width is increased the current and gate capacitance increases respectively.

The design of CMOS for various combination of basic gate using a 45nm technology is little bit challenging. As a matter of fact, design is always made with an idea to have least possible size after considering all the restrictions that serves for basic rule check to avoid shorting of contacts between the different layers of CMOS. The quality of design can be recognized when it comes to rise/fall time, which is computed for every single combination in this project.

Rise time here is considered as the time for the waveform to rise from 20% to 80% of the steady state value. Fall time is considered as the time for the waveform to fall from 80% to 20% of the value. Depending on how much the transistor takes to switch between ON/OFF is directly computed in the waveform. The average delay can be computed from rise and fall time.

Propagation delay is the maximum taken for the waveform to reach from the previous input to 50% of the next output which is VDD/2. The average propagation delay is calculated by taking the average of worst case Tpdf and Tpdr

Tpdf= propagation delay falling, Tpdr= propagation delay rising

Average propagation delay Tpd= Tpdf+Tpdr/2

CMOS INVERTERX2:

Equation: Y=A`

The design of inverter is done with the size of NMOS as 540nm/45nm and to PMOS is 1080nm/45nm. The technology has a restriction to size which leads to usage of fingers with multiple transistors in parallel. Since, the resistance of PMOS is twice that of NMOS the width is adjusted respectively to maintain the charge and discharge. The design is made to utilize minimum size as possible. The propagation delay for falling and rising is also calculated Tpdr is 310.8ns and Tpdf is 354ns. This is computed on the layout considering all the parasitic values which has impact on the output values.

Rise time with parasitic is 310.8ps

Fall time with parasitic is 354.6ps

Average propagation delay = 332.4ps

CMOS NAND:

Equation: Y= ~(A+B)

The design of NAND using CMOS is done with size of NMOS as 540nm/45nm and of PMOS as 540nm/45nm. The resistance is added in series NMOS, in order to reduce the added resistance the width is doubled. Width is inversely proportional to the resistance. The design is simple and not much complication is found. Considering the propagation delay, it is calculated for single input keeping other input constant to observe the variation of output and vice versa.

Rise time with parasitic: 562.2ps

Fall time with parasitic: 709.3ps

Average propagation delay: 491.7ps

CMOS NOR:

Equation: Y= ~(A.B)

The design of NOR is done with the size of NMOS as 270nm/45nm and PMOS as 1080nm/45nm. The PMOS is in series where the resistance is added, to reduce the added resistance the width of the

transistor is doubled to 1080nm/45nm. This design can be done in 3 fingers of 360nm/45nm each for PMOS. Yet, the design seems to be pretty simple and does not get complicated. The rise time is 624.1ns and fall time is 373.3ns. The propagation delay is calculated for single input and compared.

Rise time with parasitic: 624.1ps

Fall time with parasitic: 373.3ps

Average propagation delay: 523.4ps

CMOS OAI:

Equation: Y= ~((A0+B0).(A1+B1))

The design of OR-AND-INVERTER with 2 inputs seems to have added series resistance in PMOS and NMOS. To maintain the equivalent resistance across PMOS and NMOS the width is doubled for both of them. PMOS of 1080nm/45nm and NMOS of 540nm/45nm is the size. The design gets little bit complicated here yet, gives the knowledge of designing 2 input combinations using CMOS. The rise time considering parasitic is 563.6ns and fall time is 406.1ns. The propagation delay is computed for every single input keeping others constant to figure the variation of output.

Rise time with parasitic: 563.6ps

Fall time with parasitic: 406.1ps

Average propagation delay: 547.6ps

CMOS XOR:

Equation: Y= (AB`+A`B)

The design of XOR shows up with 2 inputs which require inverted function of each other. The size of the PMOS and NMOS is doubled to maintain the equivalent resistance across them. PMOS of 1080nm/45nm and NMOS of 540nm/45nm is the size of this design. The design gets little complicated, when it comes to design of 2 base inverter with the design of XOR in single cell. The connection between different layers plays a hard role which also gives the knowledge of designing complicated circuit. The difficulty faced in this design was shorting the PMOS and NMOS with metal layer. Since metal layer needs 6λ width and 6λ spacing between them, there was not much spacing in the vertical area. Placing the Metal

on top of PMOS showed up some spacing. The rise time with parasitic is 619ns and fall time is 666.7ns. The propagation delay is calculated for every single input to find the behavior of output respectively.

Rise time with parasitic: 619ps

Fall time with parasitic: 666.7ps

Average propagation delay: 542.35ps

TMUX:

Equation: Y=(AS`+BS)

Transmission multiplexer is generally a switch that has control on the output. 2:1 MUX is deigned here, where the PMOS is of size 540nm and NMOS is of size 270nm. Since the switch "S" needs an inverted function, an inverter is required. The design seems to be pretty simple and not many complications were found. The rise time with parasitic seems to be 555.9ns and fall time seems to be 734.1ns.

Rise time with parasitic: 555.9ps

Fall time with parasitic: 734.1ps

Average propagation delay: 409ps

Conclusion:

Considering the design of all the combinations, the major issue was with design of metal layer, routing of the I/O ports. The design gets little complicated when the routing has to be in 8 λ, 8 λ spacing, which is done to eliminate the violation error by router. Considering, the aspect of reducing size and the routing that take 8 λ and 8 λ area is little complicated with respect to actual design. As discusses earlier, the metal spacing issue in XOR was eliminated by routing the metal on top of PMOS. Overall, the project was very helpful in understanding the design of various CMOS logic circuits and the issues that came across gave a good experience in designing. Considering the quality, the rise time/ fall time and propagation delay gave the relationship how the output behaves with respect to input and the parasitic values. Comparing the rise time / fall time values for pre layout and post layout, there seems to be 5-10% difference due to the parasitic effects from the design on layout.

APPENDIX:

DATASHEET OF INVERTER:

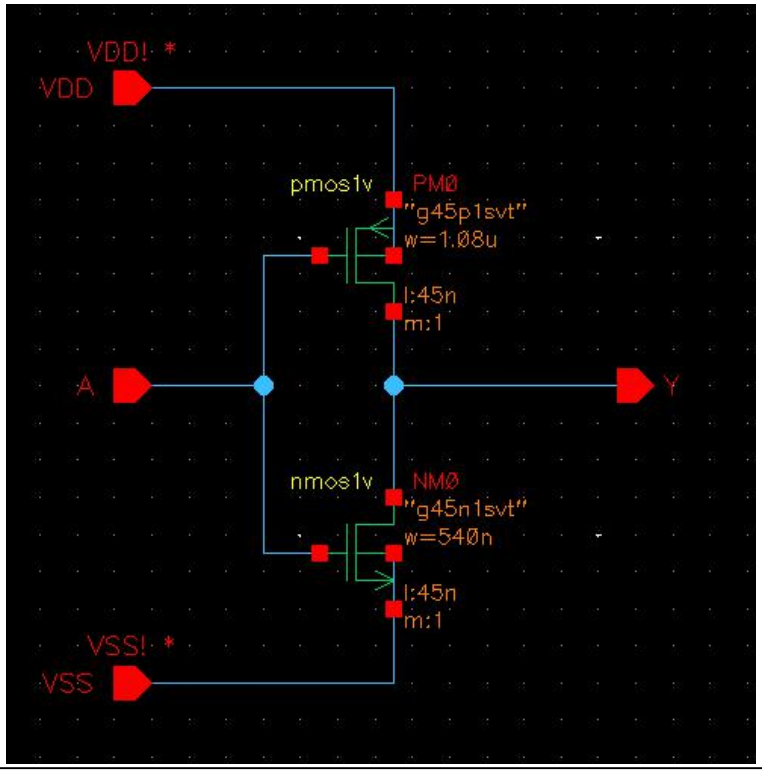
Library Name:	**dab8730_dab_lib**
Cell Name:	**dab_INVX2**
Function/Truth Table:	
A	**Y**
O	**1**
1	**0**
Propagation Delay:	
1. Signal A → Falling edge	**247.9E-12**
Signal Y → Rising edge	
2. Signal A → Rising edge	**279.5E-12**
Signal Y → Falling edge	
Output Rise Time: 310.8E-12	

Output Fall Time: 354.6E-12

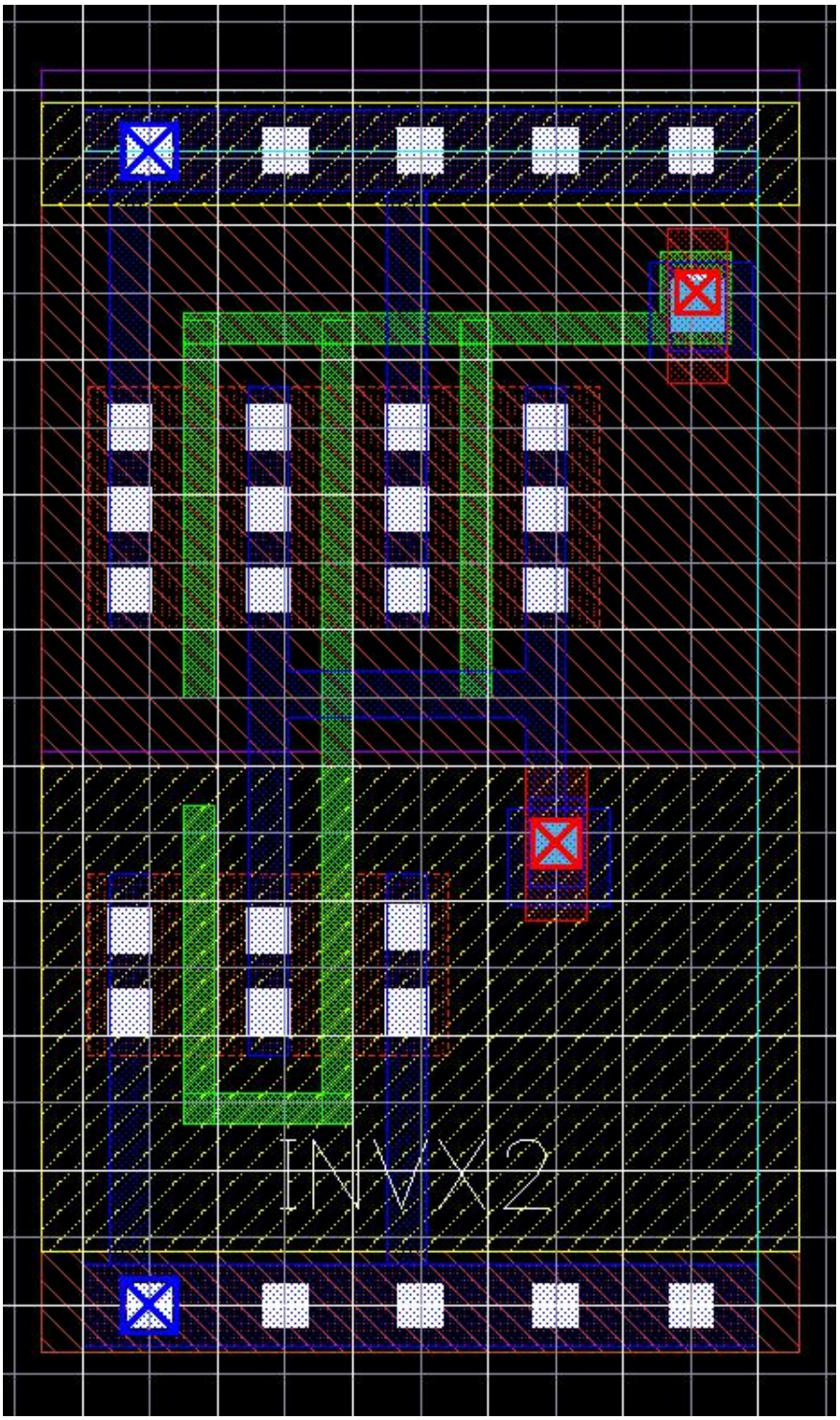
Layout Area: 1.71μm

Symbol with Port Names:

Schematic:



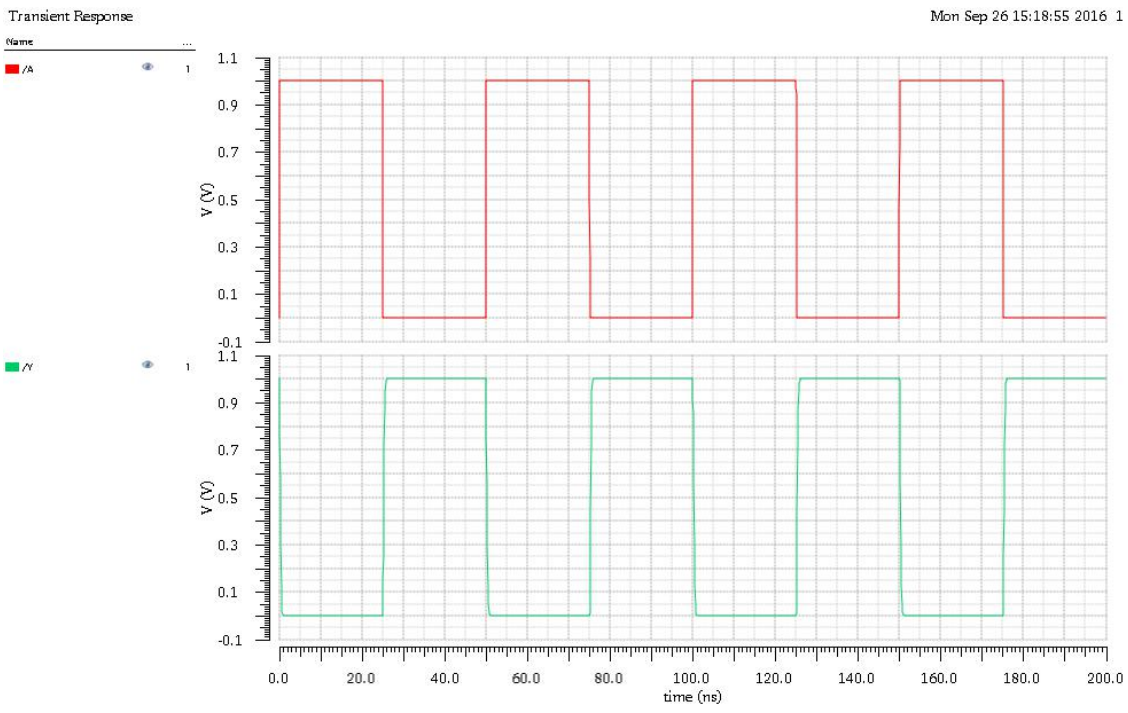
Layout:



Verilog Model:

```
//Verilog HDL for "dab8730_dab_lib", "dab_INVX2" "functional"


module dab_INVX2 ( Y, A, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;

not U1 (Y, A);

endmodule
```

Functional Simulation Waveforms:



Comments/Notes:

Reference inverter : nMOS Wn/L= 270nm/45nm

pMOS wp/l= 540nm/45nm

To maintain the equivalent resistance between pMOS and nMOS, scaling is done

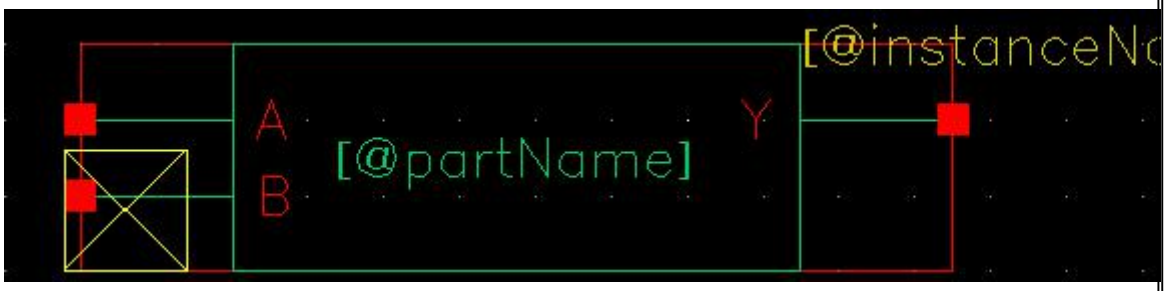
After scaling: nMOS Wn/L= 540nm/45nm

pMOS wp/l= 1080nm/45nm.

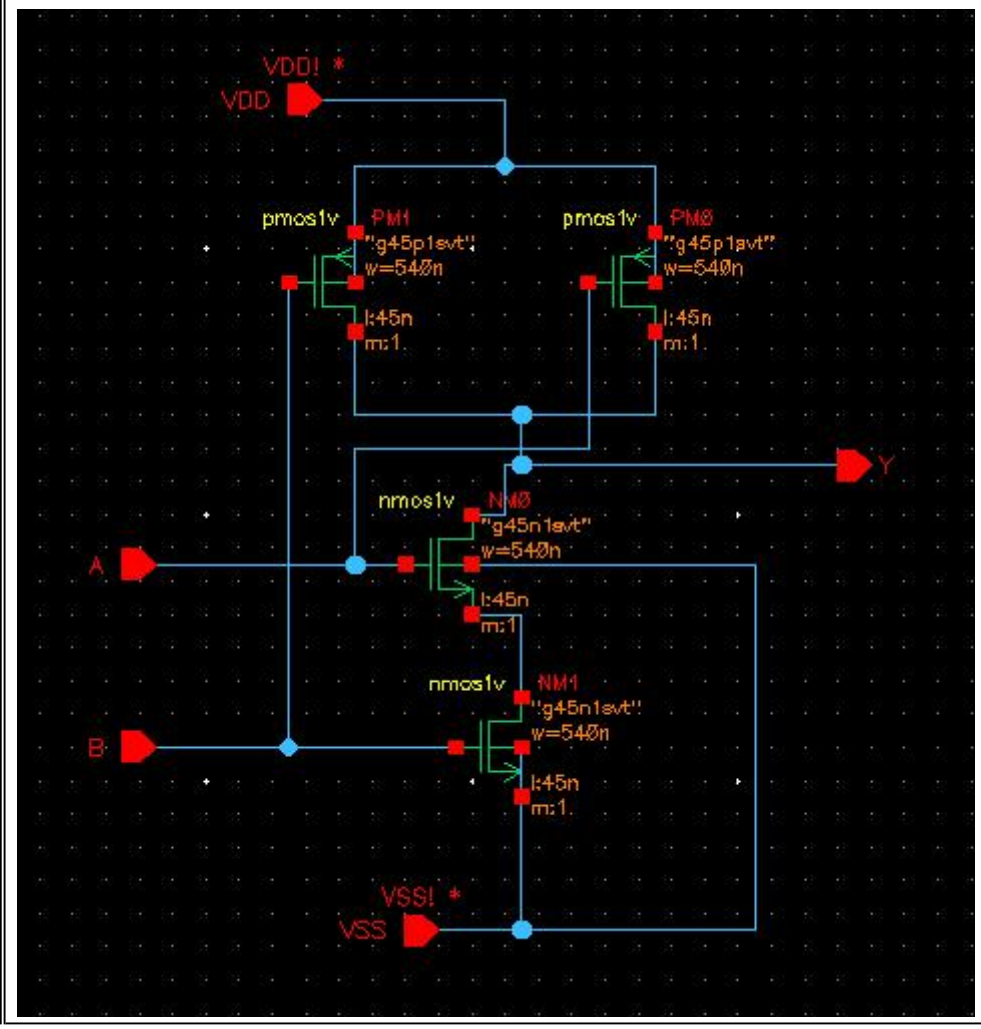
Tpd= 332.4ps

DATA SHEET FOR NAND:

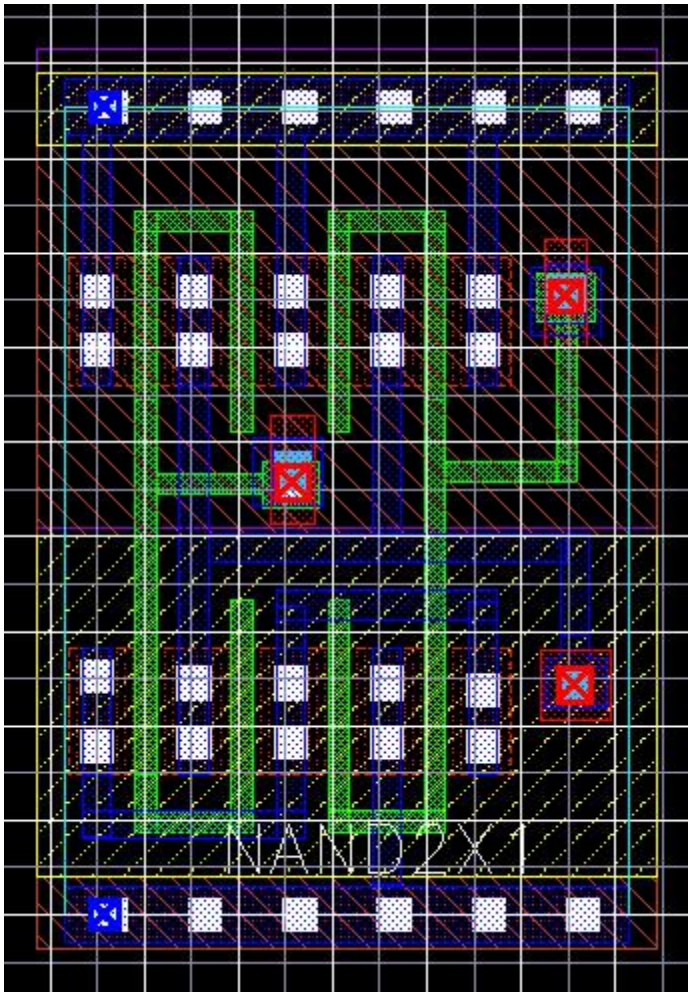
Library Name:	**dab8730_dab_lib**	
Cell Name:	**dab_NAND2X1**	
Function/Truth Table:		
A	**B**	**Y**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Propagation Delay:	
1. Signal A → Falling edge Signal Y → Rising edge	**430.8E-12**
2. Signal A → Rising edge Signal Y → Falling edge	**551.7E-12**
3. Signal B → Falling edge Signal Y → Rising edge	**431.7E-12**
4. Signal B → Rising edge Signal Y → Falling edge	**551.7E-12**
Output Rise Time: 562.2E-12	
Output Fall Time: 709.3E-12	
Layout Area: 2.052 µm	
Symbol with Port Names: 	

Schematic:


VDD! *
VDD
pmos1v
PM1
"g45p1svt"
w=540n
l:45n
m:1
pmos1v
PM0
"g45p1svt"
w=540n
l:45n
m:1
Y
nmos1v
NM0
"g45n1svt"
w=540n
l:45n
m:1
A
nmos1v
NM1
"g45n1svt"
w=540n
l:45n
m:1
B
VSS! *
VSS

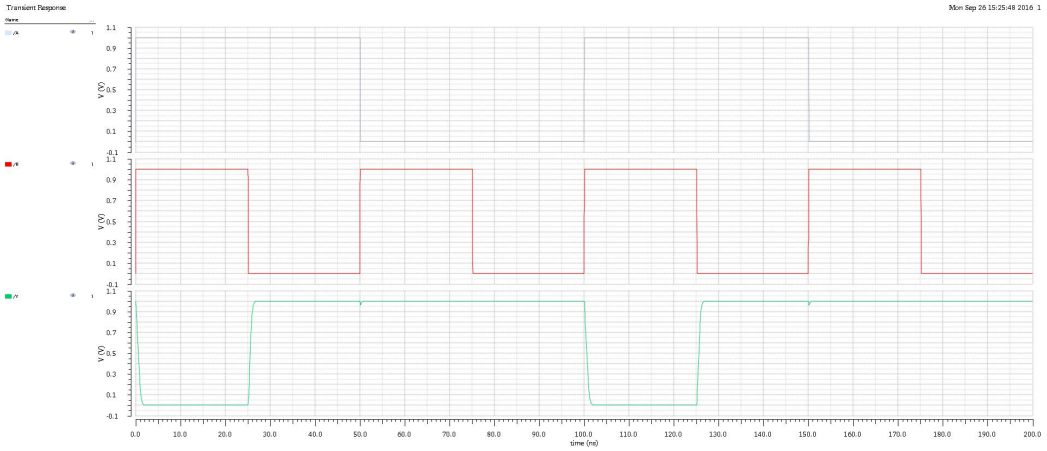
Layout:

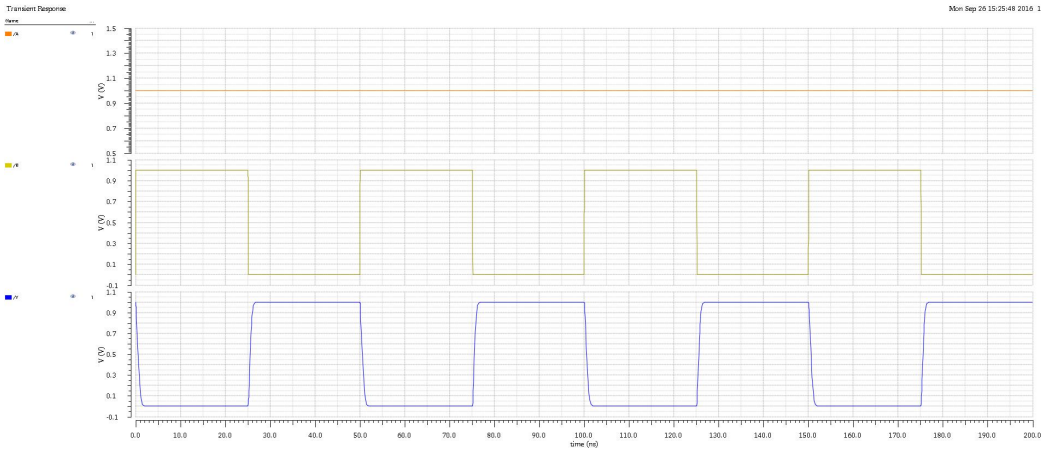


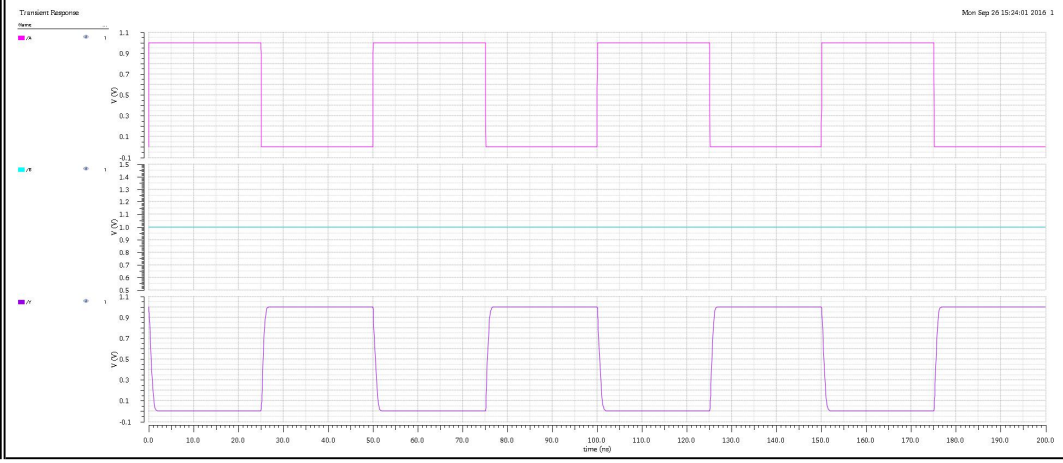
Verilog Model:

```
//Verilog HDL for "dab8730_dab_lib", "dab_NAND2X1" "functional"


module dab_NAND2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;

nand U1 (Y, A, B);

endmodule
```

Functional Simulation Waveforms:







Comments/Notes: **With respect to the reference sizes, the nMOS width is doubled as they are in series with each other to maintain the equivalent resistance R across the layout.** **pMOS Wp/L=540nm/45nm** **nMOS Wn/L= 540nm/45nm** **Tpd= (431.7+551.7)/2= 491.7ps**

DATA SHEET FOR NOR:

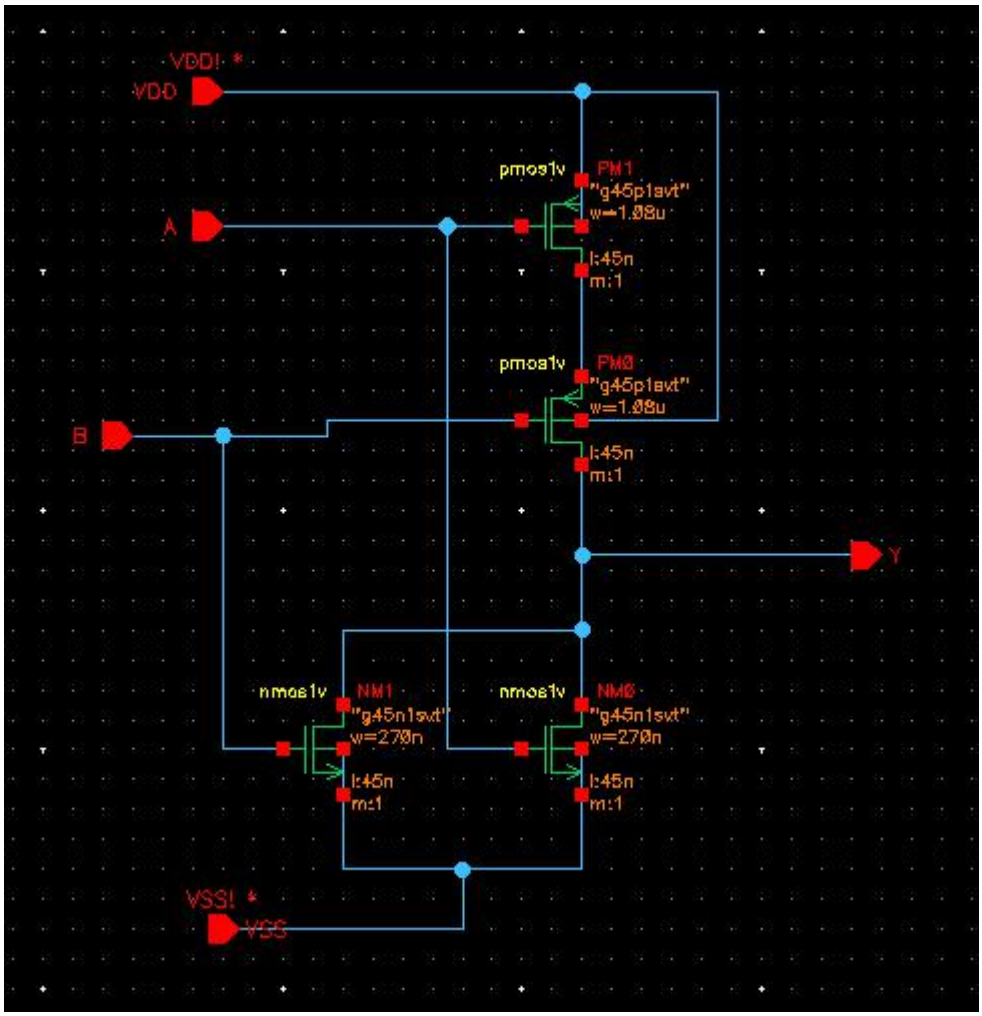
Library Name:	**dab8730_dab_lib**
Cell Name:	**dab_NOR2X1**
Function/Truth Table:	

A	**B**	**Y**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**

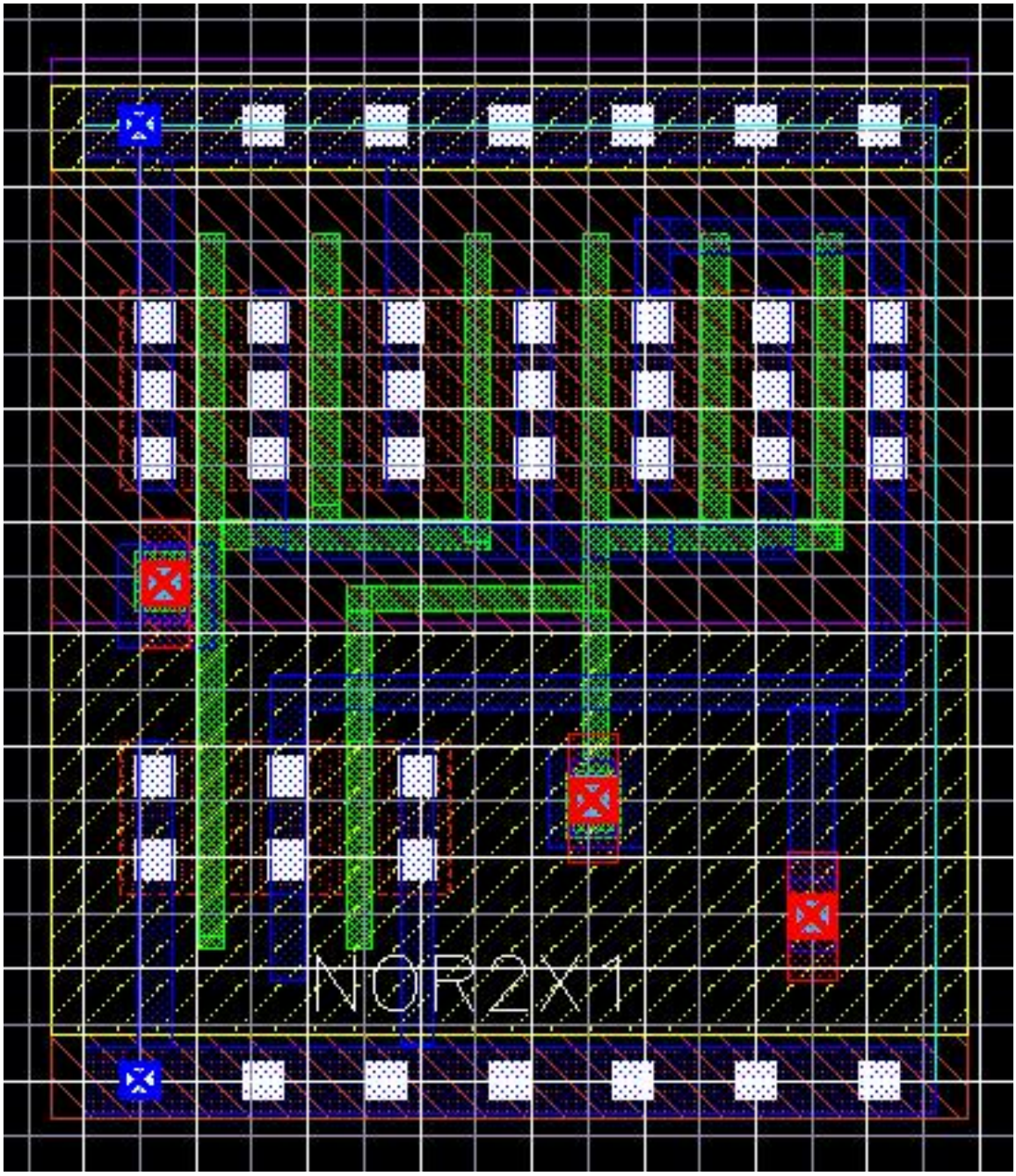
Propagation Delay:

1. Signal A → Falling edge **Signal Y → Rising edge**	**484.6E-12**
2. Signal A → Rising edge **Signal Y → Falling edge**	**548.2E-12**
3. Signal B → Falling edge **Signal Y → Rising edge**	**486.7E-12**
4. Signal B → Rising edge **Signal Y → Falling edge**	**560.1E-12**
Output Rise Time: 624.1E-12	
Output Fall Time: 373.3E-12	
Layout Area: 2.5992 µm	
Symbol with Port Names: 	

Schematic:


VDD! *
VDD
pmos1v
PM1
"g45p1svt"
w=1.08u
A
l=45n
m=1
pmos1v
PM0
"g45p1svt"
w=1.08u
B
l=45n
m=1
Y
nmos1v
NM1
"g45n1svt"
w=270n
l=45n
m=1
nmos1v
NM0
"g45n1svt"
w=270n
l=45n
m=1
VSS! *
VSS

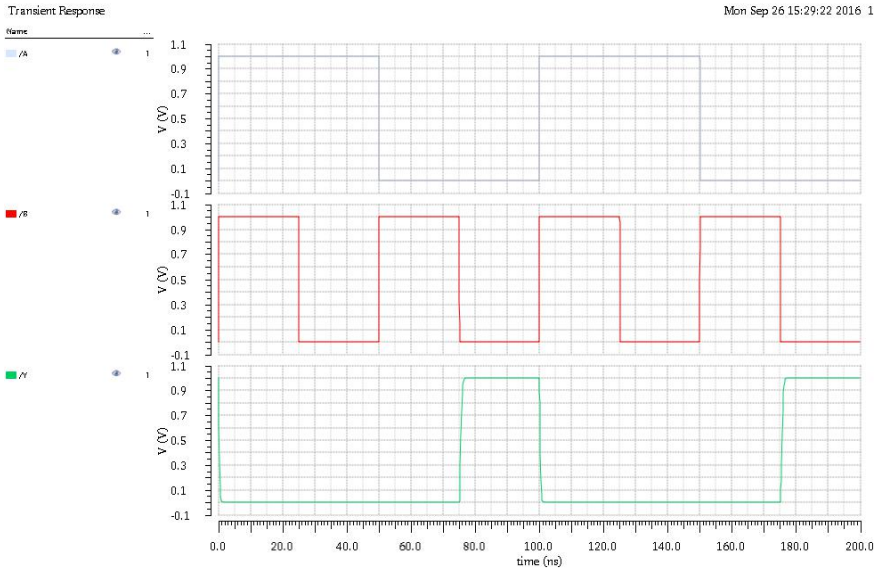
Layout:

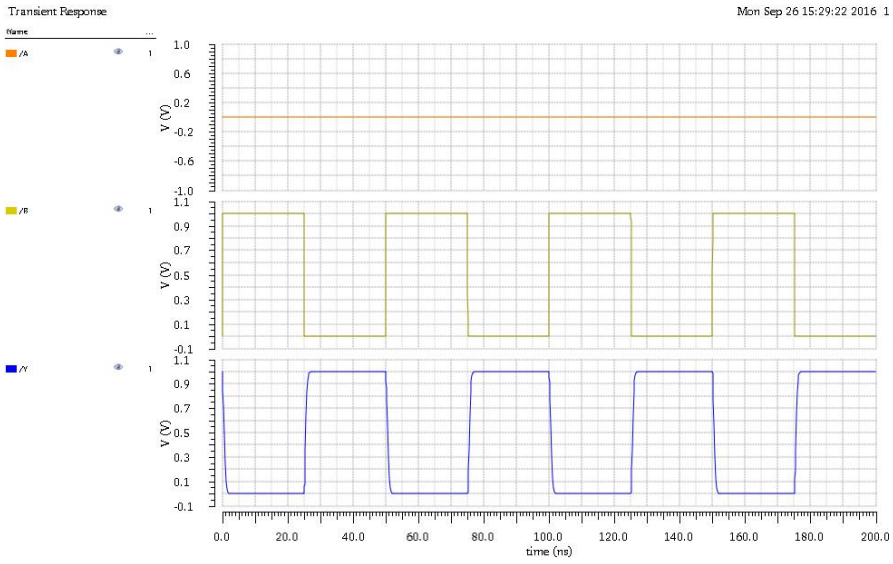


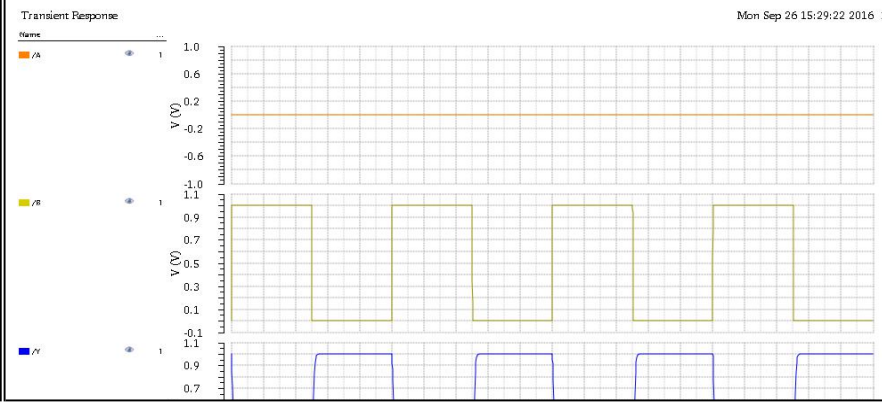
Verilog Model:

```
//Verilog HDL for "dab8730_dab_lib", "dab_NOR2X1" "functional"


module dab_NOR2X1 ( .VSS(\VSS! ), Y, A, B, .VDD(\VDD! ) );

  input A;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  output
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;

nor U1 (Y, A, B);

endmodule
```

Functional Simulation Waveforms:







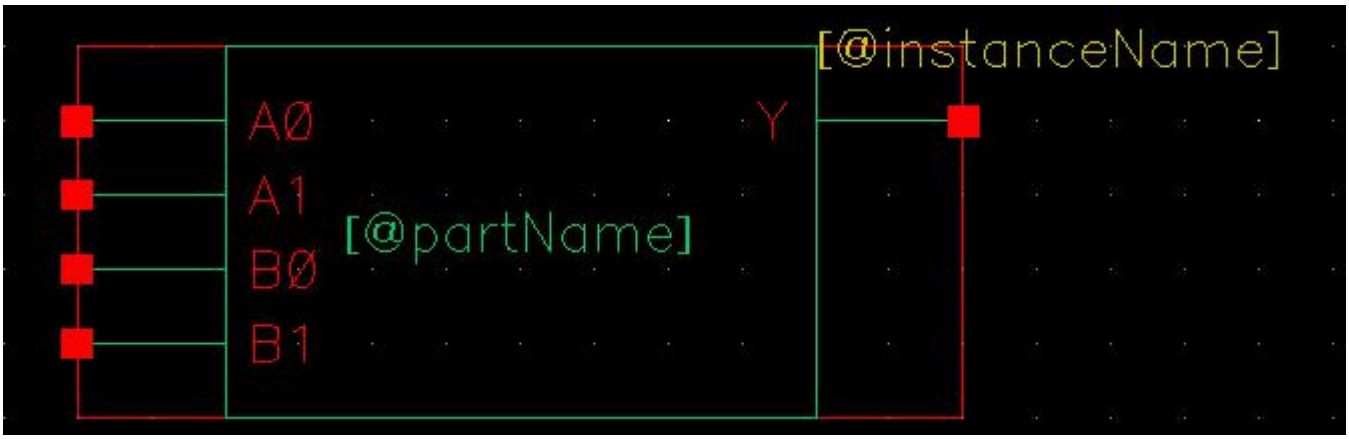
Comments/Notes:
With respect to the reference sizes, pMOS size is doubled to 1080nm/45nm to keep the equivalent R across the nMOS and pMOS. pMOS Wp/l= 1080nm/45nm nMOS Wn/l= 270nm/45nm Tpd = (486.7ps+560.1ps)/2 = 523.4ps

DATA SHEET FOR OAI:

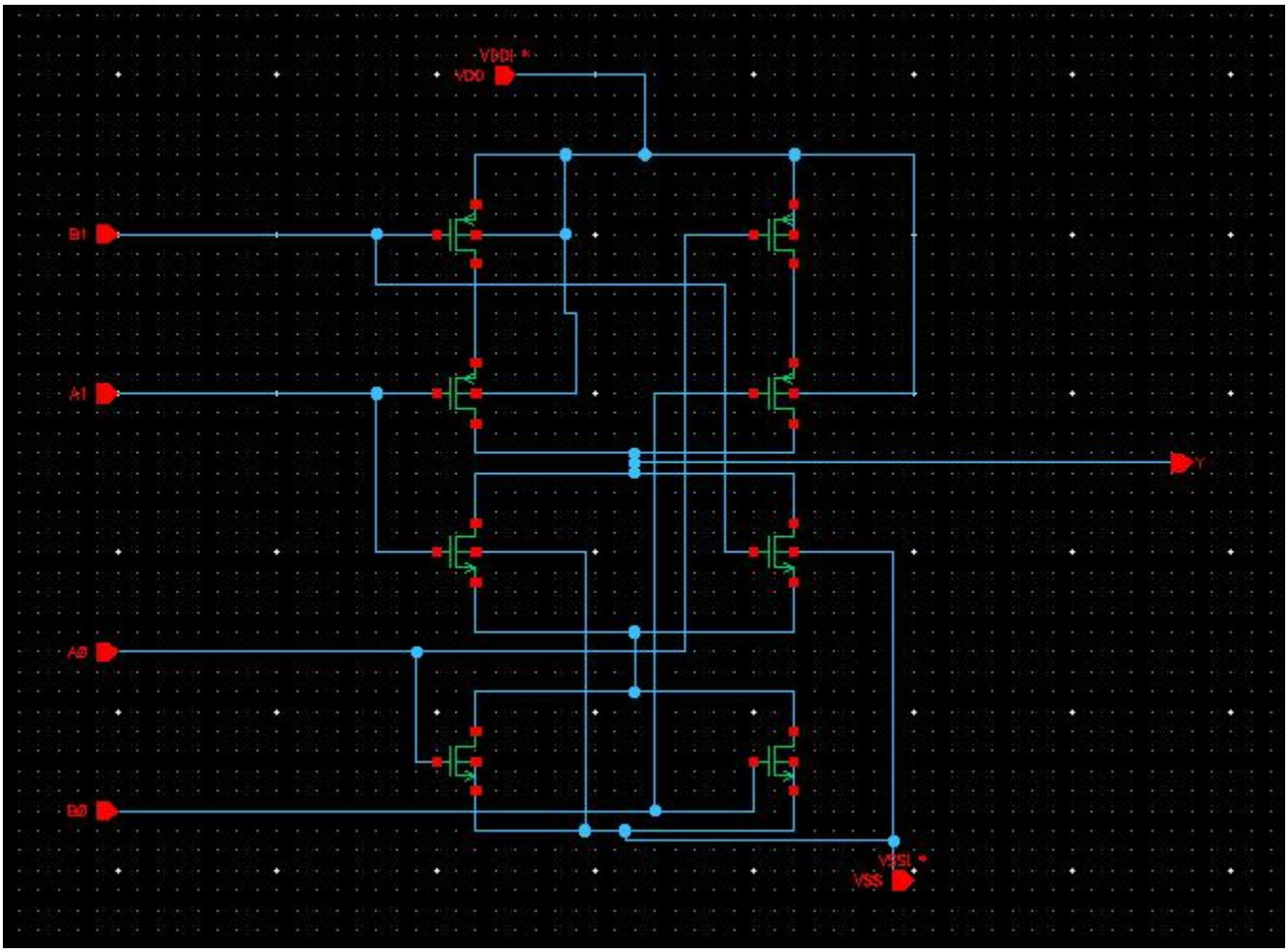
Library Name:	dab8730_dab_lib
Cell Name:	dab_OAI22X1
Function/Truth Table:	

A0	A1	B0	B1	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	0	0	0	1

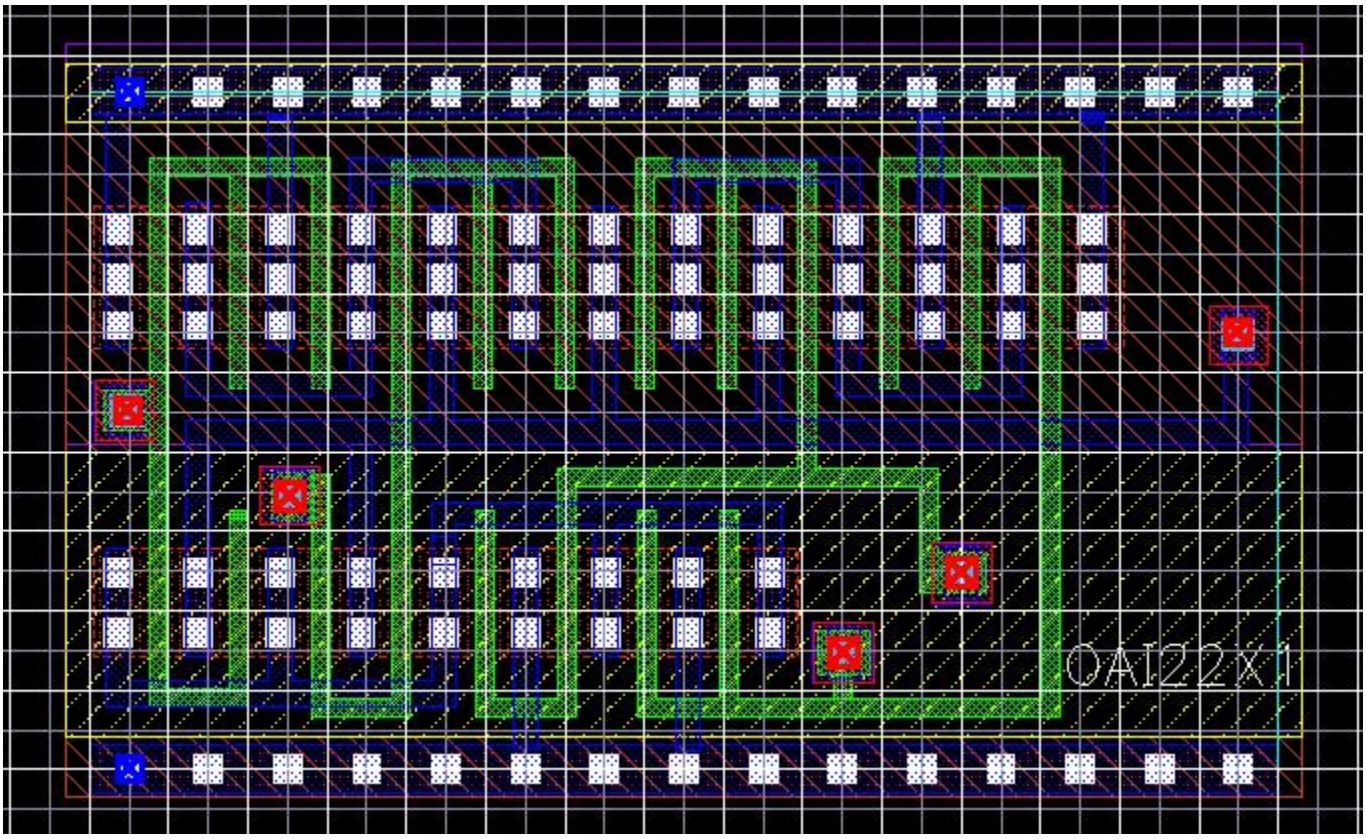
0 1 0 1	0
0 1 1 0	0
0 1 1 1	0
1 1 0 0	1
1 0 0 1	0
1 0 1 0	0
1 0 1 1	0
1 1 0 0	1
1 1 0 1	0
1 1 1 0	0
1 1 1 1	0
Propagation Delay:	
1. Signal A0 -> Falling Signal Y-> Rising	451.9E-12
2. Signal A0 -> Rising Signal Y-> Falling	643.3E-12
3. Signal A1 -> Falling Signal Y-> Rising	449.4E-12
4. Signal A1 -> Rising Signal Y->Falling	462.8E-12

5. Signal B0 -> Falling Signal Y-> Rising	447.9E-12
6. Signal B0 -> Rising Signal Y-> Falling	632.7E-12
7. Signal B1 -> Falling Signal Y-> Rising	450.6E-12
8. Signal B1 -> Rising Signal Y->Falling	627.1E-12
Output Rise Time: 563.6E-12	
Output Fall Time: 406.1E-12	
Layout Area: Cell Width*Cell Height = 3.1µm*1.71 µm = 5.13µm	
Symbol with Port Names: 	

Schematic:



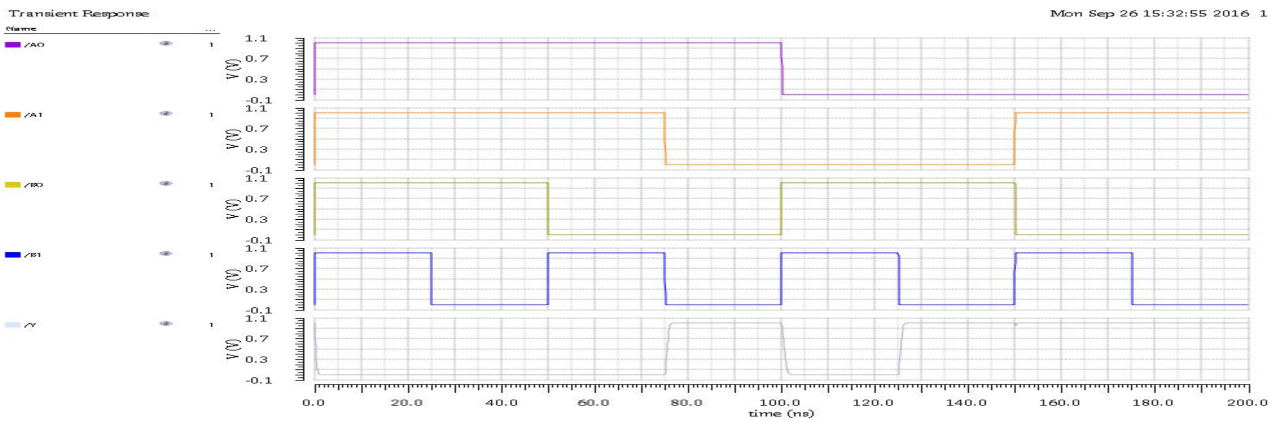
Layout:

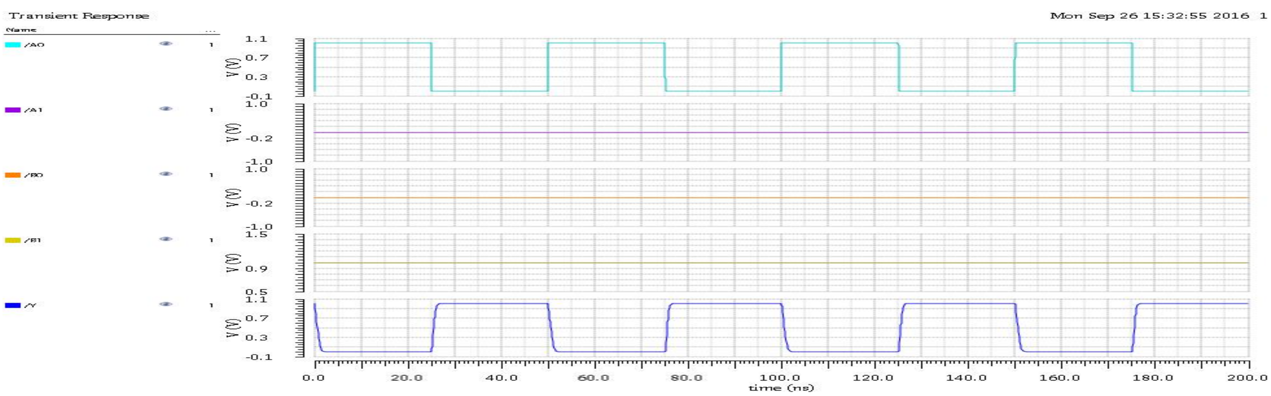


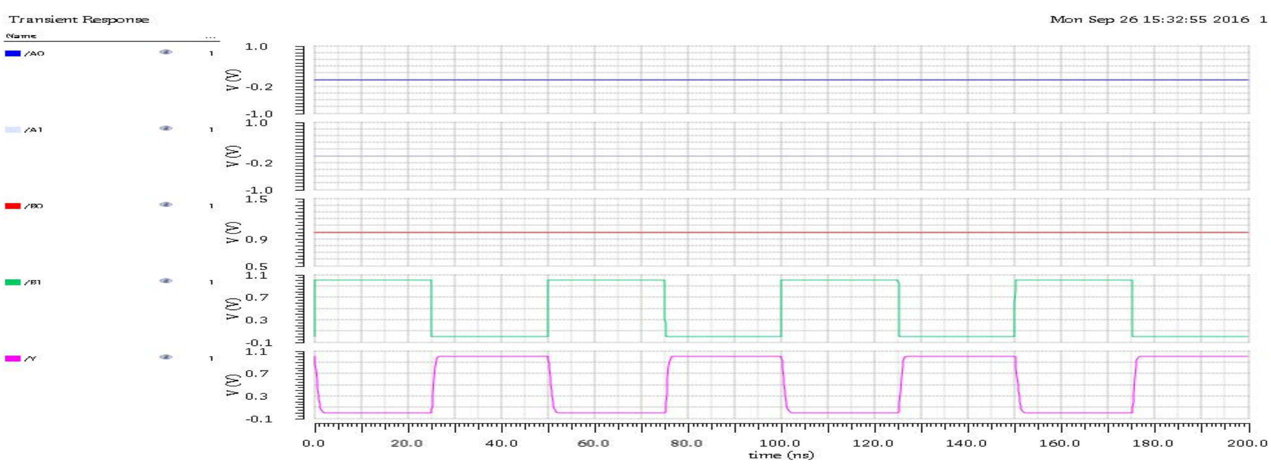
Verilog Model:

```
//Verilog HDL for "dab8730_dab_lib", "dab_OAI22X1" "functional"


module dab_OAI22X1 ( Y, A0, A1, B0, B1, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A0;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input B0;
  input B1;
  input A1;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
assign Y= ~ ((A1|B1)&(A0|B0));
endmodule
```

Functional Simulation Waveforms:







Comments/Notes:

The width of nMOS and pMOS are doubled with respect to the reference size as, they are in series combination the equivalent resistance across them has to be same.

pMOS Wp/L= 540nm/45nm

nMOS Wn/L=1080nm/45nm

Tpd= (451.9ps+643.3ns)/2= 547.6ns

DATA SHEET FOR XOR:

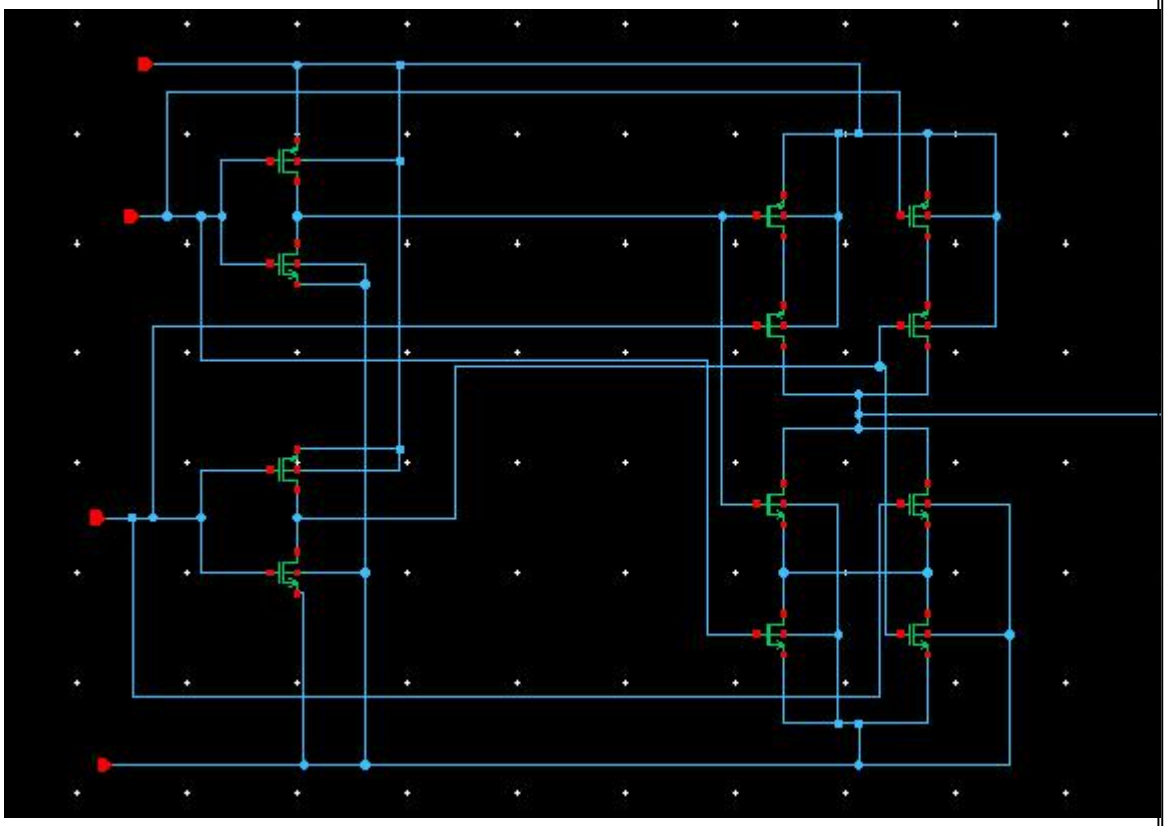
Library Name:	**dab8730_dab_lib**
Cell Name:	**dab_NOR2X1**

Function/Truth Table:

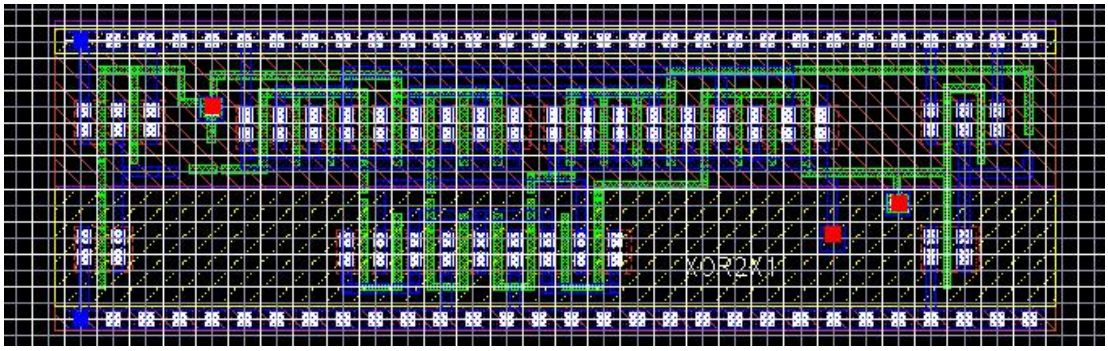
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Propagation Delay:	
1. Signal A → Falling edge **Signal Y → Rising edge**	**517E-12**
2. Signal A → Rising edge **Signal Y → Falling edge**	**547.7E-12**
3. Signal B → Falling edge **Signal Y → Rising edge**	**537.7E-12**
4. Signal B → Rising edge **Signal Y → Falling edge**	**513.4E-12**
Output Rise Time: 621.5E-12	
Output Fall Time: 664.6E-12	
Layout Area: 10.26 µm	
Symbol with Port Names: 	

Schematic:



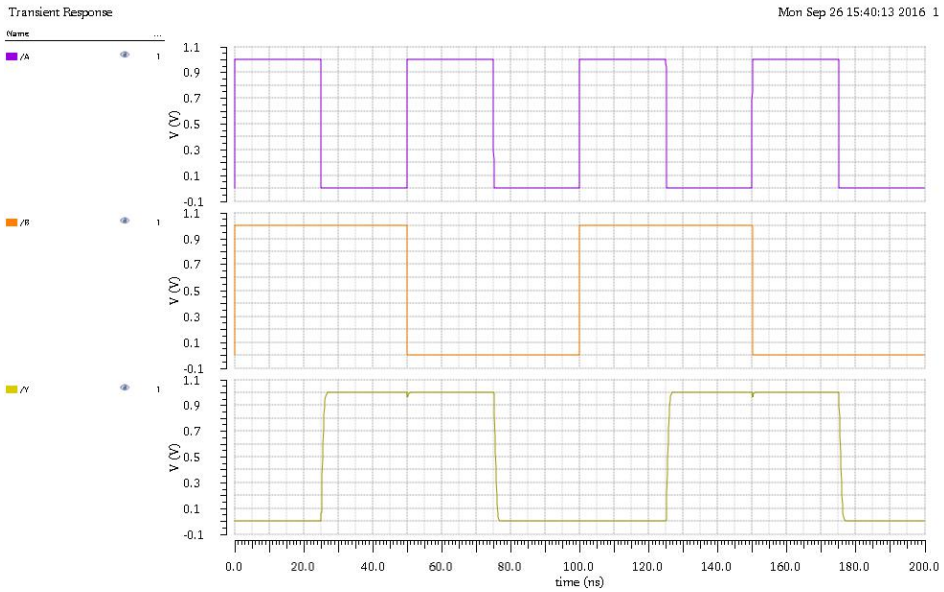
Layout:

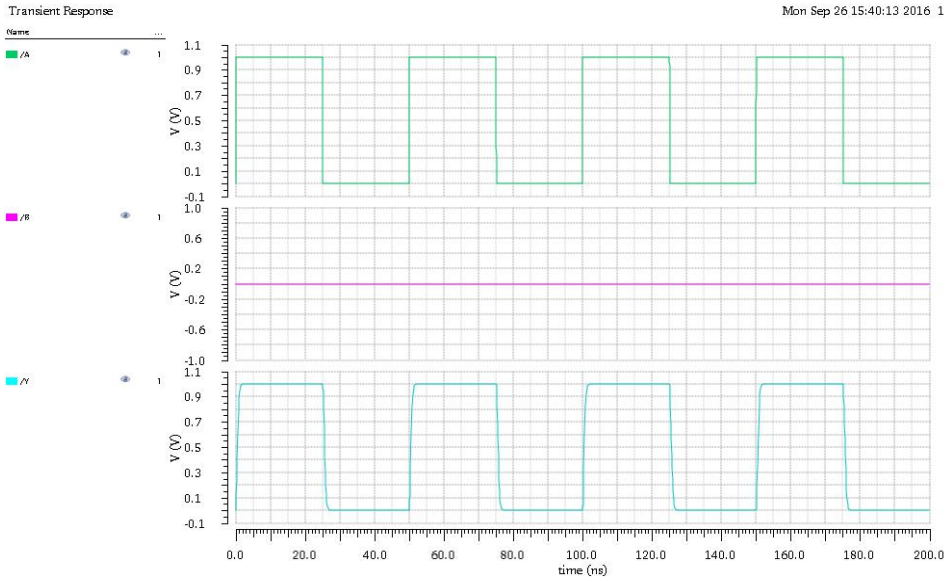


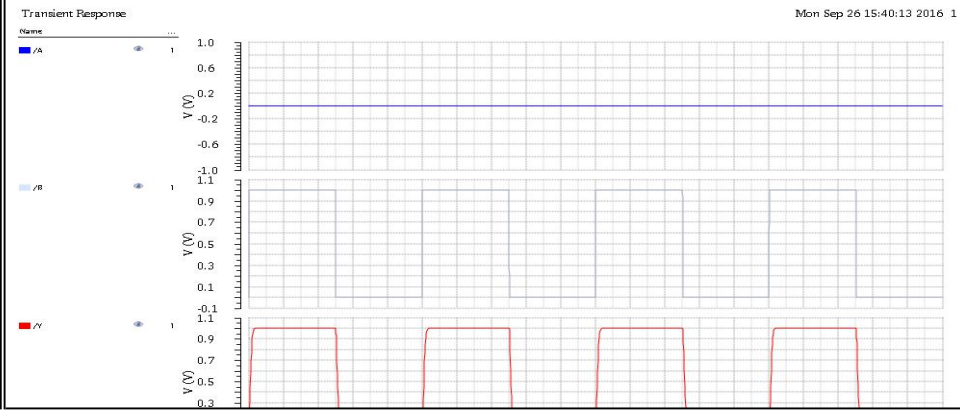
Verilog Model:

```
//Verilog HDL for "dab8730_dab_lib", "dab_XOR2X1" "functional"


module dab_XOR2X1 ( Y, A, B, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;
xor U1 (Y, A, B);
endmodule
```

Functional Simulation Waveforms:







Comments/Notes:

With respect to the reference size, the pMOS and nMOS are doubled to maintain the equivalent R across them. Since they are in series the resistance is r/2 which increases the width over x2.

nMOS Wn/L= 540nm/45nm

pMOS Wl/L = 1080nm/45nm

Tpd= (537.7ps+547.7ps)= 542.35ps

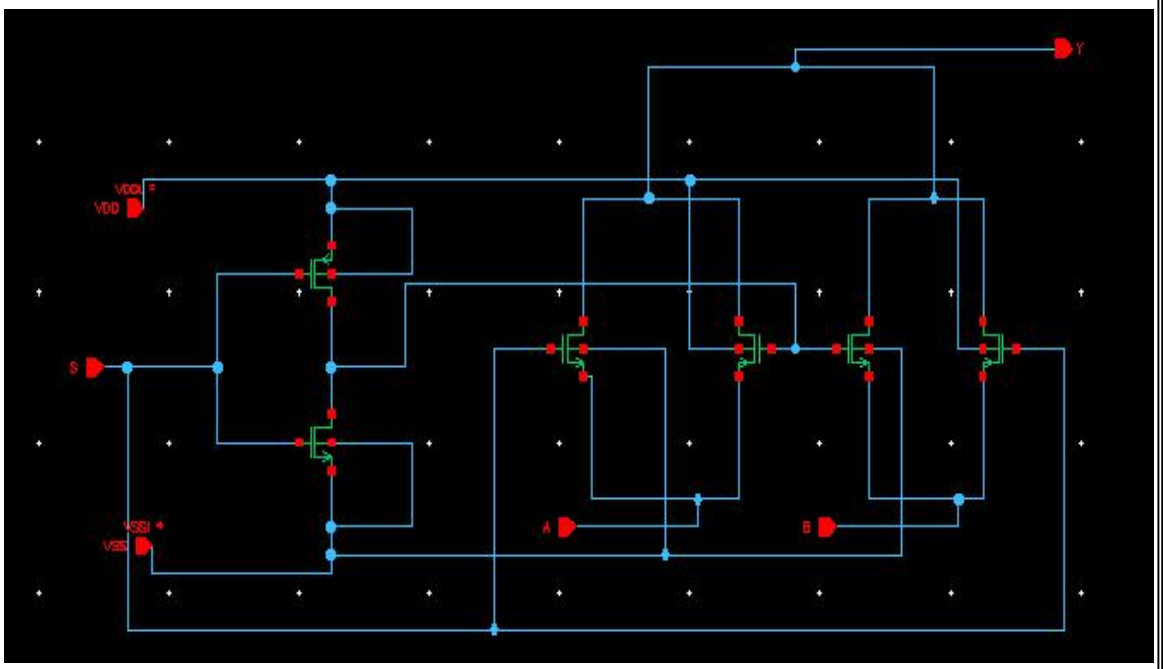
DATA SHEET FOR TMUX:

Library Name:	**dab8730_dab_lib**
Cell Name:	**dab_TMUX2X1**
Function/Truth Table:	
S A B	**Y**
0 0 X	**0**
0 1 X	**1**
1 X 0	**0**
1 X 1	**1**

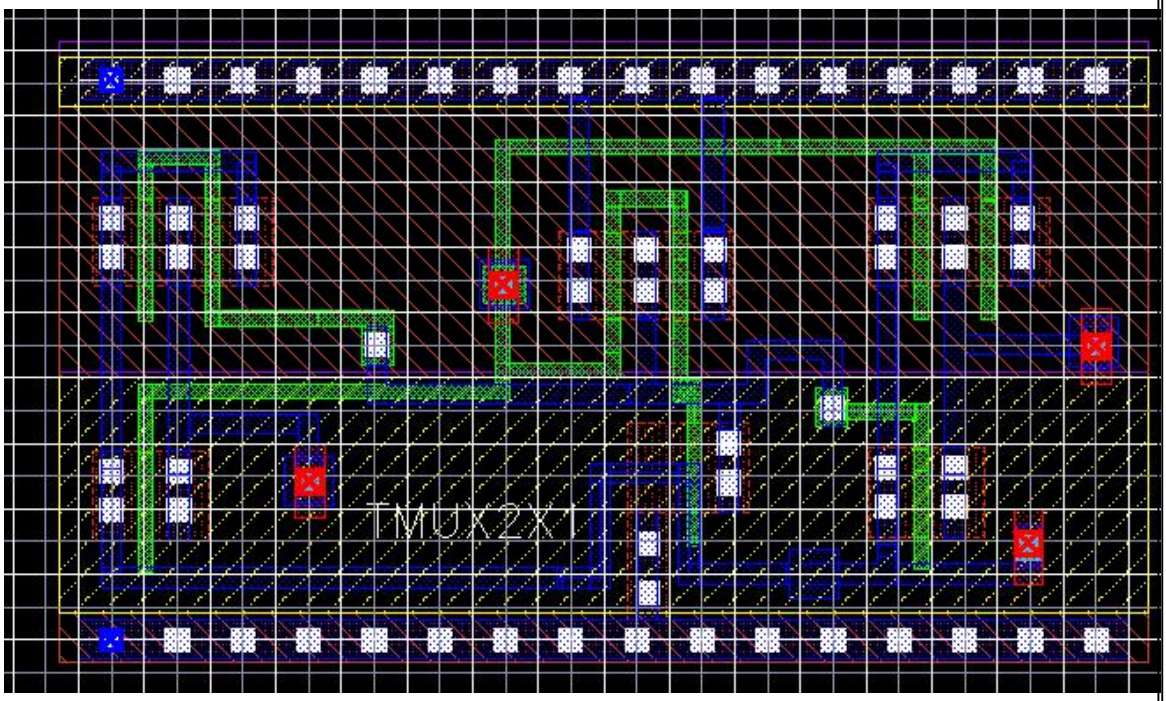
Propagation Delay:	
1. Signal S → Falling edge Signal Y → Rising edge	372.5E-12
2. Signal S → Rising edge Signal Y → Falling edge	445.5E-12
3. Signal A → Falling edge Signal Y → Rising edge	349.09E-12
4. Signal A → Rising edge Signal Y → Falling edge	408.9E-12
5. Signal B → Falling edge Signal Y → Rising edge	347.7E-12
6. Signal B → Rising edge Signal Y → Falling edge	410.2E-12
Output Rise Time: 555.9E-12	
Output Fall Time: 734.1E-9	
Layout Area: 5.472 µm	

Symbol with Port Names:

Schematic:



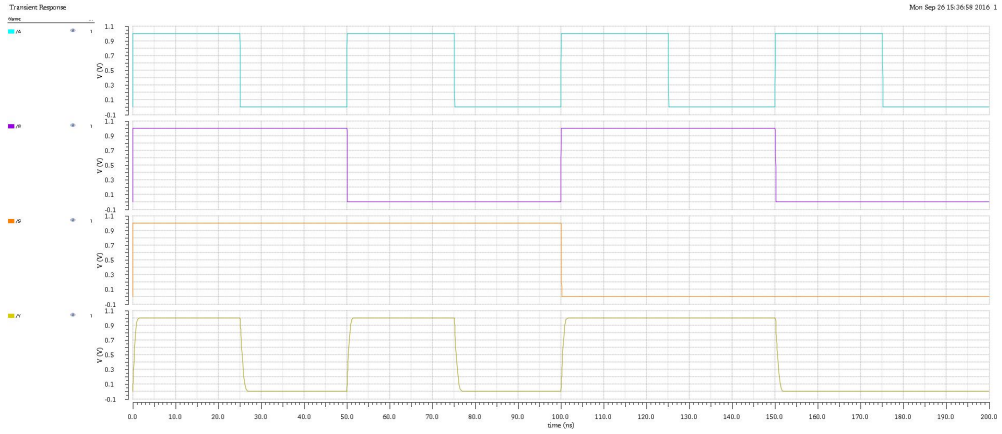
Layout:

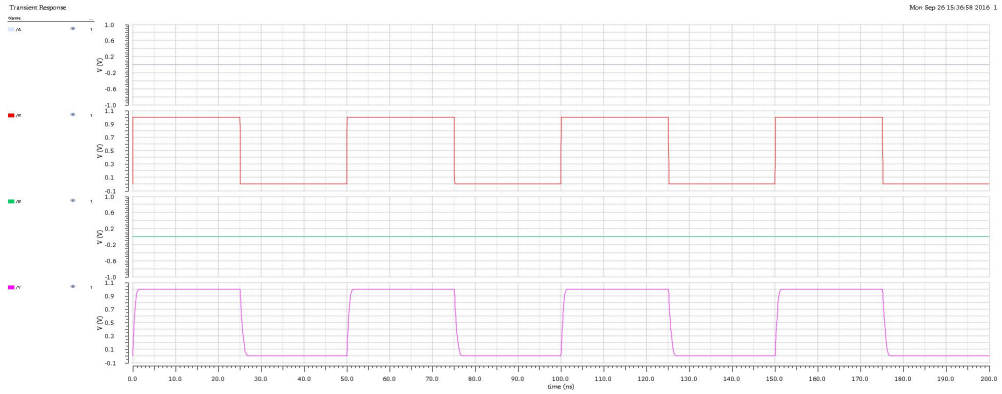


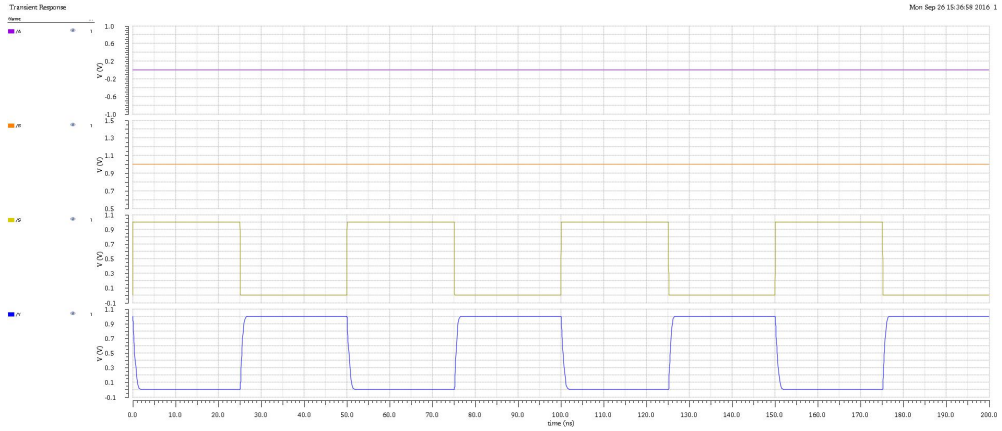
Verilog Model:

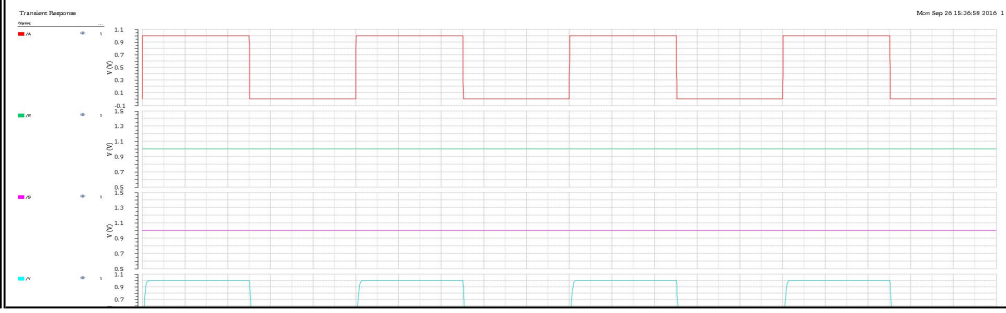
```
//Verilog HDL for "dab8730_dab_lib", "dab_TMUX2X1" "functional"


module dab_TMUX2X1 ( Y, A, B, S, .VDD(\VDD! ), .VSS(\VSS! ) );

  input A;
  input S;
  output Y;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VDD";
       integer inh_conn_def_value = "cds_globals.\\VDD! "; *)
`endif
  \VDD! ;
  input
`ifdef INCA
    (* integer inh_conn_prop_name = "VSS";
       integer inh_conn_def_value = "cds_globals.\\VSS! "; *)
`endif
  \VSS! ;
  input B;
assign Y = (((~S) & A)|(S & B));
endmodule
```

Functional Simulation Waveforms:









Comments/Notes:

Multiplexer acts as a unit where the output is totally controlled with respect to the signals which is fed into the switch. Multiplexer are cheap ,reduces complexity , reduces the usage of wires and also various implementation can be done.

pMOS Wp/L= 540nm/45nm

nMOS Wn/L=270nm/45nm

Tpd= (372.5ps+445.5ps)/2 = 409ps