

Analysis of factors affecting the performance of FinFET

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Abstract—Moore's law defines number of transistor over a square area in integrated circuits will double every year. On contradiction to the statement made by Gordon Moore in 1965, semi conductor industry already started facing saturation level. MOSFET has been a excellent candidate of transistor started to face several issue as the size started to shrink. When MOSFET gets scaled below 32nm the gate control over the channel fails and device fails to hold the promise of desired function. FinFET a new technology of small size transistors showed up by giving a new birth to Moore's law and showed a big gloom in semi conductor industry. FinFET seems to be promising candidate for scaling down the transistor below 32nm and still going on up to 7nm currently. FinFET provides the assurance of scalability, excellent gate control of channel, works on low power, improved performance. Having said this, the FinFET also comes with a pack of constrains that has to be addressed before the benefits of the FinFET is fully acquired. This paper brings the advantages of FinFET over MOSFET and provides a detailed analysis on the factors that affect the performance of the FinFET devices.

I. INTRODUCTION:

As the size of the transistors tends to go beyond a certain regime of 32nm , the MOSFET device fails to hold the gate control over the channel which ends up in leakage current, Drain induced barrier lowering (DIBL), Short channel effect(SCE). All these considerations comes into picture which reduces the reliability and reduces the performance of the MOSFET device. All of these holds the MOSFET from being scaled down further down the track. FinFET seems to be a promising candidate which works fine by having a excellent control over the channel due to the new geometry features and also increases the reliability along with the performance of the device. Every big player in the semi conductor industry shift from MOSFET to FinFET by knowing this. A 14nm/16nm FinFET process can offer 40%-50% in performance than a 28nm MOSFET process. FinFET is basically fabricated in two types as shown in the Fig.1 and Fig. 2 (1) dual gate FinFET where the the channel is made of ultra thin layer of silicon and is placed on the insulator. The electric field from the gate to fin is reduced in this structure. (2) Tri-Gate FinFET, in which the Fin gate is wrapped on three sides of the channel by proving a excellent control on the channel and since the fins are made vertical high packing density can be achieved. This improves the performance when large number of transistors can be placed in same place. Since the FinFET are smaller in size, the power consumption of the device is drastically reduced, the performance of the device can be increased by integrating more FinFET's in the same there same area, devices respond faster with less delay, reduced leakage

current from gate to channel, excellent control of channel by the gate can be obtained in tri-gate FinFET structure. When FinFET is operated in low voltage 1v It gets 18% faster than normal planar device and at 0.7V it gets 37% faster, this shows how fast a device can work when it is combined with FinFET for a low power circuits. This enables a big difference between the gate voltage and the threshold voltage which makes the performance better in the low power circuit. It comes with a pack of consuming low power and giving a fast switching activity. Another interesting fact about the FinFET with respect to design is, since the channel is well controlled by gate already the gate does not need any heavy doping which makes the fabrication convenient. This bring a major glow in the semi-conductor industry. Having said all of these, FinFETS have its own constrains that has to be addressed with proper consideration

Fig. 1. Dual gate FinFET

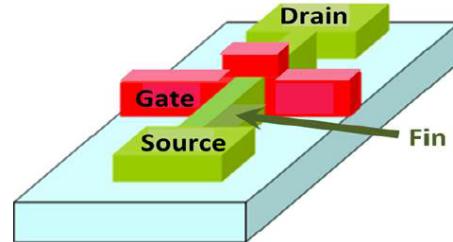
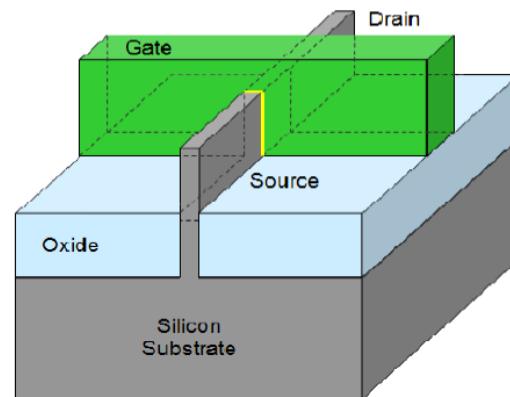


Fig. 2. Tri-gate FinFET structure



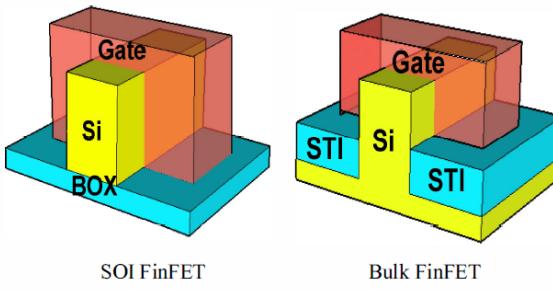
Major issues in FinFET such as self-heating, Fringing capacitance effect, Design constrain are addressed in this paper and a approach to overcome the issue is suggested. . In most of the cases suggestion are like a trade off with another

parameter. Yet, new approach for major issue has to be taken into consideration. This paper also shows the advantage of FinFET over MOSFET as an overview.

II. SELF-HEATING AND RELIABILITY ISSUES:

Self heating and reliability issues have become a major concern as the size of transistors scale down. Especially when it comes to FinFET the standing new approach for MOSFET, the heating issues becomes very serious due to complex structure where there is less possibility to eliminate heat. Self heating issues leads to electro-migration effect and reduces the reliability of the device. Electro-migration, is serious issue where the migration of metal atoms takes place due to strong electric field that attracts the atoms of metal layers in the direction of the drift field. The density of metal tends to hold the atoms until the force is strong enough to cause a shift in atoms. This reduces the life of the device and leads to performance issues or logic failure.

Fig. 3. Geometry of SOI Finfet and Bulk FinFET



Scaling has already reached upto 7nm. Decreasing the dimension will lead to hot spot in the drain region which increases the drain series resistance. FinFET of two geometry SIO FinFET and Bulk FinFET is show in the Fig. 3. Having said that FinFET devices are good enough to substitute MOSFET on the scaling track, the heating issues are serious in because of the less conductivity of interlayer dielectric material(ILD) and buried oxide(BOX). Adding on top of this, the thermal conductivity of the oxide used in SOI FinFET is very poor which can be seen from the table 1. So SOI FinFET seems to dissipate more heat when compared to Bulk FinFET due to the presence of oxide insulator which has less conductivity. From Fig. 4 we can interpret the heating issue with respect to the scaling factor. We can clearly see the scaling of transistors makes it possible to integrate large number of transistors in a small area but this increases more heat dissipation. Due to which heating effect takes place which has to be treated properly to get rid of reliability issues and maintain the life of the device.

As we say, self heating is a serious issue and steps have to be taken to get rid of it, looking closely we can figure that major part of the power dissipation occurs in the drain region because of the presence of strong electric field . Interesting fact, is that self-heating is dependent only on the number of fins used but not the number of gates. We can see, the gates don't not

Fig. 4. Power dissipation with respect to scaling

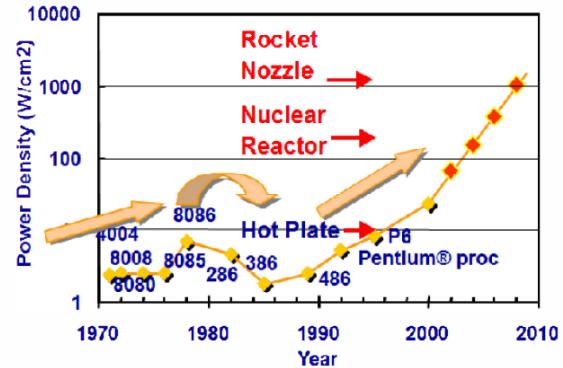
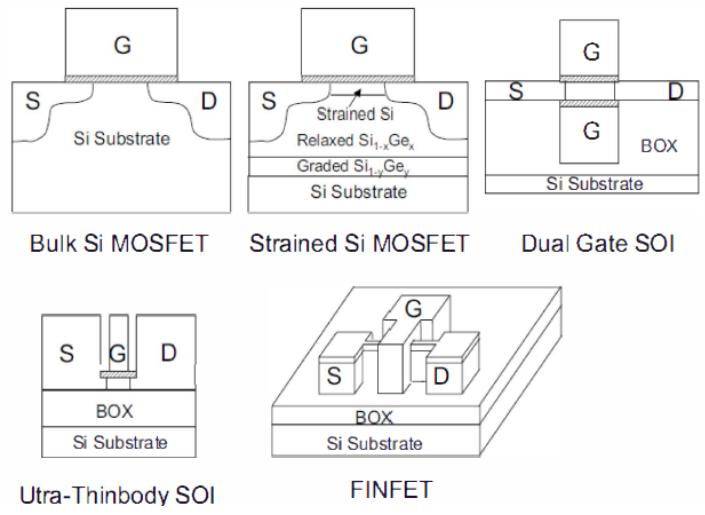


TABLE I
THERMAL CONDUCTIVITY OF MATERIAL

Material	Thermal Conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)
Si (bulk)	148
Ge (bulk)	60
Silicides	40
Si (10nm)	13
$\text{Si}_{0.7}\text{Ge}_{0.3}$	8
SiO_2	1.4

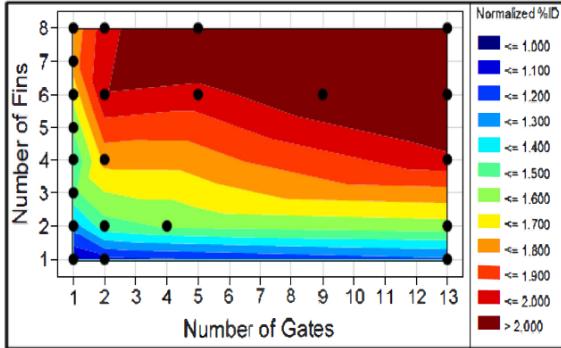
contribute to self heating issue but the fin material does. Fig. 5. shows the evolution of FinFET from bulk MOSFET. As the scaling continued the heating effect played a major role. Fig. 6 shows the impact of fins on the heating issue.

Fig. 5. Evolution of FinFET from Bulk MOSFET



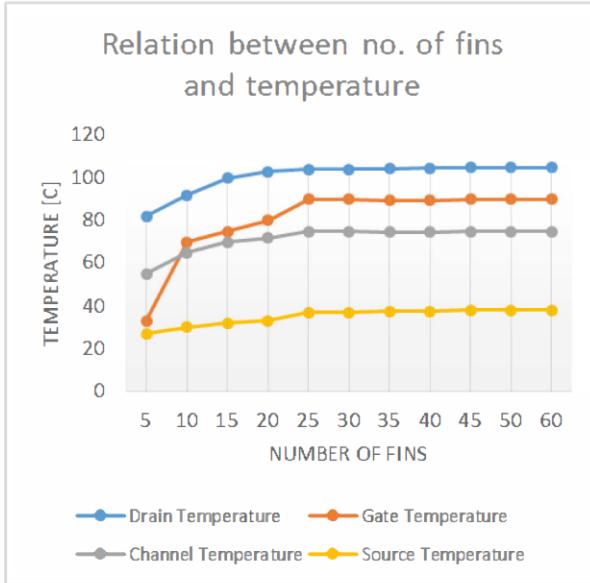
Having said SOI finFET face serious heating issues than Bulk FinFET, both of them are worse when compared to planar device by considering the heat dissipation through the channel. The substrate is hardly 10nm oxide layer in case of SOI FinFET, we cannot expect this 10nm oxide to make any

Fig. 6. self heating issues with respect to number of fins and gates



contribution to heat dissipation. Considering the structure of FinFET most of the heat dissipates through the gate that wraps around the channel and the source and drain which is then dissipates the heat to the substrate through the contacts. These heat generating structures are bigger than the 10nm substrate which apparently is not sufficient to get rid of heating issues.

Fig. 7. Graphical comparison between the number of Fins and temperature

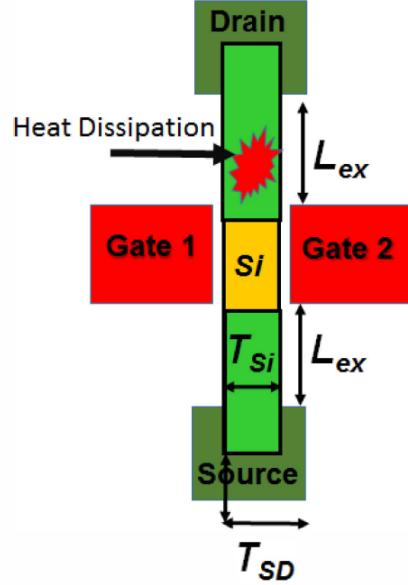


A. New approach to reduce the Heating effect transfer through the substrate:

[1]By reducing the extension length L_{ex} and increasing the height of the source/drain will increase the thermal conductivity and also reduces the thermal resistance. Reducing the extension length L_{ex} will make it easier for the heat to dissipate by moving the heat dissipation region far into source/drain near the contacts where the heat get dissipated very easily. But however there is one interesting thing we have to note that is by reducing the extension length L_{ex} and increasing the height of the source/drain the fringing capacitance of the

gate is increased. So this method approached here acts like a trade off for reduction in heating issues with increase in fringing capacitance. If this is implemented in real time, the fin width, fin pitch, gate dielectric width have to be maintained accordingly to have less fringing capacitance. However heating issue seems to be severe issue as it comes to scaling down the transistor beyond 22nm. So we can probably implement this method in read time by giving priority heating issue and find ways to reduce fringing effect which is discussed following the content.

Fig. 8. New Design approach to reduce the self heating issue in the FinFET



III. FRINGING EFFECTS:

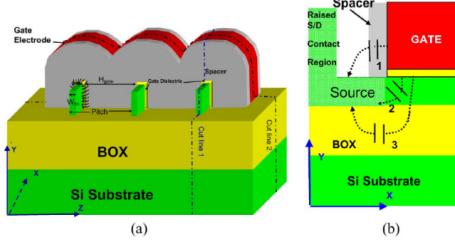
[4]The fringing field that forms between the gate to source account to parasitic value and bring a major difference in the performance of the FinFET device. The Fringing field is affected due to few factors such as gate-dielectric thickness, the spacer width, fin width and pitch, gate height etc. The geometry of the FinFET is very small where the scattering of carriers occurs due to thin and narrow source/drain regions, this increases the parasitic resistance along with increase in capacitance due to fringing fields in small 3-D geometry. The Fundamental design of FinFET should be designed appropriately by considering these factor which pulls down the performance of the device.

Since, the device has to scaled down to extreme limit, parasitic capacitance have become a significant issue. To exactly find the impact of fringing effect, the 3-Dimensional stimulation have to be considered. Especially, considering a Tri-Gate FinFET which has two vertical gates and one horizontal gates surrounded by fin as show in Fig. 9

A. EFFECT OF FRINGING FIELD THROUGH THE SPACER:

The three major components of gate-to-source capacitance is shown in the Fig. 9, are as follows:

Fig. 9. (a) Three-dimensional schematic of a multiple-fin FinFET device showing the electric-field lines from the gate to the source on the first fin. The raised S/D region is not shown as it will block the view of fins. (b) The cross section of half of the FinFET device along the cut line 1 in (a). The three major components of gate-to-source capacitance C_{GS} are shown.



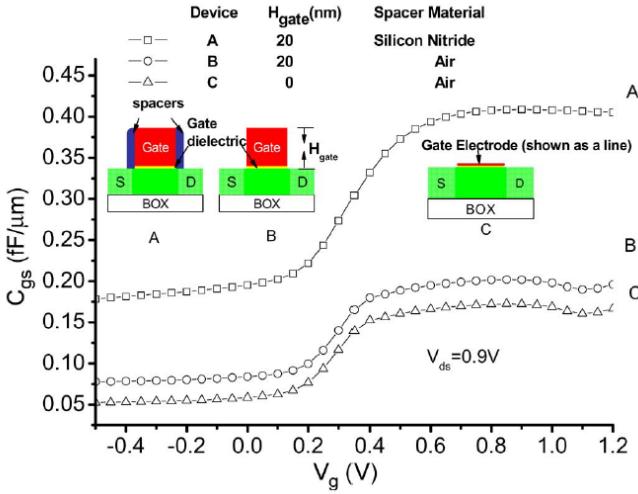
1) Sidewall fringing capacitance which flows from the sides of the gate to the source;

2) The fringing capacitance which flows to the source from the bottom of the gate through the Si body;

3) The fringing capacitance that flows to the source from the gate through the BOX layer.

Considering the device is designed using underlapped gate, the overlap capacitance is negligible here. To find the effect of fringing field due to the spacer, three structures are considered namely A, B and C which are identical except for the gate and/or the spacer. The schematic of the structure is shown in the Fig. 10

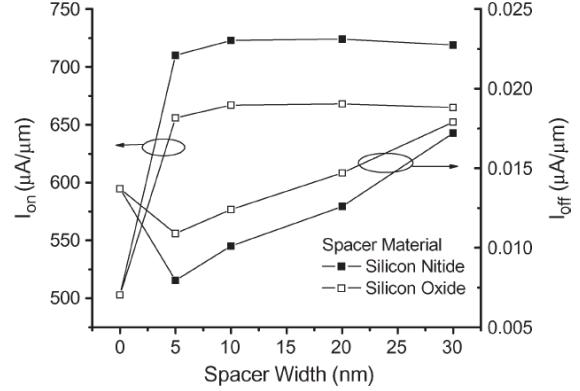
Fig. 10. Gate to source capacitance of three identical devices with different gate and spacer geometries. Device space A - with volume gate electrode and nitride spacer. Device space B - with volume gate electrode and no spacer. Device space C - with surface gate electrode and no spacer.



Device A has a gate electrode thickness of 20nm with a nitride spacer of 20nm. Device B has a gate electrode but no spacer. Device C has surface gate electrode and no spacer. The parasitic capacitance of these structures is shown in Fig. 9. C_{GS} , gate to source capacitance of device A is found to be 3 times higher than that of device B and 3.5 times that of device C. The major reason behind this difference is due to capacitive coupling between gate and source. However this is reduced when spacer material has low permittivity. Structure

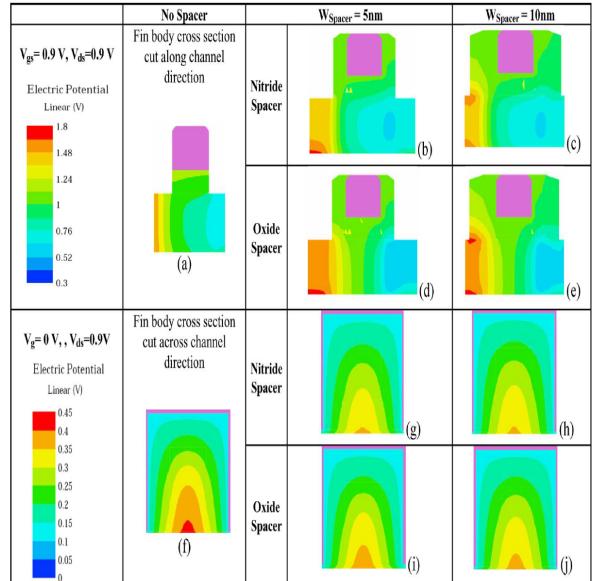
C does not suffer from any fringing capacitance because of the presence of surface gate electrode.

Fig. 11. On and OFF current for devices with different spacer widths and materials.



From Fig 11 it is significant that large fringing capacitance flows from sides of the gate to the source through the spacer which dominates the total gate to source capacitance. Due to this there is large variation in both I_{ON} and I_{OFF} . Device A and Device B have similar I_{OFF} current, but the I_{ON} is 44% more for device A. Device B and device C have similar I_{ON} but device C has 80% higher I_{OFF} than that of device C. From Fig 12, shows the I_{ON} and I_{OFF} of the devices with spacer made of material silicon oxide and silicon nitride. It is computed that spacer width that is larger than width of the gate under-lap region have constant I_{ON} . However, I_{ON} of the device without spacer is very much lower. This can be explained by plotting the potential across the channel for devices with nitride and with no spacer.

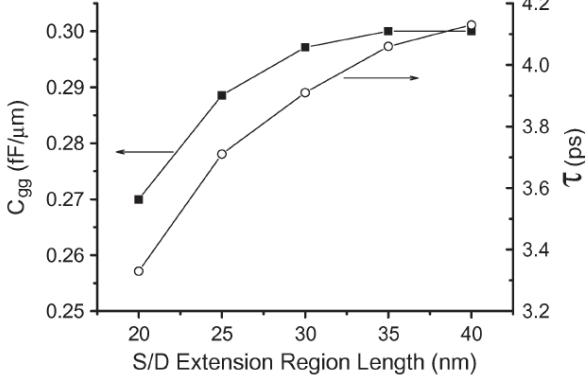
Fig. 12. Electrostatic potential plot for (a)-(e): $V_{ds}=0.9V$, $V_{gs}=0.9V$. (f)-(j) $V_{ds}=0.9V$, $V_{gs}=0V$. All devices are identical except for the width of spacers.



From the results of Fig. 12(a) the channel potential is higher

and potential gradient is lower for device with no spacer. Fig. 12(b) the device with thin spacer where the channel potential is low and the potential gradient is higher. [Fig. 12(c)] The channel potential is hardly affected due to much wider spacer. The reason why the fringing field is hardly affected in case of wide spacer is because the fringing field from the gate through the spacer gets terminated on lightly doped fin body. Fig. 12(d) and (e) shows the effect of the material type SiO₂, this yields lower ION as the fringing field is weaker due to low permittivity of SiO₂. Also due to back conduction from channel of fin body the IOFF increases in case of SiO₂. However from Fig. 12 (h) where the nitride spacer is used , the IOFF is noted to be low which gives better control of the body potential. The reason behind the better control of nitride spacer is that nitride has high permittivity. So we can a device which has a spacer of high permittivity and equals to the width of the gate is better design with improved performance.

Fig. 13. . gate capacitance and intrinsic delay potted with respect to S/D. Bias condition: V_{gs}=V_{ds}=0.9V and all devices have uniform spacer width of 10nm.



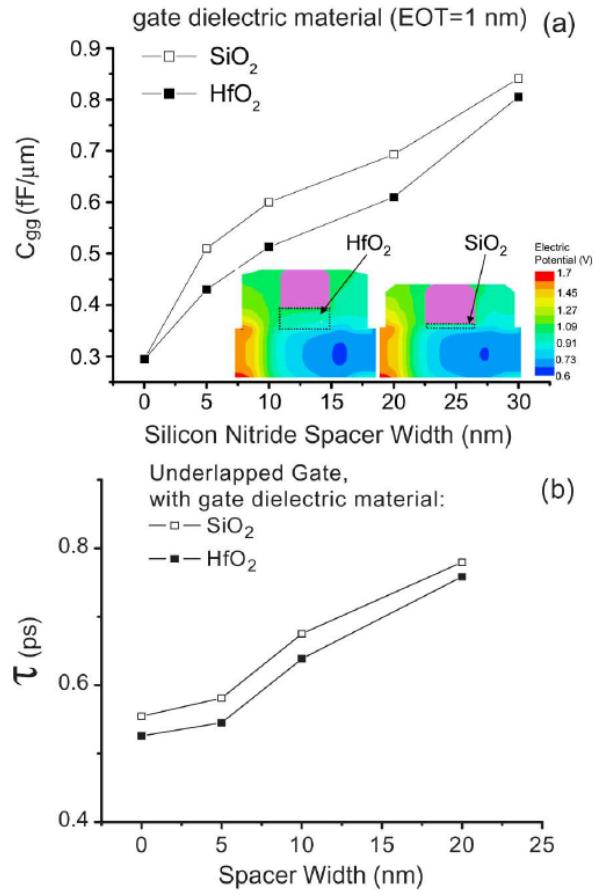
The another factor that is induced by fin body is series resistance. Since, the thinner fins are preferred for underlapping gate, the souce and drain can be made shorter which in turn reduces the series resistance. By doing this we can achieve improvement in drive current and switching speed performance. From the simualtion result in Fig. 13. increasing the souce/drain length will increase capacitance until the saturation is achieved. However drive current will be affected due to increase in series resistance. So by reducing the source/drain length by 40nm to 20nm we can achieve a reduction in switching delay by 20%.

B. Effect of High-k gate-dielectric:

Since the scaling of SiO₂ has reached its limit we need to replace it with a high-k gate-dielectric material. Hui et al have clearly shown from previous results that increase in gate di-electric will scale down the channel length. However, this induces fringing fields from the gate to the source/drain region which inturn affects the performance and give rises to V_t variation and short channel effects. A new 3-D model has been proposed to draw the comparison between various parameters which gets affected due to scaling of high-k device.

From Fig. 14. it is interpreted that when the device with high-k dielectric layer shows 20% less in total capacitance as

Fig. 14. (a) Total effective capacitance and (b) intrinsic gate delay with respect to silicon nitride space width for device with SiO₂ and HfO₂ gate-dielectric material of the same EOT(1nm).



compared to SiO₂ gate dielectric. The reason behind this is due to the spatial distribution of electric field when electric field is much larger due to thickness of the material used instead of thin sio₂. Due to which the vertical electric field in the dielectric layer and the channel is reduced. So consequently the figure shown in Fig. 14(a) is significantly affected by physical thickness of the dielectric material used.

On other aspect, when the dielectric thickness is scaled down, the capacitance value is increased. Also as the dielectric thickness reduces, the source/drain leakage, short channel performance, the drive current will improve. It is proved that when the dielectric thickness is down scaled by 2.5 times it only provides a impact of 26% with respect to performance. The reason behind this is the vertical field in the channel increase as the dielectric thickness is reduced which leads to mobility degradation. As a result we can conclude even thought high dielectric is used in 32nm technology due to leakage issue, better performance can still be achieved by down scaling the high-k dielectric thickness.

C. Effects due to Fin width and pitch:

When it comes to fin width, FinFET devices has smaller fin width due to scaling factor. Here we will discuss the impact of fin width and fin pitch. When it comes to series connection of

FinFET devices to enhance the performance the space between two fin is occupied by the gate electrode as long as the fin pitch is not greater than twice the length of gate electrode. Having said that, for a design only the top width of the electrode is dependent of gate material thickness and thickness of side gate is not a choice after the fin pitch is selected.

Fig. 15. Gate capacitance plot with respect to fin width for multifin device of different pitch. Vertical conduction of channel in multiple fins cause a source to fringing effect.

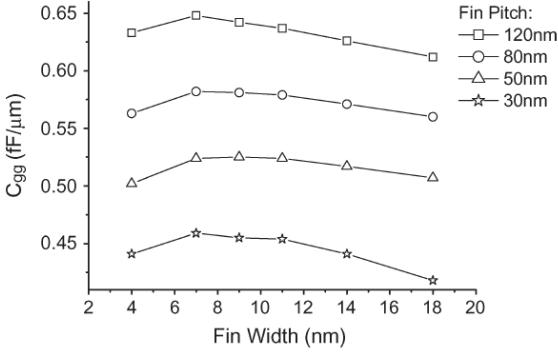
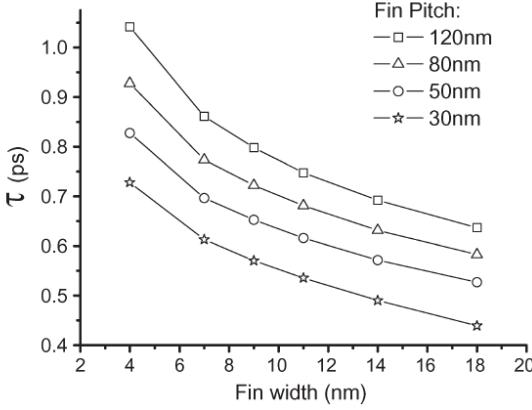


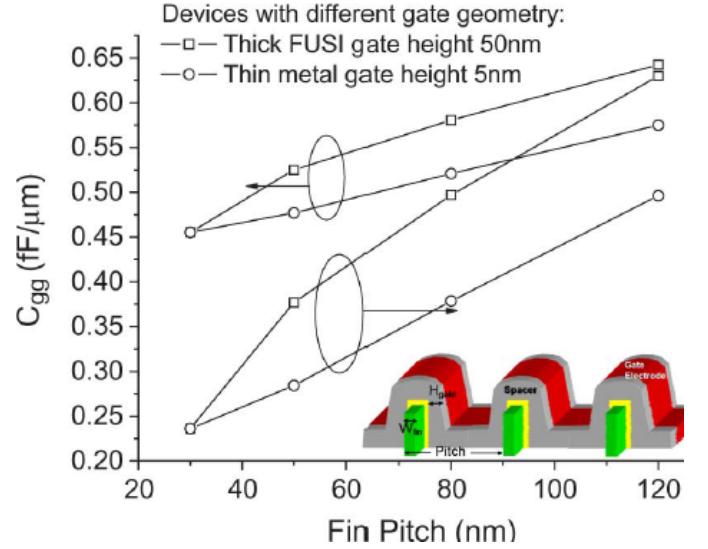
Fig. 16. . intrinsic delay against fin width for multifin device for different pitch. All device are considered to be 13nm



Hie et al proved for a given fin width, when pitch is increased by 4 times, the gate capacitance is increased by 50%. The reason behind is increase in gate to source capacitance and gate to bulk capacitance. From the Fig. 16. it is interpreted that when the fin pitch increases the intrinsic delay for all the fin width because of high fringing capacitance. So when we use a wider fin which has small pitch the delay seems to small. However, this happens with the trade to IOFF current which is more for wider fins.

A promising result is can be obtained with the help of novel gate-stack technology, where a very thin and high conductive metal gate electrode of 2-10nm believed to be feasible by reducing the fringing capacitance. This happens as the fringing field from the side of the gate electrode tends to weaken. From the Fig. 17. the simulation results shows the improvement in device performance when the parasitic capacitance is reduced. Also we can say when the fin pitch is larder than twice the

Fig. 17. comparison of intrinsic delay and total effective gate capacitance with respect to fin pitch for device with thick FUSI gate electrode and thin metal electrode.



fin width, the gate electrode improves the overall performance by 10%.

So generally speaking when the shrinking of FinFET device is done, the factors with respect to the geometry of the FinFET like Source/drain length, Pitch width, spacer and gate dielectric thickness all plays a major role in the performance of the FinFET Device. As the scaling of MOSFET is replaced by the FinFET scaling, the factors mentioned plays a major role in FinFET and they all add fringing capacitance to the gate which in turn reduces the performance by inducing delay and leakage current. So a path to new level of scaling is nominated as FinFET now the constrains have to be treated respectively to blow a new major change in semi conductor industry.

IV. SCALING ISSUES IN DESIGN:

As the scaling occurs in FinFET, there are few difficulties that has to deal with the design structure. Considering these factors the design of the FinFET is fabricated.

A. scaling issue in IDDG FinFET:

Two major types of double-gate FinFET are simultaneously driven DG (SDDG) and independently driven (IDDG). SDDG structures might have top gate which implies tri-gate FinFET but in case of FDDG the top gate is isolated by thick nitride layer. IDDG finfet is generally used in dynamic voltage threshold control and transconductance modulation. It has been showed that because of different front-back gate coupling, the threshold voltage V_t can be varied by changing the back gate voltage. The change in threshold voltage with respect to back-gate voltage is shown in Fig 18.

Where toxf and toxb are the oxide thickness of front and back gates. X_c is the distance of the charge from the centroid of front gate and W_{si} is the width of silicon fin.

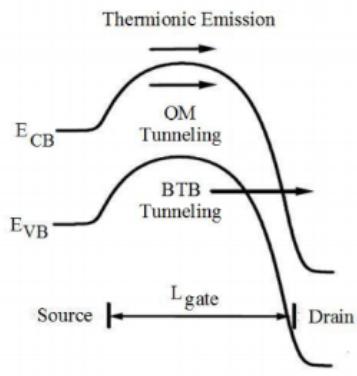
Fig. 18.

$$\frac{\partial V_t}{\partial V_{gb}} = \frac{-3t_{oxf} + X_c/3}{3t_{oxb} + (w_{Si} - X_c)}$$

B. Gate length scaling :

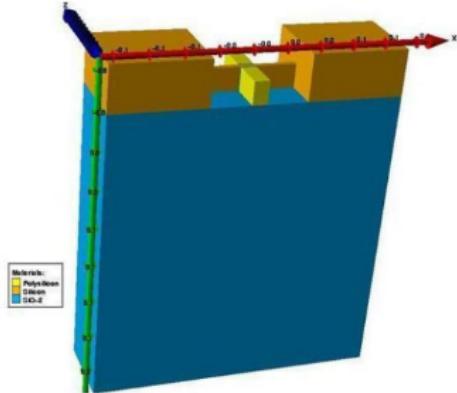
[6] Scaling of gate has been limited due to the off state leakage current. Scattering of channel is generally ignored in small channel length, but the off state leakage current is affected by thermionic emission above channel potential barrier, quantum tunneling mechanism between source and drain and band to band tunneling between the body and the drain. This is shown in the Fig. 19

Fig. 19. tunneling mechanism



[6] Varun et al has proved from the simulation results that as the Tbody reduces, leakage from the gate is completely eliminated which decreases the off state leakage current, short channel effect can be reduced drastically. When the Tbody = 4nm , Tox=1nm, high performance of leakage current specification is met at gate length of 10nm.

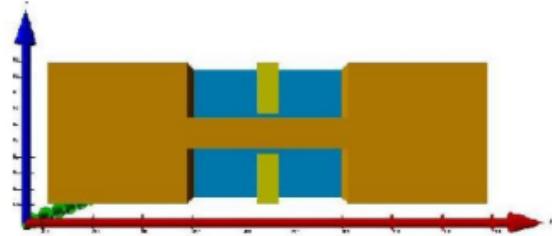
Fig. 20. Three dimensional structure of IDDG FinFET



C. Threshold voltage :

[6] Generally In nanoscale devices the threshold voltage is dependent on the gate function but in case of thin fin width

Fig. 21. Top View of IDDG FinFET



FinFET the fin width also plays a major role. Varun et al has shown from proved results that for thin fin width FinFET the threshold voltage fluctuation is highly significant and is caused by quantum mechanical effects. A fin thickness of 4nm can be used to reduce the threshold fluctuation and to obtain a good control for the gate over the channel.

TABLE II
DEVICE DIMENSION AND DOPING

Attributes	Values
L_g	10nm
t_{fin}	4nm
t_{ox}	1nm
H_{fin}	16nm
L_{ext}	16nm
Fin doping	$3.8 \times 10^{18} cm^{-3}$
Extension doping	$1 \times 10^{19} cm^{-3}$
S/D doping	$1 \times 10^{20} cm^{-3}$

From the Table. 2 we can see that the threshold voltage vary by 8% from its nominal value of 140mV as the impact of process variation. So for any value more than 4nm threshold voltage can be a concern which has to be taken in picture. When the gate oxide thickness is constant and the fin width is decreased the threshold voltage is increased. The energy level quantization increases the band gap for narrow fin devices. On top of this when gate oxide thickness is reduced the threshold value is increased. The ultimate reason behind this is the choice of gate work function which has been selected to provide a way to set off current, which puts the device in weak regime ($V_{gs}=0V$). So we can say when the gate oxide is thin, higher gate voltage is required to bring the device in inversion. Consequently, when the gate oxide thickness decreases in one hand the threshold voltage increases on the other hand. The transfer characteristics of 10nm IDDG FinFET is show in Table. 2.

V. DRAWBACKS IN DESIGN OF FINFET:

As the size of the mosfet gets reduced smaller and smaller, issues faced in the performance of the device increases. Few major issues are leakage current from gate to channel and short channel effect where the gate loses the control on the channel. FinFET seems to be a promising candidate to get rid of these issue and provide a better control of the device which increases the reliability along with the performance of the device. Since the entire design flow is changed with respect to new base design structure of FinFET, the entire tool chain is affected from the base transistor level modeling, physical extraction, verification, simulation tools, validation of models, library has to be changed with respect to the new design structure from fundamental level of architecture. So measure have to be taken to maintain the previous design flow which enable quick transparent adoption of new FinFET structure.

A. Corner Effect:

[2]Reduction of fin-width reduces the short channel effect but at the time this induces more parasitic resistance of source/drain which reduces the drive current of the device. Also when the fin-width is very thin the dissipation of heat comes into page and brings a major challenge in the performance of the device. Considering tri-gate FinFET where the channel is enclosed by gates in two vertical and one horizontal direction the sharing of charges occurs at the two adjacent corners of the gate. The gate to channel electric field is accumulated in the corner of the gate fin. Due to this the gate to source input voltage increases towards the device threshold voltage, this in turn induces leakage of sub threshold voltage at the corners of the fin. This effect is called corner effect which reduces the threshold characteristics of the FinFET device leading to high off state leakage current. An approach to get rid of accumulating charges in the corner is found to be making the corner as a curved profile as show in the Fig. 23. However, the electric field crowding on the corner is reduced by new profile, this increases the challenge in parasitic extraction. So moving on with other possible methods such as reduction of oxide thickness and reduction of doping concentration in the channel. When the fin width is smaller than the radius of the curvature of the corner, the sub threshold leakage current increases.

Fig. 22. Cross sectional view of conventional Tri-Gate FinFET

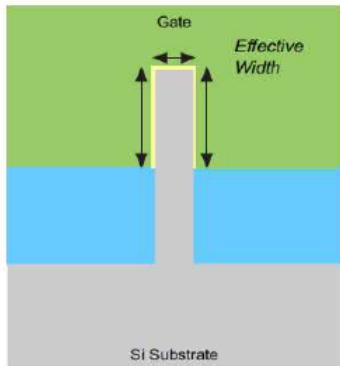
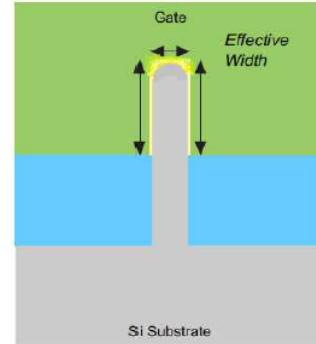


Fig. 23. Cross-sectional view of curved Tri-Gate FinFET



B. Challenges with fabrication :

The si surface of the fin is different from that of the bulk, after usual pre gate clean oxide a lot of si loss is noted. Wet cleans can be a alternate method for this case. Apart from this, oxidation effect on the corner and tip of the fins happens faster. Since, the fin shape is thin the low-doping on channel is preferred which reduces the sub threshold leakage. This leads to complex and expensive work function for the implementation of the gate.

C. Quantum effects :

[2]The thickness of the FinFET plays a key role. If the thickness of the FinFET is very much large then the electrostatic influence of the gate will get weaker due to thick Fin walls around it and this makes the fin to act like a bulk substrate loosing the small size and the benefits of the FinFET topology. If the thickness of the FinFET is very thin then density of the electron is reduced. Under the normal conditions these free electrons have sufficient energy to reside in the conduction state and they start to conduct current in the transistor channel. The electron energy and band level are the strong functions of applied voltage and temperature. At normal conditions there is no shortage of available free states for the electron at the band edge. However, quantum effect on thin fins reduces the density of available free states which makes the available electron/hole to require more energy to occupy the states more than the band energy.

D. Double patterning :

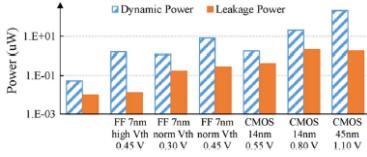
[2]As the size of the FinFET go low there are few new challenge that comes into picture. The design of 20nm FinFET is done using double patterning where two masks are used to print alternating features. This determines how the layout features will be implemented. Layout dependency effects (LDE) occurs where the layout features are placed close the cell will suffer from time and power issues. Electro-migration comes into play as the geometry shrink. Double patterning will make fabrication of 20nm possible but when it goes to 10nm a new approach is required which can be full filled by side wall image transfer. However the fabrication gets complex when its goes below 10nm.

VI. ANALYSIS OF POWER CONSUMPTION IN FINFET:

The estimation of power consumption in FinFET consists of two parts, which involves leakage power consumption and dynamic power consumption. The estimation of leakage power consumption is done by adding all the leakage power consumption of all cells that are not power gated. The estimation of dynamic power consumption depends on switching activities of all the nets in the circuit, so we need a logic synthesis tool, gate level simulator and power analysis tool to provide an accurate estimation of dynamic power consumption.

[3] Qing et al has shown a method to do this where a benchmark circuit is first synthesized using a standard cell library to obtain synthesized netlist and a standard delay format for the gate-level simulator. A file which contains the state-dependent and path-dependent information of all standard cells is generated for every single cell library. Basically the gate-level simulator collects the information about switching activities in all nets of the netlist and logs it in a backward file. The power analysis tool uses this backward file along with the power analysis parameter in the standard library to estimate the power analysis result. This flow can be used to determine power consumption for a 7nm FinFET device. Although, this method estimates the power consumption in FinFET the capacitance is being ignored here. It is noted that the netlist circuit for 7nm FinFET 14nm/ 45nm MOSFET have different threshold voltage but this difference in threshold netlist does not affect the power analysis. The benchmark of different standard library is show in the Fig

Fig. 24. Dynamic and leakage power consumption of c432 benchmark for standard cell libraries



A. Results for the benchmark circuit:

[3] Qing et al has showed the results for the power consumption in FinFET. The complete results are shown in the table (3) and (4) below. We can observe that there is significant improvements in the 7nm FinFET is achieved, when we apply super threshold voltage to the 7nm FinFET device which operates normal threshold voltage we observe almost 3x/15x increment in the speed of 7nm FinFET with respect to 14nm/45nm CMOS. At the worst case when the operating is at the near threshold regime the speed increment is done by 7x times.

In addition to this, the power consumption is very low for every operation in 7nm FinFET when compared to MOSFET under test. Results show that energy reduction in 7nm FinFET is observed to be 5times less for 14nm CMOS and 600times less for 45nm CMOS. The table 4 breaks the power analysis into dynamic and leakage park.

TABLE III
CIRCUIT DELAY/CLOCK PERIOD AND ENERGY CONSUMPTION PER OPERATION

CIRCUIT DELAY/CLOCK PERIOD AND ENERGY CONSUMPTIONS PER OPERATION

Benchmark circuits	Circuit delay or clock period (ps)						Energy consumption per operation (J)					
	FinFET 7nm		CMOS 14nm		NCSU 45nm		FinFET 7nm		CMOS 14nm		NCSU 45nm	
	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}
V _{dd}	0.30V	0.45V	0.30V	0.45V	0.55V	0.80V	1.10V	1.10V	0.30V	0.45V	0.30V	0.45V
c432	1.292	164.3	172.8	80.5	795	220.0	1.460	0.083	0.264	0.237	0.697	1.725
e880	1.025	126.7	154.9	74.9	810.1	183.7	1.060	0.154	0.505	0.228	0.632	1.401
c1355	1.031	123.4	161.4	79.4	702.5	156.0	1.020	0.286	0.992	0.462	1.383	2.266
e1908	1.320	160.3	190.8	93.1	1.118	227.7	1.260	0.224	0.736	0.334	0.932	4.680
e2670	1.196	151.4	142.7	67.1	944.9	210.3	1.300	0.282	0.935	0.434	1.246	2.358
c3540	1.658	204.8	238.5	117.7	1.281	291.1	1.790	0.504	1.583	0.792	2.070	5.101
16-bit adder	637.4	70.2	163.3	68.5	450.7	97.6	1.010	0.111	0.384	0.251	0.650	1.762
16-bit multiplier	1.606	201.3	214.3	107.3	1.039	235.1	1.440	0.964	3.276	1.363	4.018	6.244
s820	330.6	45.28	41.8	21.1	262.8	49.68	360.0	0.075	0.267	0.110	0.345	0.972
s1196	942.0	116.6	134.5	57.8	684.6	158.1	1.010	0.150	0.464	0.409	1.224	1.362
s1423	2.323	280.7	313.2	154.1	1.840	405.7	2.040	0.228	0.405	0.363	0.826	2.392
LEON2 SPARC	2.600	520.0	650.0	325.0	3.250	500.0	650.0	8.66	20.70	28.70	52.30	364.40
												516.9
												16,837

TABLE IV
DYNAMIC AND LEAKAGE POWER CONSUMPTION

DYNAMIC AND LEAKAGE POWER CONSUMPTIONS

Benchmark circuits	Dynamic power consumption (uW)						Leakage power consumption (uW)					
	FinFET 7nm		CMOS 14nm		NCSU 45nm		FinFET 7nm		CMOS 14nm		NCSU 45nm	
	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}	High V _{th}	Normal V _{th}
V _{dd}	0.30V	0.45V	0.30V	0.45V	0.55V	0.80V	1.10V	1.10V	0.30V	0.45V	0.30V	0.45V
c432	0.054	1.593	1.20	0.839	1.75	21.29	223.9	0.013	0.13	0.17	0.27	0.42
e880	0.13	3.96	1.12	0.789	1.12	11.45	403.2	0.021	0.029	0.35	0.55	0.61
c1355	0.24	8.00	2.39	1.68	2.38	27.70	990.8	0.028	0.038	0.47	0.74	0.85
e1908	0.14	4.56	1.34	0.938	2.94	36.82	508.1	0.024	0.031	0.41	0.63	1.25
e2670	0.20	6.13	2.42	1.764	1.61	16.47	836.9	0.032	0.045	0.62	0.93	0.89
c3540	0.25	7.65	2.31	16.03	2.25	25.01	1.076	0.038	0.076	0.20	0.56	0.73
16-bit adder	0.16	4.25	1.00	0.65	4.00	2.03	400.0	0.019	0.026	0.20	0.31	1.18
16-bit multiplier	0.53	16.18	5.19	35.63	4.51	50.30	2.045	0.070	0.095	1.17	1.82	1.5
s820	0.21	5.88	2.33	15.92	2.96	47.23	357.2	0.018	0.024	0.29	0.46	0.74
s1196	0.13	3.94	2.53	20.39	1.08	11.18	441.3	0.029	0.040	0.51	0.78	0.91
s1423	0.07	1.40	0.65	4.56	0.58	5.88	620.1	0.032	0.043	0.51	0.80	0.72
LEON2 SPARC	4.08	86.6	21.28	131.2	21.09	353.7	7.483	2.45	3.4	42.61	66.2	67.5
											197	691.1

VII. CONCLUSIONS & DISCUSSION:

The FinFET becomes a promising VLSI technology for the future of semi conductor industry due to its extraordinary properties. FinFET stands to be the candidate that extends the Moore's law and provides a new path way for the semi conductor industry an it is clearly known FinFET will be the new booming technology for this decade. A 7nm FinFET circuit with normal threshold voltage consume 600x less energy on average and 7nm FinFET circuit with high threshold voltage consume 1000x compared 14nm and 45nm CMOS circuit. This pretty much explains, FinFET shows up being a excellent technology that provides a very good performance at very low size and also consumes very low power. Having discussed the challenges faced in FinFET technology with respect to self heating, reliability, Fringing effects, Design constraints, Fabrication process yet FinFET stands on top of the transistor design. FinFET allows the scaling beyond 22nm because of its complex geometry properties. With further more research, new approaches can be found to reduce the issues faced in FinFET rather than existing approach that only acts as a trade off with another parameter.

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