ROCHESTER INSTITUE OF TECHNOLOGY

EEEE:722 - Lab Report

Perl Project

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Abstract

The perl project is about generating RTL and test bench. The ultimate aim of the project is to learn perl scripting and how to auto generate code irrespective of the variables used in it. The perl scripting is very useful in generating explicit code.

Perl borrows syntax and concepts from many languages: awk, sed, C, Bourne Shell, Smalltalk, Lisp and even English. However, there are some definite differences between the languages.

A Perl program consists of a sequence of declarations and statements, which run from the top to the bottom. Loops, subroutines, and other control structures allow you to jump around within the code. Every simple statement must end with a semicolon (;).

Perl is a free-form language: you can format and indent it however you like. Whitespace serves mostly to separate tokens, unlike languages like Python where it is an important part of the syntax, or Fortran where it is immaterial.

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1 Introduction:

This project focus on generating VERILOG RTL / TEST BENCH for shift registers. The Perl script is used to generate the code. The parameters for the shift registers are width (number of bits), stages (number of shift registers), reset (value assigned to shift register) , outputfile name (the name on which the module and verilog.v file should be created).

The parameters for verilog could be given in two ways. Either user can give the values in command line or they can have a file with values. Either case, perl script has to accept these values and generate verilog and testbench respectively.

2 Parameters:

The parameters has it own limit and so user should select the values between those values width should be between 1-64. stages should be between 1-128. Reset shoule be less than 2*width. If these restrictions are not followed by the user, the perl script should throw an appropriate error.

The format on command line is -width -stages -reset -outputfile

PROGRAM FLOW: The program consists of 2 sub routines, One for RTL and One for Testbench. The values on which the shift register has to be generated is extracted from the user as discussed above. 000000000000000

3 BUGS:

There is no bugs, the program works fine with respect to user input and parsing the values

4 ACKNOWLEDGEMENTS:

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5 AUTHOR:

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