2020

Integrated Process Technology

FINAL REPORT

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UNDER GUIDANCE :

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Abstract

The following report is a complete explanation of manufacturing a solar cell from the scratch. This report explains the Procedures, rules and calculation for designing and manufacturing the solar cell. It contains a list of tables and figures Which can be helpful for future usage. This report does not explain more about the CleWin5 software which I used to Create the mask design but it will demonstrate the rules which should be consider while designing the mask. My own Design and process flow images are given in the Appendix.

Introduction :

This report represents the process flow of manufacturing a solar cell with the help of silicon wafers, testing the finished product and documenting the results. The process flow consist of 7 unique steps from designing the solar cell to making an electrical characterization of solar cell. Silicon is most commonly used for producing the solar cell because of its easily available and can be produced in high purity and in single crystal can be doped as an n- and p- type semiconductors. The most commonly used method of producing silicon wafer is known as Czochralski method, which produces long monocrystalline rods so-called seed crystals which can be cut into desired shape.

Photovoltaic Cell :

A photovoltaic (PV) cell, also known as a solar cell, is an electronic component that generates electricity when exposed to photons, or particles of light. A photovoltaic cell is made of semiconductor materials that absorb the photons emitted by the sun and generate a flow of electrons. When the photon strikes a semiconductor materials like silicon, they release the electrons from its atoms, leaving behind a vacant space. The stray electron move around randomly looking for another “hole” to fill.

A photovoltaic cells need to establish an electric field, much like an magnetic field which occurs due to opposite poles, an electric field occurs when opposite charges are separated. A photovoltaic cell is comprised of a junction of two semiconductors materials known as p-type semiconductors and n-type semiconductors. The p-type material has the tendency to give up the electrons (creation of holes), whereas n-type material has the tendency to accept electrons.

When the electrons are excited by the photons, they are swept to the n-side by an electric field, while the holes drift to the p-side. The electrons and holes are directed to the electrical contacts applied to both the sides before flowing to the external circuit in the form of electrical energy. This produces direct current. An anti-reflective coating is added to the cell to minimize photon loss due to surface reflection [1].

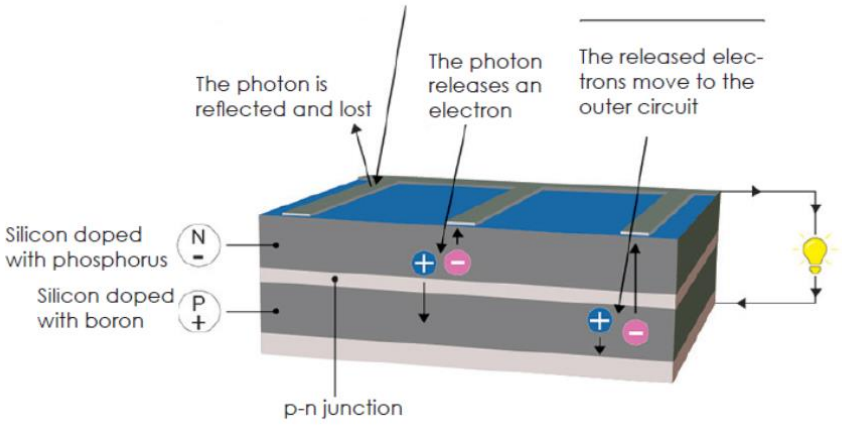

Figure 1 : Photovoltaic cell working [1].

Electrical Background :

Equivalent Circuit :

While manufacturing a solar cell the electrical background and their parameters should be taken into consideration. Every solar cell consist of an equivalent circuit from which one can easily study the nature of working and the parameters changes. Every solar cell consist of basic components that can be fitted together to study their nature of working, one such circuit is shown below.

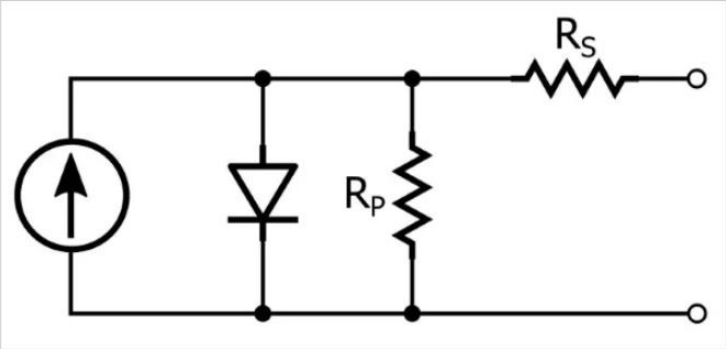

Figure 2 : Equivalent Circuit [2].

The idea here is that solar cell generates an internal current corresponds to the light intensity. Not all of this current is available to the load, because some flows through the parallel diode and some flows through the parallel resistance (R_P) [2].

When no load resistance is present, the voltage available at the terminals of the solar cell is determined by the interaction of the current source with the parallel diode and the parallel resistance. This is called as “Open – Circuit Voltage”. If the circuit is still supplying load current, the voltage at the terminals will be lesser than the open circuit voltage, since some of the voltage is dropped across series resistance.

Voltage or current Source ?

From the technical terms we understood that solar cell is neither voltage source nor current source. But I can power a circuit in voltage – source style. The additional components in the equivalent circuit indicates that the internal current source is not in direct interaction with the load components. The cell will always generate a voltage because of the internal current flows through the internal diode and R_P [2].

The irradiance in an indoor environment might be 10 or 20 W/m^2 , and direct sunlight outdoors might give you 900 W/m^2. So, in practical usage the supply voltage must be higher when compared to original voltage.

In practical point of view, a solar cell can be manufactured in such a way to favour voltage or current : high current capacity is obtained by filling the available area with one pn junction, and higher voltage is obtained by splitting the area up into multiple junctions and connecting them in series.

Peak Power :

The peak power can be obtained by controlling the current and voltage characteristics by changing the device's physical configuration. A small example is shown below, what happens when the necessary changes are made to the circuit.

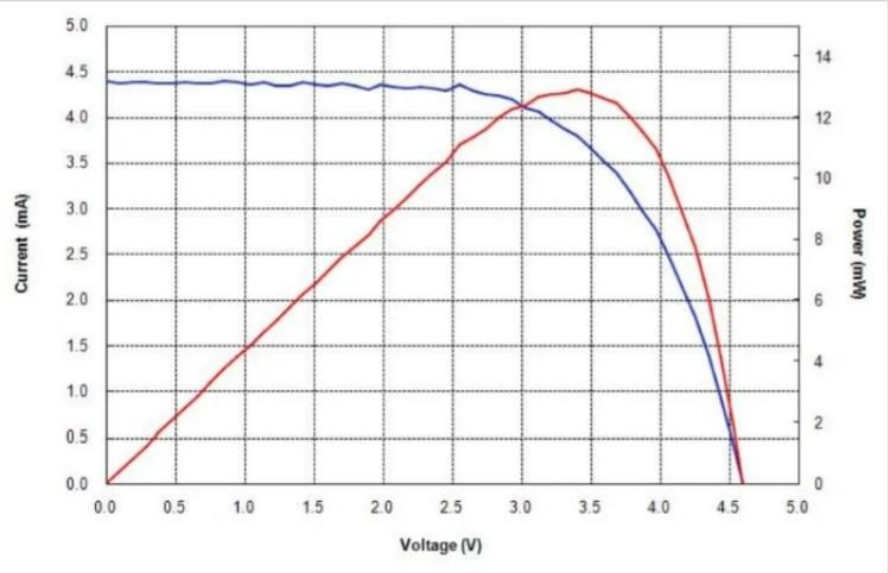

Figure 3 : Peak Power [2].

In this graph, the red curve is the power and the blue curve shows the voltage provided by the cell at a given load current. The plot shows that circuit can operate at maximum power but its not a good practice to extract power from the sunlight falling on the solar cell.

Fill Factor :

The fill factor is the ratio between the maximum power ($P_{max} = J_{mpp}\ V_{mpp}$) generated by a solar cell and the product of V_{OC} with $J_{SC.}$

$$\text{FF} = \frac{Jmpp\ Vmpp}{Jsc\ Voc}$$

The subscript "mpp" denotes the *maximum power point* (MPP) of the solar cell, i.e., the point on the J – V characteristics of the solar cell, at which the solar cell has the maximal power output. To optimise the operation of PV systems, it is very important, to operate the solar cells at the MPP.

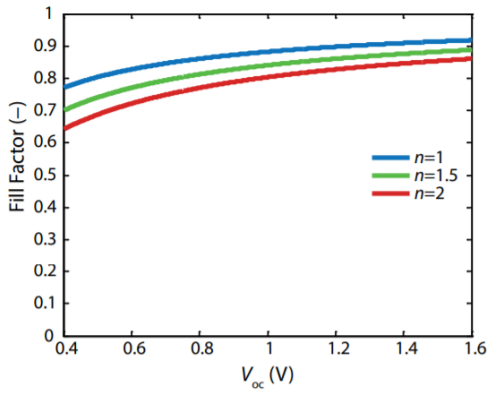

Figure 4 : The FF as a function of V_{OC} with ideal diode behaviour [3].

Assuming that the solar cell behaves as an ideal diode, the fill factor can be expressed as s function of open – circuit voltage V_{OC},

$$FF = \frac{Voc - \ln(Voc + 0.72)}{Voc + 1}$$

Where,

$$v_{OC} = V_{OC}\frac{q}{KBT}$$

is a normalised voltage. The above figure shows that FF does not change drastically with a change in V_{OC}. For a solar cell with a particular absorber, large variations in V_{OC} are not common. The above graph demonstrates the importance of the diode ideality factor when introduced into the normalised voltage in the above equations. The ideality factor is a measure of the junction quality and the type of recombination in a solar cell. For the ideal junction where the recombination is represented by the recombination of the minority carriers in the quasi – neutral regions the *n* is equal to 1 [3].

I – V Characteristics Curves :

Solar cell I – V characteristics curves are graphs of output voltage versus current for different levels of insolation and temperature and can tell about PV cell or panel's ability to convert sunlight into electricity. These curves provide the information needed for us to configure a solar power array so that it can operate as close as possible to its maximum peak power point [4].

Open – circuit solar cell :

In this open – circuit solar cell the current is zero, so the solar cell delivers maximum voltage, since the output power is determined as :

$$I = \{ I_S [\exp(qV_{OC} / KT) - 1] - I_{ph} \} = 0$$

$$P = I * V = 0$$

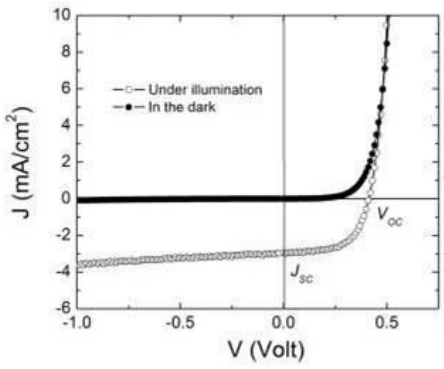

Figure 5 : Open – Circuit Solar cell.

Short – Circuit Solar cell :

In this short – circuit the voltage across the diode is zero, so the solar cell provides maximum current into the circuit, since the output power is determined as :

$$I_{SC} = \{ I_S [\exp(qV / KT) - 1] - I_{ph} \}_{V = 0}$$

$$I_{SC} = I_{ph} = -qAG(L_h + L_e)$$

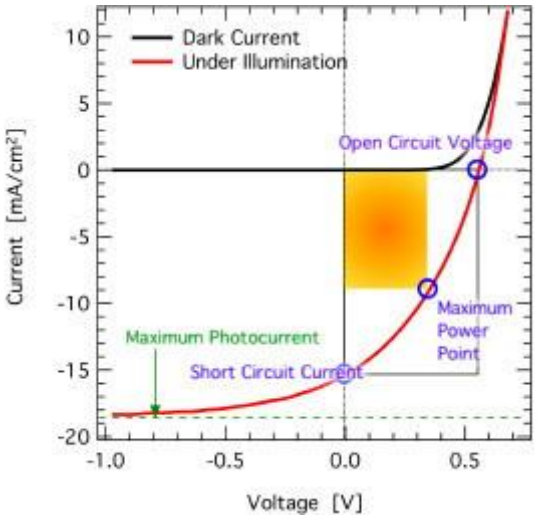

Figure 6 : Short – Circuit Solar cell [5].

Process Flow :

Process flow is a blue print for preparing the silicon wafer before manufacturing. The process flow for solar cell consist of 17 steps which have been displayed below. These steps are followed to manufacture the solar cell from the scratch.

Step 1 :

A silicon wafer is doped with p-type impurities and then both sides of the silicon wafer are oxidised, while the boron is doped on one side of the wafer.

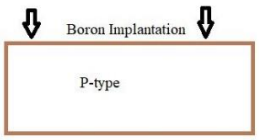

Figure 7 : Boron implantation.

Step 2 & 3 :

Deposit photoresist on front side and performing oxide etching from the back side with the help of BHF. Then the photoresist is removed.

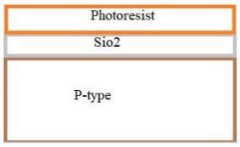

Figure 8 : Photoresist.

Step 4 & 5 :

Now removing the photoresist on the top side and then oxidising to maintain a positive charge on the lower side of the wafer, while the new layer of photoresist is applied on the lower side of the wafer.

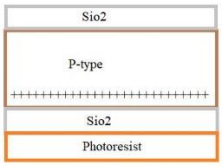

Figure 9 : Photoresist.

Step 5 & 6 :

Oxide etching takes place on the front side and the removal of photoresist takes place from the back side and the wafer is doped with phosphorus.

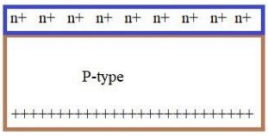

Figure 10 : Phosphorus doping.

Step 7 & 8 :

Oxidation process takes place and then photoresist is provided, while then the wafer is exposed to the light with the mask (Photolithography).

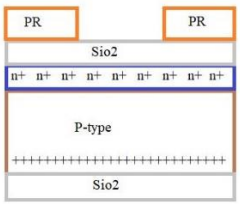

Figure 11 : Photolithography.

Step 9 & 10 :

Oxide layers and photoresist are removed and then aluminium is provided on the wafer.

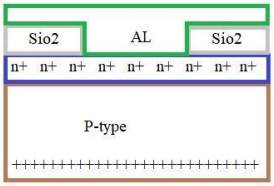

Figure 12 : Aluminium.

Step 10 – 17 :

Resist coating is made on both the sides and exposure and development takes place on the front side. Finally the photoresist is removed from the front side and the desired structure is obtained.

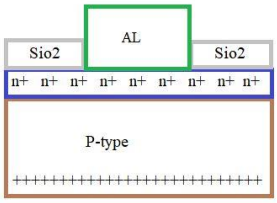

Figure 13 : Final design.

These above shown images are followed in order to get the exact result for the structure. These designs are usually produced by using a software known as CleWin5 from which the design of the structure that is to be used as a mask for the design is imprinted. A overall view of the process flow is given in **Appendix A**.

Mask Design with CleWin5 :

The first step of this solar cell manufacturing is to produce an exact and proper mask design which has to implanted to the silicon wafer. The design is carried into photolithography process where it is exposed for some time in order to get the desired design onto the wafer. The development for solar cell mask design consist of three stages namely :

- Creating contact mask
- Aluminium mask
- n well mask

First mask is used for etching contact areas (contact) through anti-reflective coating (Sio_2) and the second mask for structuring the Al conductor lines (aluminum). The third mask will help in separating the different areas in the solar cell [6].

The mask consist of borosilicate, soda lime glass or quartz plate, one side is coated by thin layer of chromium of 100nm, this chromium layer is structured by etched openings. The chromium is coated with photoresist of 500nm, the resist is structured in a lithographic process and then the resin is removed [6]. The exposure can be done based on the design pattern. For solar cell we did for around 9 seconds in the photolithography process.

Alignment Keys :

Alignment of the wafer with respect to the machine plays an important role in manufacturing the solar cell. Because an improper alignment may lead to lousy structure over the wafer and this in turn leads to less efficiency of the solar cell.

For the alignment there are special key drawings on each layer, the keys are fitting in each other. **Vernier structures** are very useful for direct visualization of the misalignment, without the need to measure distances of the structures [6].

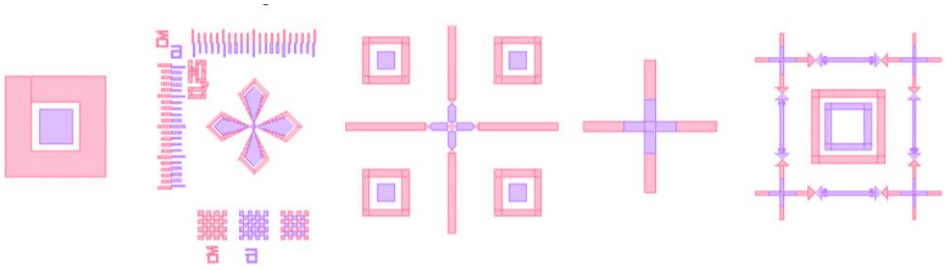

Figure 14 : Different alignment key combination [6].

The above shown are some alignment key combination which can be used for alignment in the photolithography process. In the process of creating the solar cell our design consist of one such alignment key, and this is used for aligning the mask to the wafer.

In our solar cell design the “contact” mask and the “Aluminium” mask are aligned with two alignment keys.

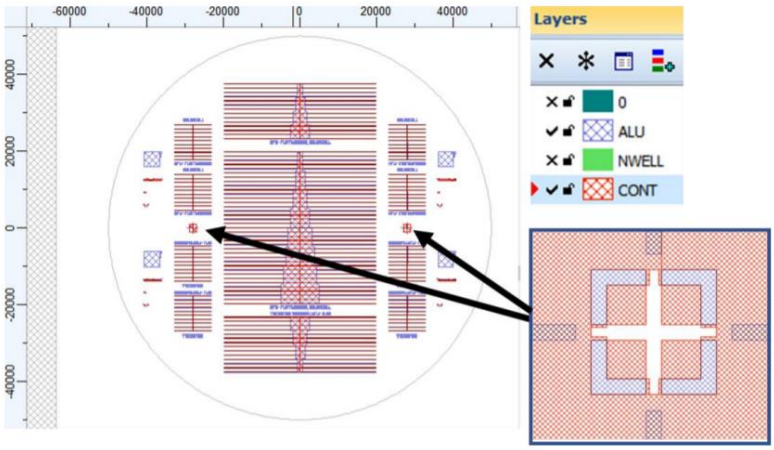

Figure 15 : Alignment key position in solar cell [6].

Design Rules :

There are some design rules which should be followed in order to extract the maximum efficiency out of the solar cell.

- All polylines should be closed.
- All closed polylines will be completely filled-out on the inside.
- Polylines crossing themselves will produce data errors.
- Polygons should show no more than 1,000,000 vertices.
- Design centre has to be in the centre coordinate (x = 0, y = 0) [6].

These are some rules which are followed while designing the solar cell mask.

	Area of cell 40 mm x 40 mm	Area of cell 40 mm x 15 mm	Area of cell 10 mm x 10 mm
a) Al line width	100 µm		20 µm
b) Contact width (under Al line)	50 µm		10 µm
c) Distance between Al fine lines	1 mm		
d) Width of collection Al lines near **bond pad (= thick side of the Al contact)**	10 mm	5 mm	200 µm
e) Width of collection Al lines opposite to bond pad	1.25 mm	1.25 mm	100 µm
f) Numbers of steps in width of collection Al lines	8 steps	4 steps	2 steps
g) Overlap of Al over contact (each side) (alignment accuracy)	25 µm		5 µm
h) Distance between n-wells	3 mm		
i) Distance between Al and n-well, next do the bond pad (at the pad side)	200 µm		

Figure 16 : Design rules for solar cell [6].

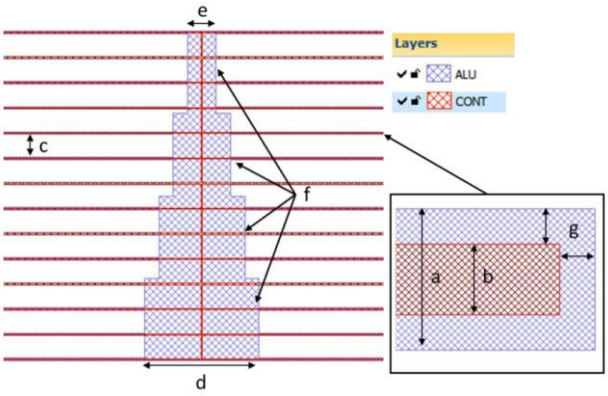

Figure 17 : Design rules visualization [6].

Designing of Mask :

While designing the mask the above mentioned rules are followed. As mentioned in the above the design of the mask in three different areas which are shown below.

N well mask with 3 different solar cell areas.

- 1 cell with 40mm * 40mm
- 2 cells with 40mm * 15mm
- 8 cells with 10mm * 10mm

The contact mask, aluminium mask and the n-well mask has been shown below, where as the completed design is shown in the Appendix.

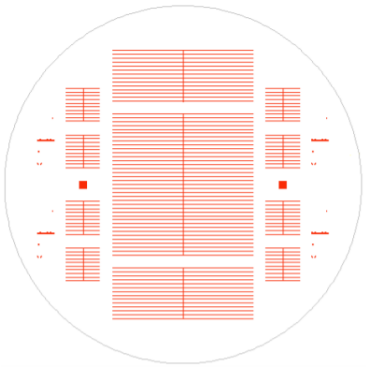

Figure 18 : Contact mask [6].

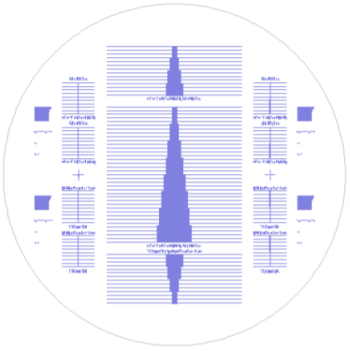

Figure 19 : Aluminium mask [6].

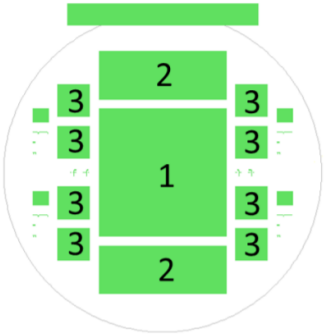

Figure 20 : n-well mask [6].

Phosphorous Doping :

Doping simply means including impurities into the semiconductor in order to conduct electricity. Doping usually depends on diffusion rate and the temperature at which the impurities are added. Phosphorous sits next to the silicon in the periodic table, that means it has one electron more than the silicon. When these two atoms combine the four electrons in the phosphorous will combine with the silicon while the fifth electron will be set free which act as a charge carrier. The doping is based on this process.

Diffusion is a thermally activated, unordered movement of atoms, which is often described as adding impurities in the crystal lattice. This diffusion process is based on **Fick's law** which states that the particle current is proportional to the concentration gradient [7].

$$j = -D\frac{dc}{dx}$$

For a constant concentration C_0 at x=0 (continuously delivery through the gas phase) the concentration profile is :

$$c(x, t) = c_0 \left[1-\frac{2}{\sqrt{\pi}} \int 0 \; e^{\xi 2} \, d\xi\right]$$

The phosphor doping consists of two steps :

- Deposition of dopant.
- Diffusion of the dopant into the silicon lattice (drive – in).

Firstly the wafer is placed in the oven and the selection of program has been set in the oven. This contains a list of data which should be followed. A mixture of nitrogen, phosphorous oxychloride ($POCl_3$) and oxygen is fed into the quartz tube. Oxygen is added to form phosphorus pentoxide (P_2O_5) at a temperature of 875ºc.

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

At high temperature phosphorus pentoxide formed a layer on silicon wafers and then is reduced to phosphorus by silicon :

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$$

The phosphorus pentoxide on the other hand mixed with the formed silicon dioxide, liquid phosphorus pentoxide was formed. After solidification the liquid becomes phosphosilicate glass :

$$P_2O_5 + SiO_2 \rightarrow P_2O_5 - SiO_2 \ (liquid)$$

The formed phosphorus cannot be able to dissolve with the silicon so it forms a new state SiP which forms a crystals on the surface of the silicon.

$$2P_2O_5 + 9Si \rightarrow 4SiP + 5SiO_2$$

The main step after the deposition of dopant is the diffusion process. It takes place at high temperature of about (1000º). The growth of the oxide occurs between the silicon (respectively the SiP deposits) and the $P_2O_5 - SiO_2$ liquid melt, therefore the surface is raised. Phosphorus atoms move into the silicon lattice and the SiP decreases its phosphor content until the phase is transferred again to crystallin silicon [7].

Spin Coating :

This spin coating process is one of the most important process in the solar cell manufacturing. Spin coating is the process of coating the wafer with photoresist which is an integral aspect of the photolithography. Depending on the requirements and the substrate topography, they can be divided into :

- Spin coating.
- Spray coating.
- Dip coating.

But in the report only the spin coating method is studied and observed. The process of spin coating is described as follows :

- Wafer is placed on the spin coating machine and the photoresist solvent is poured onto the centre of the wafer (carefully without forming any air bubbles).
- Then the lid is closed, while the acceleration, time and RPM are set as per the requirements.
- Acceleration = 25 * 100 RPM (s) – constant
- Time of rotation = 25 sec – constant
- Speed = based on the requirements

The spin coating works on the principle of centrifugal force which helps the resin to spread evenly onto the surface of the wafer, while the excess photoresist is spun off the edge of the substrate. Film thickness depends on some factors such as :

- Viscosity of the photoresist.
- Drying rate.
- Percent solids.
- Surface tension [8].

The next step in the spin coating is the **soft baking**. Soft baking is nothing but keeping the wafer in an oven for a certain time for about **100ºC**. This is done to clear off some the photoresist which are not spun off during the spinning and also in some places the solvent concentration is not linear, which in turn affect the thickness of the photoresist. The subsequent soft bake reduces the remaining solvent concentration to values of typically 5% [8]. Spin coating is normally

first done with dummy wafers until the ambient solvent saturation in the spin coater reduces and then the original wafers are used.

We used two photoresist namely AZ4562 (thick photoresist) and S1818 (thin photoresist) for the spin coating in which the results are observed and demonstrated below. We spin coated the wafers with different speed for thin and also for thicker photoresist, which are all observed and shown below.

The observation was done on the wafer in 5 places from left to the right which is pointed as 1 – 5 in which point 3 is the centre. The left position is defined while the **wafer's flat side is facing onto the person**.

Thick :

RPM's = 3800; 2650; 5300

Thin :

RPM's = 2200; 4800; 3600

Thick (5300 RPM) before baking & after baking :

Table 1 : Before and after baking of thick film.

Point of measurement	Before baking (nm)	After baking (nm)
Point – 1 - Left	3801.4	5589.9
Point – 2	3812.3	5348.9
Point – 3 - Centre	2749.7	4845.5
Point - 4	3261.2	5419.7
Point – 5 - Right	3322.9	5931.2

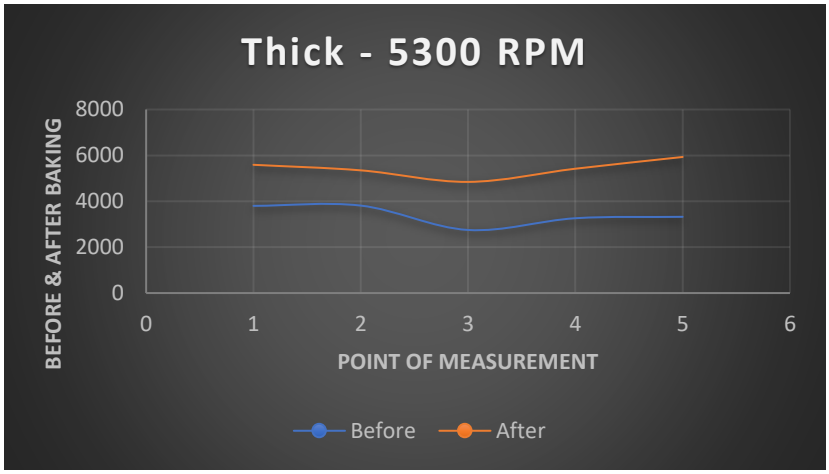

Chart 1 : Thick film before & after baking.

Thin (4800 RPM) before & after baking :

Table 2 : Before and after baking of thin film.

Point of measurement	Before baking (nm)	After baking (nm)
Point – 1 - Left	2093.6	1707.7
Point – 2	2033.5	1672.8
Point – 3 - Centre	2029.6	1670.6

Point – 4	2017.9	1668.3
Point – 5 - Right	2106.8	1740.8

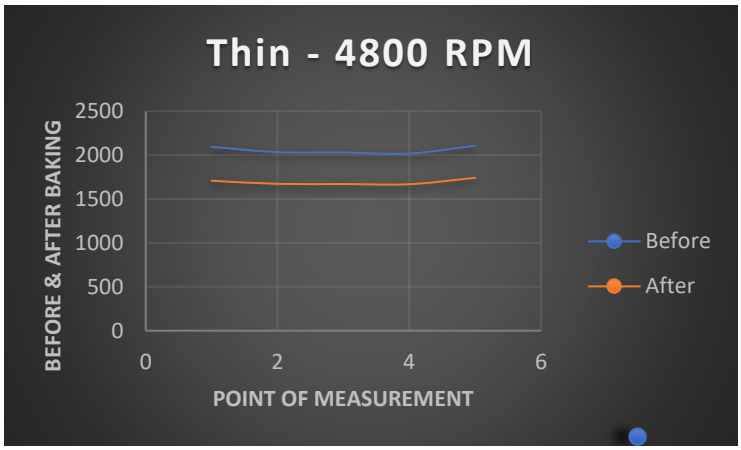

Chart 2 : Thin film before and after baking.

Now that we have seen the thickness change in the photoresist for both the cases before and after baking. The next process is providing a small scratch on the wafer in 5 spots. This scratches are made in order to measure the depth of photoresist of the wafer. This measurement is made with the famous machine **Dektak Profilometer** (destructive method).

Thick Photoresist Measurement :

Table 3 : Thick Dektak measurement of various RPM.

Point of measurement	3800 RPM (um)	2650 RPM (um)	5300 RPM (um)
Point – 1 - Left	6.28288	7.91086	5.51918
Point – 2	6.03722	7.72236	5.06896
Point – 3 - Centre	6.05802	7.89822	5.2354
Point – 4	6.31815	8.80332	5.4687
Point – 5 - Right	7.03511	8.66831	5.72691

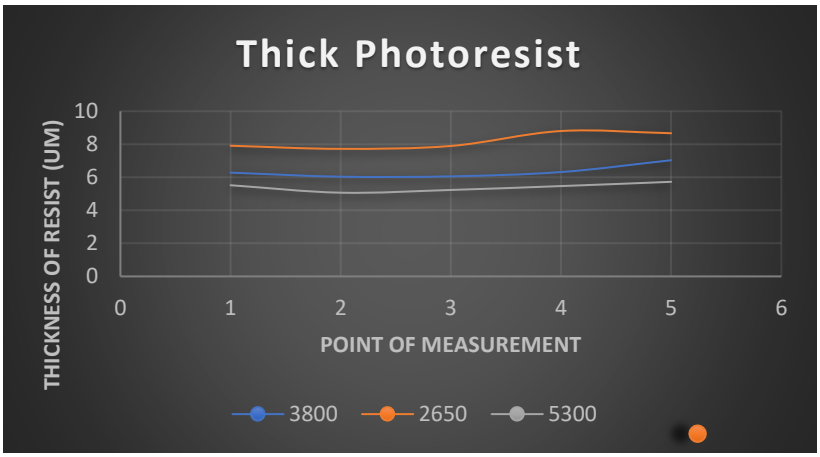

Chart 3 : Thick Resist.

Thin Photoresist Measurement :

Table 4 : Thin Dektak measurement of various RPM.

Point of measurement	2200 RPM (um)	4800 RPM (um)	3600 RPM (um)
Point – 1 - Left	1.45843	1.63238	1.97527
Point – 2	2.41160	1.36770	1.67741
Point – 3 - Centre	2.44743	1.62441	1.5394
Point – 4	2.20621	1.64013	1.87157
Point – 5 - Right	2.52848	1.8738	1.96513

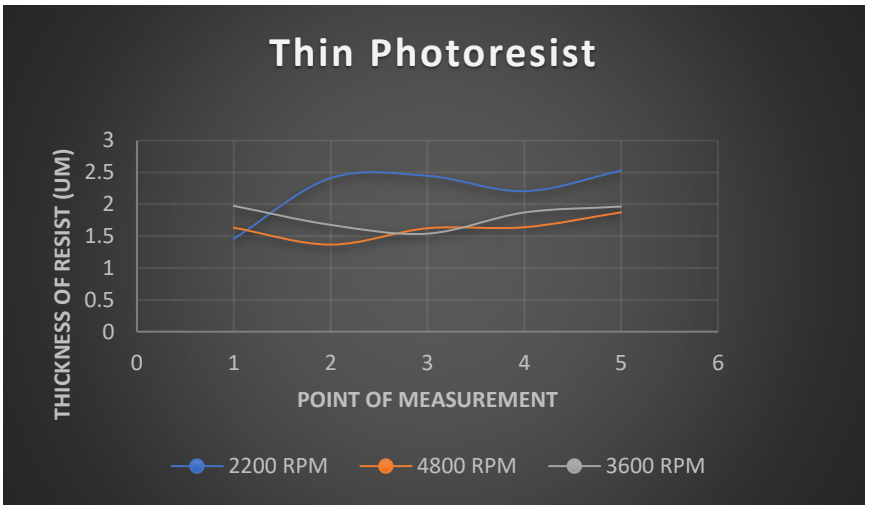

Chart 4 : Thin resist.

Anti – Reflective Coating & Annealing :

Anti – reflective coating plays an important role in improving the efficiency of the solar cell. Anti – reflective coating is typically specified by either the maximum allowable reflectance at a single wavelength or by the average allowable reflectance over a specified wavelength range [9].

One of the main barriers of solar cell efficiency is that it reflects light from its surface. Because bare silicon reflects about 30% of incoming light [9]. The intensity of light transmitted and reflected between two medium is depend upon change in refractive index of mediums and angle of incident of light as interference. The intensity of reflected light is given by Fresnel law :

$$I_R = \frac{(n2-n1)2}{(n2+n1)2}$$

Transparent material with refractive index ***n = 2*** is a best suitable method of anti-reflective coating [9].

The process of Anti – reflective coating is that we create a grooved surface over the surface of the silicon wafer. These grooved surface act as anti-reflective coating by making the sunlight to stay a bit more longer than usual within the substrate for the interactions of atoms. The grooved surface here designed is a pyramid-like structure. When a light falls onto this grooved structure it provides an angle in which the light can hit the surface multiple times before leaving the surface.

Anti – reflective coating does not only provide reduced optical losses but also provide better surface passivation in order to avoid surface recombination [10]. Surface passivation is the measurement of incident rays which goes through the substrate.

As mentioned above a refractive index of *n = 2* is the best choice of the material, in which it is calculated as:

$\eta_{air} = 1$ $\eta_{Si} = 4$

$\eta_C = \sqrt{\eta s * \eta o}$

$\eta_C = 2$

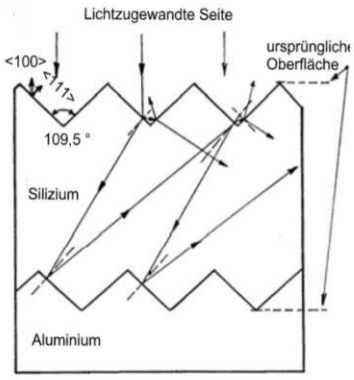

Figure 21 : AR-coating [10].

Oxidation Process :

The next process in the solar wafer is the oxidation process, in which wafer is placed in a furnace where gases are led into the chamber for the oxidation process to take place. This can be done two methods as Dry oxidation and wet oxidation. Dry oxidation is controllable and the formed density of oxide layer is good, whereas for Wet oxidation formation of density oxide layer is poor but it is quicker.

Dry oxidation : O_2 gas : $Si + O_2 \rightarrow SiO_2$

Wet oxidation : H_2O vapour : $Si + H_2O \rightarrow SiO_2 + 2H_2$

The gases O_2 or H_2O are led into the chamber in which the wafer are placed, where the oxygen or water molecules are absorbed and solved into the oxide. The oxygen and water molecule should move through a layer of oxide layer which is already grown on the wafer.

The wafers are placed inside the chamber and the pre conditions are set in the machine to start the oxidation process (the data sheet is displayed in the Appendix). The oxidation is normally given by Deal-grove method :

$$t^2_{OX} + A * t_{OX} = B*(t + \tau)$$

This equation will give the relation between oxide thickness (t_{OX}) and the oxidation time (t).

Photolithography for Aluminium Contacts :

Photolithography process for Aluminium contact is an important step in solar cell manufacturing. Due to its high electrical conductivity Aluminium is plated onto the surface of the wafer. Photolithography process allows transfer a desired structure on the surface of the wafer.

Photolithography consist of three major steps :

- Mask alignment.
- Illumination.
- Development.

Steps involved in Photolithography :

- Wafer is placed on to the photolithography machine (Karl Süss) while facing the flat side of the wafer opposite to the person and vacuum is introduced from the underneath the wafer to prevent misalignment.
- Similarly mask wafer is also placed on top of the machine aligned perfectly with the test wafer.
- Then contact is made by pulling a lever onto the left side of the machine.
- A time of **9 second** is set on the dial for the process to take place.
- After exposure, the wafer is taken out and developed using DI – Wasser (deionized) until the solution rating comes down to **0.09µs** (microsemens).
- Then the wafer is taken out and immediately trenched into the developer for about **60 sec** with constant stirring. The developer used in this process is **AZ351B** which is a NaOH solution.

Photolithography for Aluminium Wires :

The photolithography process for Aluminium wires was also done with the procedures as mentioned above in the photolithography for aluminium contacts.

Firstly the wafer is placed onto the photolithography machine (Karl Süss) and then made contact with the mask that contains the design. A exposure time of **9 seconds** is set on the dial for the process to take place. After exposure the wafer is fed into the DI – Wasser until the readings come down to **0.09µs** and then it is transferred to the developer (AZ351B) for **60 sec** with constant stirring.

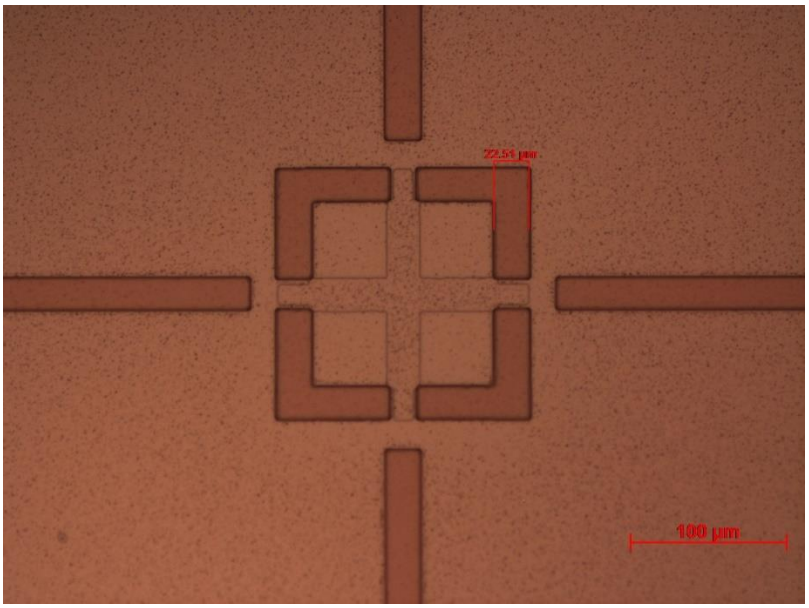

Figure 22 : Aluminium wire.

The above shown picture represent the Aluminium wire from the photolithography process. The only problem with this method of exposure is that we have to look for the perfect point of alignment from the microscope in order to get the expected results.

After exposure and development the wafer is placed underneath a microscope which is attached to a software to measure the width of the aluminium wire created.

Aluminium Etching :

Aluminium etching is the last step in solar cell manufacturing process. In this lab we did use wet etching to etch away the aluminium formed on the top surface of the solar cell, because simple wet etching will provide **high etch rate** and **high selectivity**.

Etching consist of two major steps :

- Preparing etchants and etching the wafer.
- Developing the wafer.

First step is to create a proper etchants which will be useful for the process to take place. We use 2.5% of HNO_3 (nitric acid) for Al – oxidation and 75% of H_3PO_4 (phosphoric acid) to dissolve Al_2O_3 and 5 – 10 % of CH_3COOH (acetic acid) for wet etching and buffering. All these kept in a bath to encounter the wafer. The wafer is first dipped in DI – Wasser for 30 seconds because the process is highly exothermic and releases H_2 bubbles which will in turn reduce the homogeneity. Then the wafer is dipped into the solution of HNO_3 + H_3PO_4 for about 45ºC until all the aluminium is etched away. It took us exactly **3 min 51 sec** for the etching process to get over. Then the wafer is taken out and developed in the DI – Wasser until the conductivity reduces to 0.09µs. Then the wafer is taken out and nitrogen gas is introduced to remove the water molecules from the wafer and kept under the microscope to observe the wafer. This step will be the last in manufacturing the solar cell.

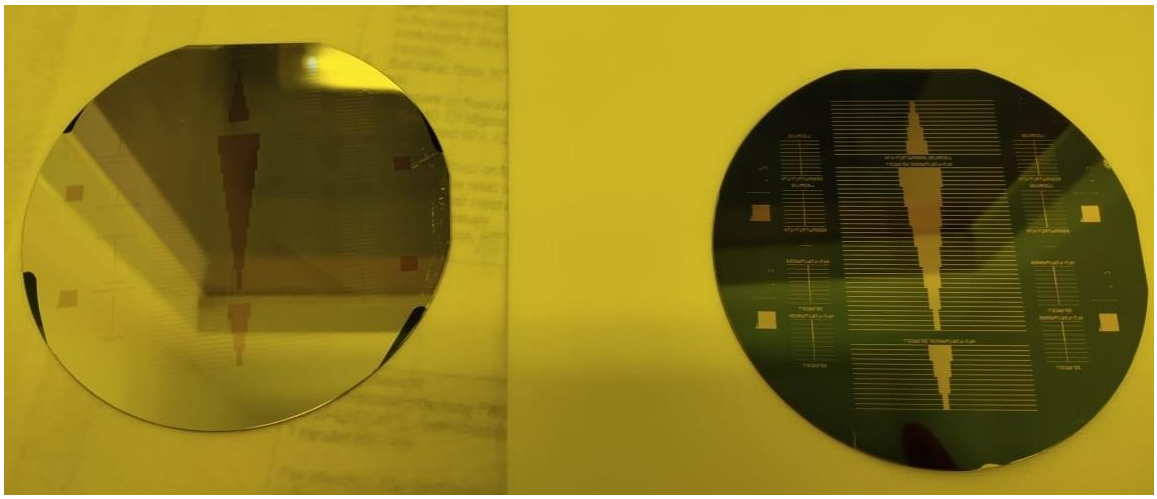

Figure 23 : Before and after etching.

Electrical Characterization of Solar Cells :

This section deals with performing electrical measurement for the solar cell which we have created. The solar cell is placed directly under a lamp and then a multi-meter is connected to the series of resistance and to the wafer. The lamp illumination was about 1000 W/m^2 which is equal to 0.1 W/cm^2. The incident power is 1.6W.

In this voltage and current is measured in three different places as 40mm * 40mm ; 40mm * 15mm and 10mm * 10mm. These values are noted down and a respective charts are made to show the range of possibilities. These voltages and currents are used to calculate the power and efficiency of the solar cell and the formula for power and efficiency goes like :

$$P = V * I$$

$$\text{Efficiency} = (P_{out} / P_{in}) * 100$$

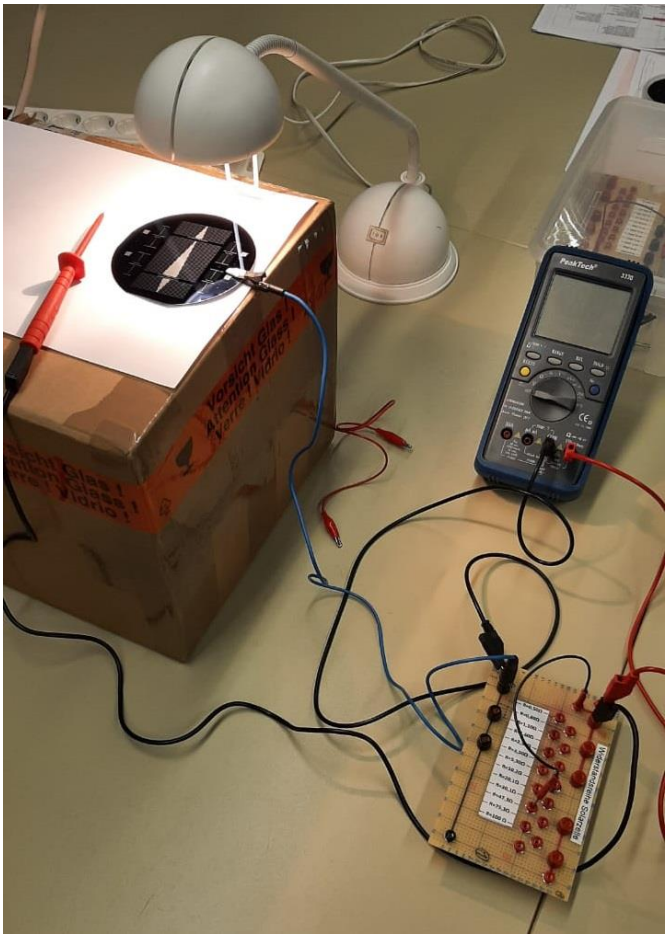

Figure 24 : Electrical Characterization.

Results :

This section will be comprised of the results of electrical characterization which is discussed in the above section. All the values are observed and appropriate graphs are provided.

Error calculation :

In this section we have measured the current and voltage value for three wafers namely wafer 2, wafer 3 and wafer 6 respectively. Mean value is calculated by adding all the voltage and divided by number of calculations, which is the same procedure for the current. Error is calculated by standard deviation of the voltage/current divided by the number of calculations.

Wafer...2	Area	I sc [mA]	V oc [mV]
	4 * 4	-104	433
	1,5 * 4	-101	436
	1 * 1	-73.5	440

Figure 25 : V & I for wafer 2.

Wafer ...3	Area	I sc [mA]	V oc [mV]
	4 * 4	-171.3	433
	1,5 * 4	-157	426
	1 * 1	-86.3	479

Figure 26 : V & I for wafer 3.

Wafer ...6	Area	I sc [mA]	V oc [mV]
	4 * 4	-176.2	409
	1,5 * 4	-157.7	413
	1 * 1	-88.8	412

Figure 27 : V & I for wafer 6.

	Area	I sc [mA]	V oc [mV]
Mean Value	4 * 4	-451.5	1275
	1,5 * 4	-415.7	1275
	1 * 1	-248.6	1331

Figure 28 : Mean values.

Wafer ...	Area	I sc [mA] Error %	V oc [mV] Error %
	4 * 4	23.29298893	8
	1,5 * 4	18.78442026	6.658328118
	1 * 1	4.73861208	19.42792949

Figure 29 : Error values.

Efficiency Calculation :

In this section efficiency and the respective graphs are displayed. The efficiency is calculated by the formula:

$$\text{Efficiency} = (P_{out} / P_{in})*100$$

For 4 * 4 wafer :

Size 4 * 4 cm2	Pin = 1.6 W			
R [Ohm]	**V [mV]**	**I [mA]**	**Pout [uW]**	**Eff. [%]**
0.5	128.6	257.2	33075.92	2.067245
0.8	171.6	214.5	36808.2	2.3005125
1.1	246.6	224.1818182	55283.23636	3.455202273
1.6	286	178.75	51122.5	3.19515625
2.3	308.8	134.2608696	41459.75652	2.591234783
3.5	342.3	97.8	33476.94	2.09230875
5.3	362.3	68.35849057	24766.28113	1.547892571
10.2	380	37.25490196	14156.86275	0.884803922
20.1	390.6	19.43283582	7590.465672	0.474404104
30.1	393	13.05647841	5131.196013	0.320699751
47.3	395	8.350951374	3298.625793	0.206164112
75.3	397	5.272244356	2093.081009	0.130817563
100	398	3.98	1584.04	0.0990025

*Figure 30 : Efficiency for 4*4 wafer.*

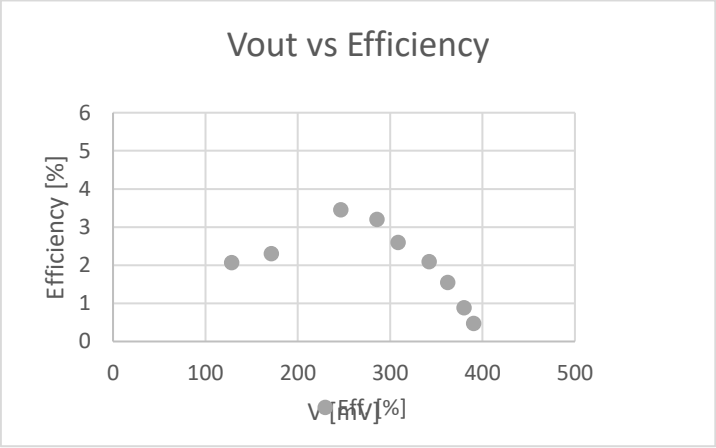

*Figure 31 : V_{out} vs Efficiency for 4*4.*

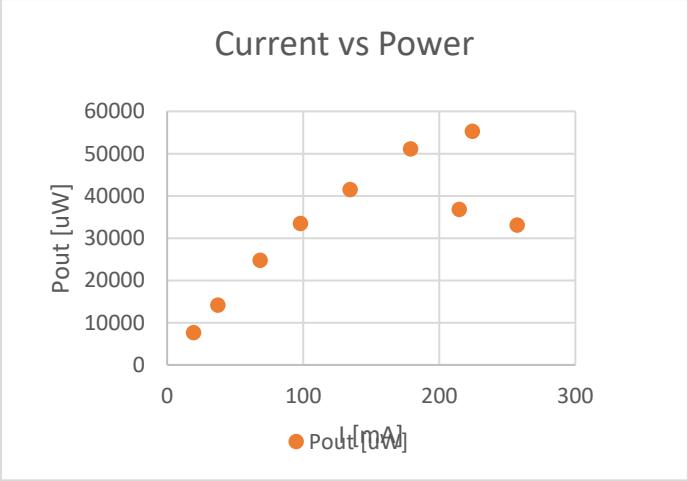

*Figure 32 : I vs P for 4*4.*

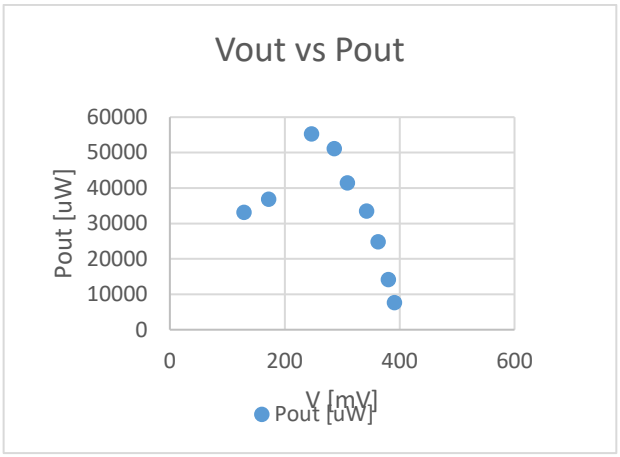

*Figure 33 : V_{out} vs P_{out} for 4*4.*

For 1.5 * 4 wafer :

Size 1.5 * 4 cm2	Pin = 0.6 W			
R [Ohm]	**V [mV]**	**I [mA]**	**Pout [uW]**	**Eff. [%]**
0.5	94.8	189.6	17974.08	2.99568
0.8	130.8	163.5	21385.8	3.5643
1.1	206.7	187.9090909	38840.80909	6.473468182
1.6	255	159.375	40640.625	6.7734375
2.3	286.5	124.5652174	35687.93478	5.94798913
3.5	330.6	94.45714286	31227.53143	5.204588571
5.3	357.7	67.49056604	24141.37547	4.023562579
10.2	384	37.64705882	14456.47059	2.409411765
20.1	398	19.80099502	7880.79602	1.313466003
30.1	404	13.42192691	5422.458472	0.903743079
47.3	408	8.625792812	3519.323467	0.586553911
75.3	411	5.458167331	2243.306773	0.373884462
100	412	4.12	1697.44	0.282906667

*Figure 34 : Efficiency for 1.5*4 wafer.*

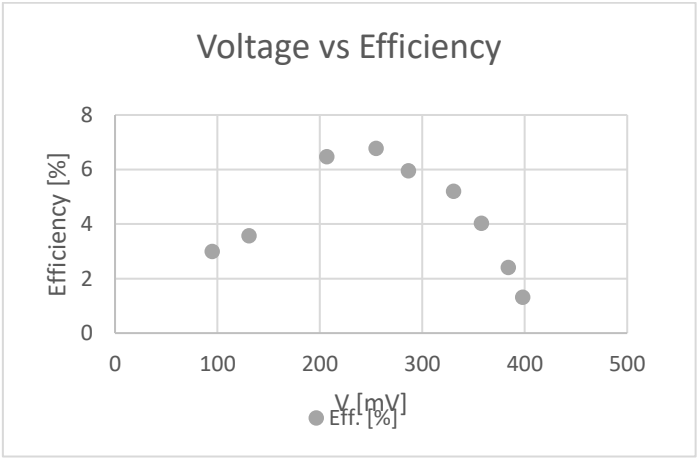

*Figure 35 : V_{out} vs Efficiency for 1.5*4.*

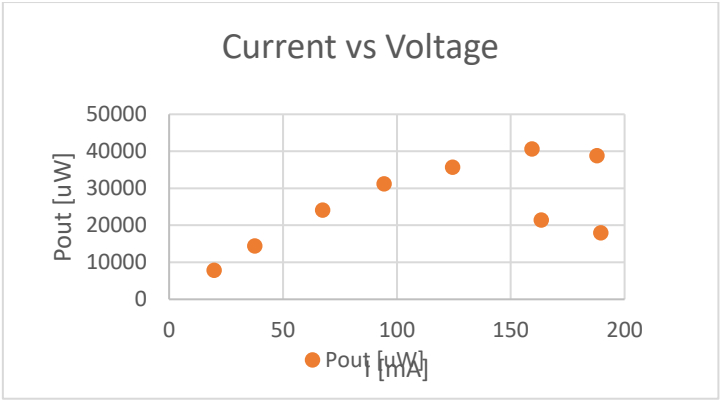

*Figure 36 : I vs V for 1.5*4.*

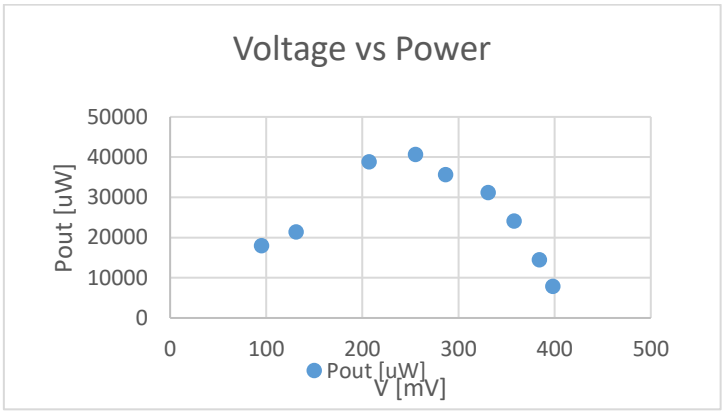

*Figure 37 : V vs P for 1.5*4.*

For 1 * 1 wafer :

Size 1* 1 cm2	Pin = 0.1 W			
R [Ohm]	**V [mV]**	**I [mA]**	**Pout [uW]**	**Eff. [%]**
0.5	40.8	81.6	3329.28	3.32928
0.8	59.3	74.125	4395.6125	4.3956125
1.1	105.3	95.72727273	10080.08182	10.08008182
1.6	142.9	89.3125	12762.75625	12.76275625
2.3	174.2	75.73913043	13193.75652	13.19375652
3.5	231.8	66.22857143	15351.78286	15.35178286
5.3	278.9	52.62264151	14676.45472	14.67645472
10.2	318.8	31.25490196	9964.062745	9.964062745
20.1	361	17.960199	6483.631841	6.483631841
30.1	378	12.55813953	4746.976744	4.746976744
47.3	390	8.245243129	3215.64482	3.21564482
75.3	399	5.298804781	2114.223108	2.114223108
100	404	4.04	1632.16	1.63216

*Figure 38 : Efficiency for 1*1 wafer.*

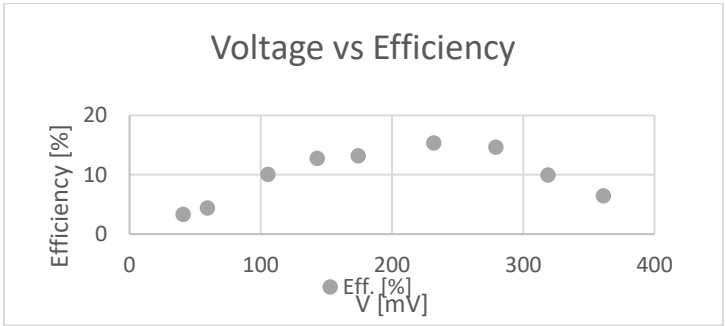

*Figure 39 : V vs efficiency for 1*1.*

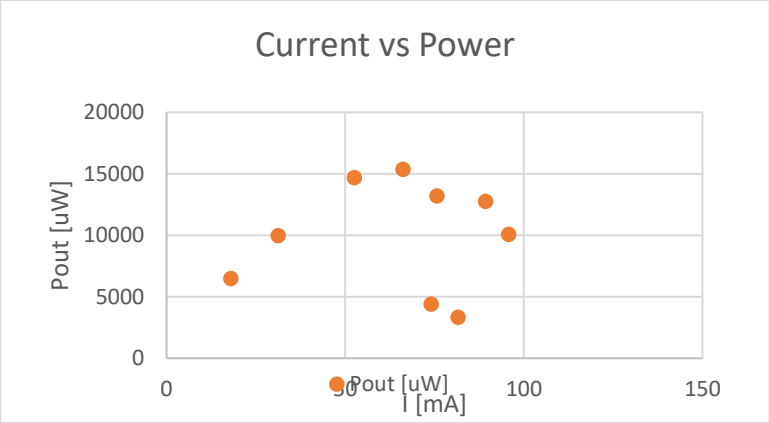

*Figure 40 : I vs P for 1*1.*

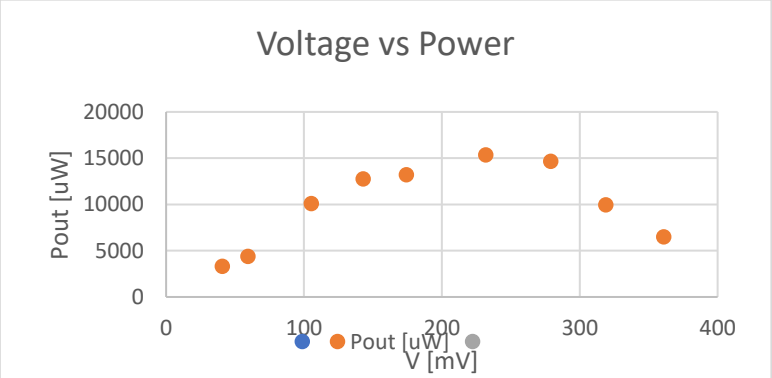

*Figure 41 : V vs P for 1*1.*

Conclusion :

From the above shown images clearly depicts that the maximum efficiency is about 19.4% which is comparatively higher when compared to the real time simulation. This is because the calculations are made under constant light condition with constant illumination and also the efficiency depends on the size of wafers which are typically used.

This report gives an detailed understanding of photovoltaic cell, their manufacturing process and electrical components. Every step involved in manufacturing process has been depicted clearly and also the results of simulation are also mentioned. The Appendix contains some additional information regarding the manufacturing of solar cell.

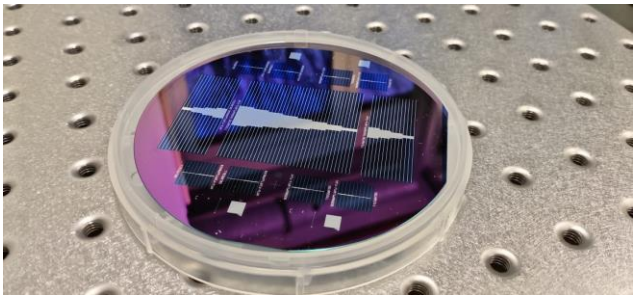

Figure 42 : Completed solar cell.

Appendix

Appendix A :

This Appendix will be displaying the overall view of the process flow which was discussed above in the report.

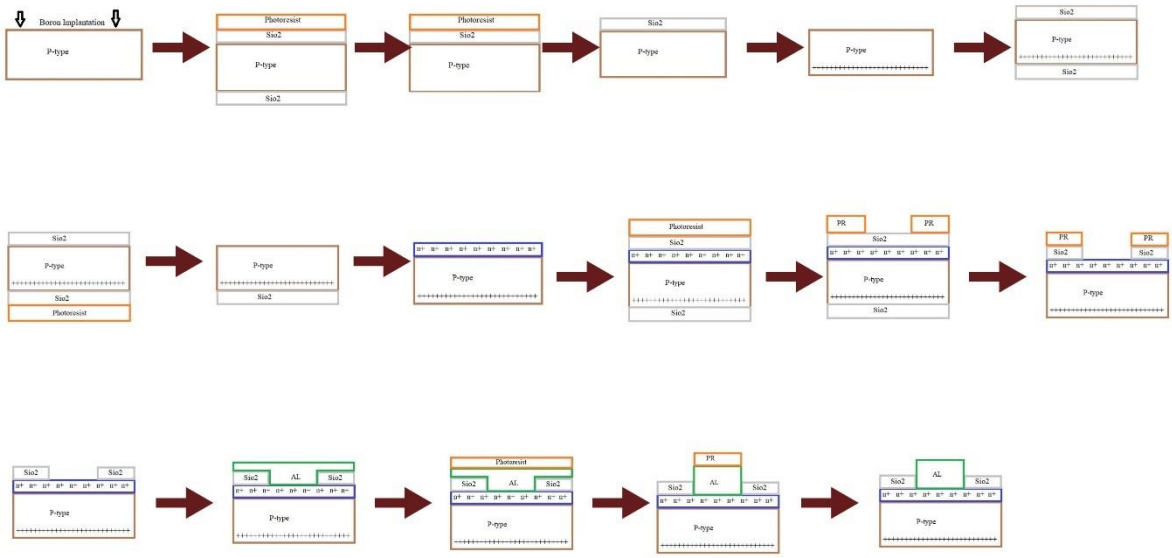

Figure 43 : Overall Process flow.

Appendix B :

This will be showing the mask design which I created using the CleWin5 software.

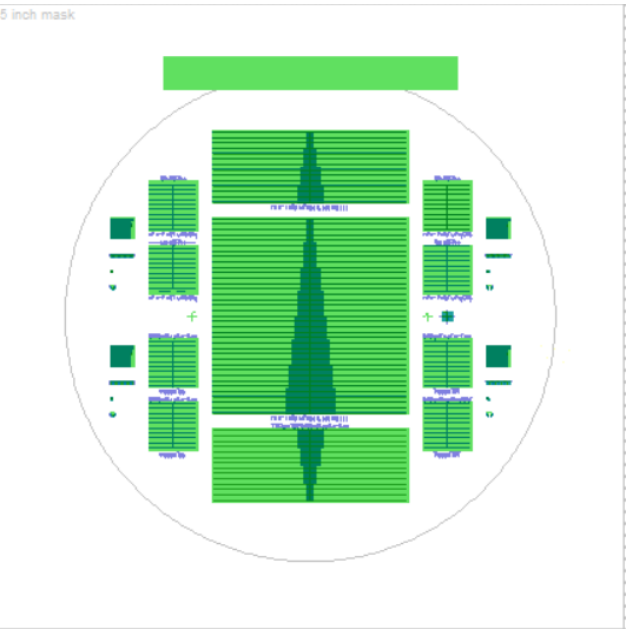

Figure 44 : Mask design.

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