LWL and LWR

Imagine we are trying to read a word from the address 0x1fc00002. Because the MIPS instruction set enforces alignment of memory access, this is not possible with the `lw` instruction. To provide the ability to make unaligned reads while still enforcing alignment, the MIPS ISA provides the instructions `lwl` (Load Word Left) and `lwr` (Load Word Right). Their use is as follows:

Load word left takes an unaligned address, and loads from memory the values starting at the effective address up to the next word boundary, placing these values in the most significant (left) portion of the destination register (leaving the other values in the register unchanged). For example, a read using load word left from the address 0xbfc00001 will read the bytes at 0xbfc00001, 0xbfc00002 and 0xbfc00003, placing them in the most significant portion of the destination register, leaving the remaining parts of the register unchanged.

Load word right takes an unaligned address, and loads from memory starting at the word aligned address immediately prior to the effective address (i.e. if the effective address is 0x1fc00001, it starts reading from 0x1fc00000) and reads values up to the effective address, placing the read values in the least significant (right) portion of the destination register (leaving the other values in the register unchanged). For example, a read using load word right from the address 0xbfc00001 would read the bytes at 0xbfc00000 and 0xbfc00001 and would place them in the least significant portion of the destination register, leaving the rest of the register unchanged.

1 Examples

Note: The destination register starts with the value 0x87654321 at the start of each example

Assume that memory initially contains the values:

Address	Value
0x1fc00000	0x90abcdef
0x1fc00004	0x12345678

Table 1: Initial Memory Values

1.1 Load Word Left

Effective Address	Result Value in Register
0x1fc00000	0x**90abcdef**
0x1fc00001	0x**abcdef**21
0x1fc00002	0x**cdef**4321
0x1fc00003	0x**ef**654321
0x1fc00004	0x**12345678**
0x1fc00005	0x**34567821**
0x1fc00006	0x**5678**4321
0x1fc00007	0x**78**654321

Table 2: Results of Load Word Left (Bold is value written)

1.2 Load Word Right

Effective Address	Result Value in Register
0x1fc00000	0x87654**390**
0x1fc00001	0x8765**90ab**
0x1fc00002	0x87**90abcd**
0x1fc00003	0x**90abcdef**
0x1fc00004	0x87654**312**
0x1fc00005	0x8765**1234**
0x1fc00006	0x87**123456**
0x1fc00007	0x**12345678**

Table 3: Results of Load Word Right (Bold is value written)

In the MIPS instruction reference provided with the project, Figures 3-5, 3-6, 3-7, and 3-8 provide visual examples of Load Word Left and Load Word Right.