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RC – Report

Introduction

For acceleration purposes and for avoiding dependencies, the geo_dist function was chosen to be synthesized. By translating the geo_dist (new) function, the parallelism of the hardware platform ensures a better performance.

This function was tested against 10 million inputs, and the following times were obtained:

```
xilinx@pynq:~/RoutingKit$ ./test_geo_dist
running time of old geo distance for 10000000 tests : 45157694 musec
running time of new geo distance for 10000000 tests : 31343527 musec
```

This means that a single calculation takes 3 us.

Vivado HLS

The cpp function was taken and translated into HDL language using Vivado HLS. The following report was obtained after synthetization:

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	8.00 ns	8.843 ns	1.00 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
109	361	0.964 us	3.192 us	109	361	none

Detail

Instance

		Latency (cycles)		Latency (absolute)		Interval (cycles)		
Instance	Module	min	max	min	max	min	max	Type
grp_generic_asin_20_8_s_fu_103	generic_asin_20_8_s	1	253	8.843 ns	2.237 us	1	253	none
grp_generic_sincos_fu_110	generic_sincos	97	97	0.858 us	0.858 us	97	97	none
grp_generic_sincos_fu_117	generic_sincos	97	97	0.858 us	0.858 us	97	97	none
grp_generic_sincos_fu_124	generic_sincos	97	97	0.858 us	0.858 us	97	97	none

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Utilization Estimates

Summary

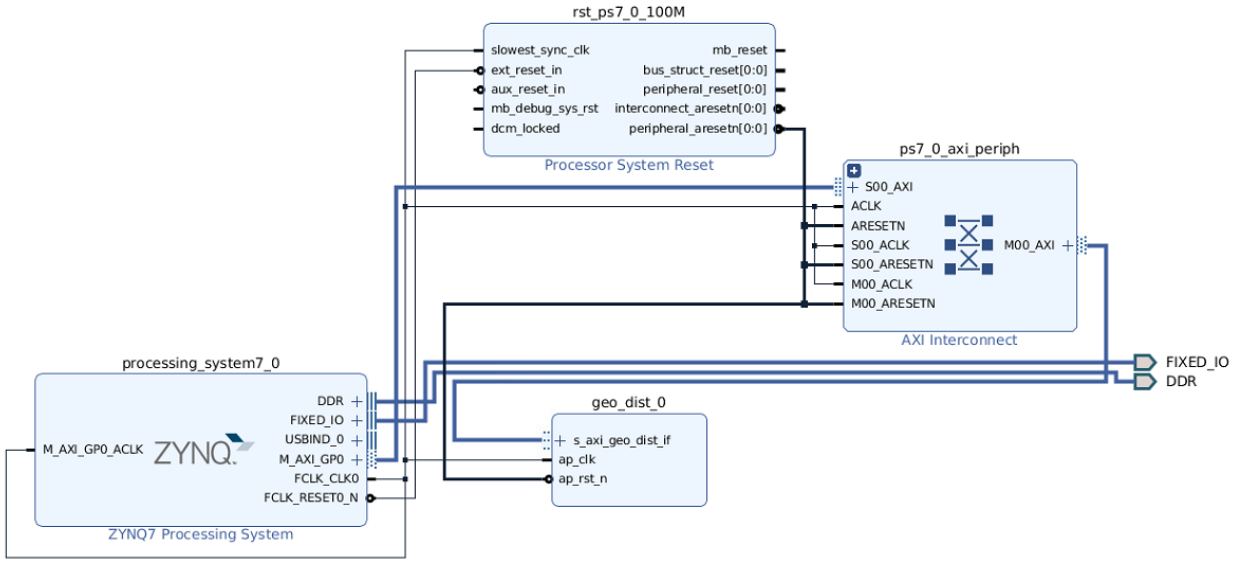
Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	5	-	-	-
Expression	-	-	0	95	-
FIFO	-	-	-	-	-
Instance	20	10	15990	17670	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	71	-
Register	-	-	423	-	-
Total	20	15	16413	17836	0
Available	280	220	106400	53200	0
Utilization (%)	7	6	15	33	0

The implementation was check with a testbench, from which we got the following results for random inputs:

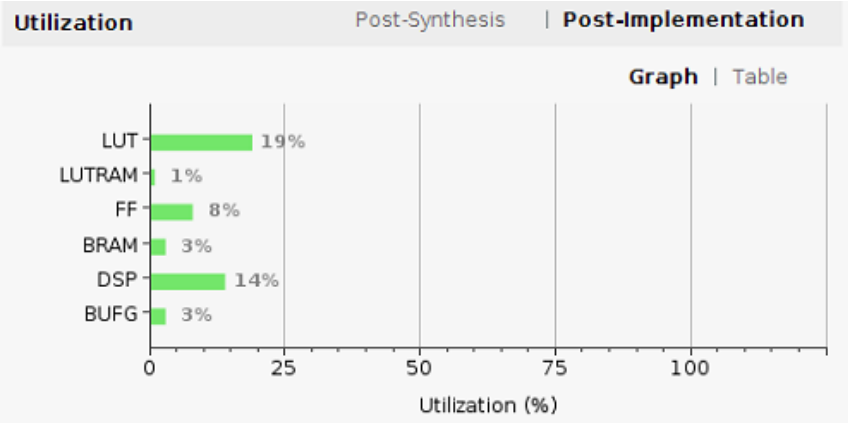
```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../src/tb.cpp in debug mode
   Generating csim.exe
The expected and actual results match! (57.6199)
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Vivado

After synthesizing the IP, the geo_dist function was linked to the Zynq Processing system as shown below:



The following reports were obtained:



Timing	Setup
Worst Negative Slack (WNS):	0.524 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	13777
Implemented Timing Report	

From Vivado the bitstream was generated and translated (along with the hardware description file) to the Pynq-Z2 board.

Jupyter

We tested the IP using the Jupyter interface as follows:

```
from pynq import Overlay
from datetime import datetime

import struct

overlay = Overlay('/home/xilinx/pynq/overlays/project_aces/design_1.bit')
geo_dist_ip = overlay.geo_dist_0

lat_a_addr = 0x10
lon_a_addr = 0x18
lat_b_addr = 0x20
lon_b_addr = 0x28

result_addr = 0x30

geo_dist_ip.write(lat_a_addr, 30)
geo_dist_ip.write(lon_a_addr, 30)
geo_dist_ip.write(lat_b_addr, 32)
geo_dist_ip.write(lon_b_addr, 32)

result = struct.unpack('f', struct.pack('I', geo_dist_ip.read(result_addr)))[0]

print(result)
```

```
1.4564942095361073e-39
```

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Conclusions

After translating the geo_dist function into the FPGA logic, the best latency is 0.96 us, which represents an acceleration of ~3x compared to the software version. For the worst-case scenario, the latency is 3.19 us, almost the same as the software one.

The results are better for the synthesized version, as seen in the reports.