Instrumentation Final Report

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1 Introduction

The circuit utilises an auto-balancing bridge (ABB) to measure the voltage across the Device Under Test (DUT), enabling precise impedance characterisation. A branched current sensor detects the current flowing through the DUT, while the voltage across it is determined using the following equation:

$$V_{DUT} = \frac{V_{OUT}}{I_{DUT}} \times (V_{OUT} - V_{IN}) \tag{1}$$

The current measurement is performed using an operational amplifier (op-amp) in conjunction with a transistor, which effectively measures the current flowing through the shunt resistor. To maintain measurement accuracy across varying DUT impedances, a relay is employed to dynamically select the appropriate feedback resistor, ensuring that the resistor value remains within an optimal range.

The acquired signals are digitised using an Analog-to-Digital Converter (ADC) and subsequently processed by the STM32 Nucleo F446RE microcontroller, which features an ARM Cortex-M4 processor with floating-point and DSP instructions. The ADC samples the voltage and current signals at a high resolution, typically at 12-bit (using an external ADC if necessary). The STM32's DMA (Direct Memory Access) controller is utilised to handle real-time data acquisition without excessive CPU overhead.

To extract impedance parameters, the system computes the in-phase (I_{real}) and quadrature (I_{imag}) components of the signal using Goertzel's algorithm, leveraging the CMSIS-DSP library for optimised real-time processing. The impedance of the DUT is then determined using:

$$Z_{DUT} = \frac{V_{DUT}}{I_{DUT}} \tag{2}$$

where V_{DUT} and I_{DUT} are obtained through precise synchronous detection. The phase angle θ is computed as:

$$\theta = \tan^{-1}\left(\frac{I_{\text{imag}}}{I_{\text{real}}}\right) \tag{3}$$

Additionally, the system compensates for parasitic impedances using calibration techniques, storing correction factors in flash memory. The STM32's timers and PWM outputs are used to generate the test signal, ensuring stability and minimising harmonic distortion.

The primary objective of this system is to achieve real-time, high-accuracy impedance measurement for applications. By leveraging the STM32 Nucleo F446RE's computational power and peripheral capabilities, the system ensures robust performance, minimal latency, and high precision.

2 Photograph of Prototype

Figure 1 shows the prototype of the impedance measurement system, which consists of the STM32 Nucleo F446RE microcontroller mounted on a custom-designed printed circuit board (PCB) by female header pins. The PCB includes key analogue front-end components such as an operational amplifier (op-amp), a relay-controlled resistor network, and a shunt resistor, enabling precise impedance measurements. The DUT is connected via a green terminal block, while the power and communication interface is provided through the USB connection to the STM32 board.

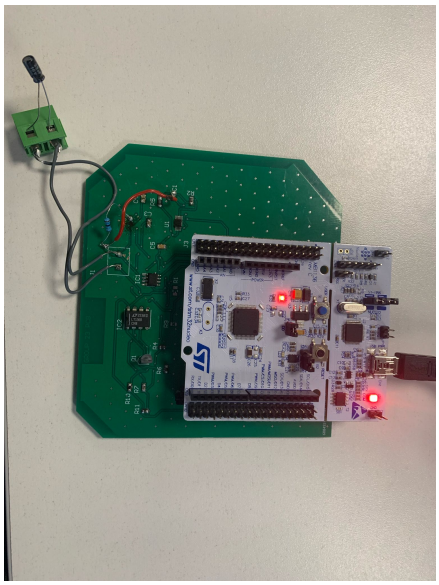


Figure 1: Photograph of the prototype

3 Schematic Diagram

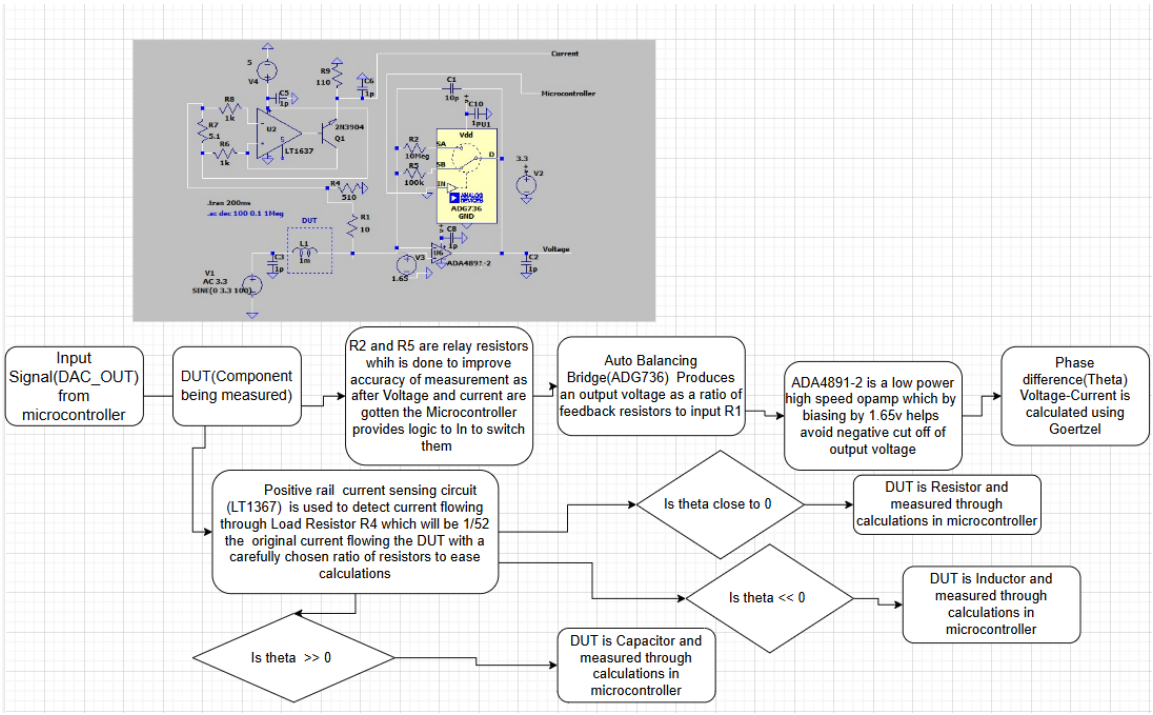


Figure 2: Flow chart of schematic

The DUT (device under test) connects between an AC source (high side) and the op-amp's summing node (low side). In this configuration, U6 acts as the auto-balancing bridge op-amp. It forces the summing node to the virtual ground (0 V) by feeding current through a reference resistor in its feedback path, ensuring the bridge remains balanced. Transistor Q1 provides additional drive capability, allowing U6 to source or sink the DUT's current without saturating the op-amp. The ADG736 dual SPDT analogue switch, acting as an electronic relay, selects different feedback resistors or network configurations for auto-ranging and maintaining balance across varying DUT impedances.

In this setup, U2 functions as the transimpedance amplifier. The DUT's low terminal is held at the virtual ground through U2's negative feedback. The AC source drives the high side of the DUT, and all current flowing through the DUT is routed into U2's inverting input node. U2 then drives its output to inject an equal-magnitude, opposite-phase current through the known reference resistor (feedback resistor) back into the summing node. This feedback mechanism keeps the summing node at approximately 0V (balance), akin to a null in a bridge measurement. Essentially, the current through the DUT is mirrored (but inverted) by the current through the feedback resistor. By measuring the voltage across the feedback resistor, the instrument infers the DUT's current.

The current-sensing path is the feedback network of U2, which converts the DUT current into a voltage, $V = I \times R_f$, at its output, representing the current magnitude and phase. The voltage-sensing path is the direct measurement of the AC source across the DUT (often via a high-impedance buffer or separate sense lead, though in simulation it can be taken as the source voltage itself). This separation of voltage (DUT voltage) and current (feedback voltage) measurements is key to accurate impedance characterization.

Because the op-amp must handle a wide range of currents and voltages, additional components support its operation. Transistor Q1 is used as a booster/output stage to assist U2 in driving the DUT and the feedback network. In scenarios where the DUT demands high current (for example, a low-resistance or low-frequency inductive load), Q1 sources or sinks the majority of that current so that U2's output can remain within its linear range. In essence, Q1 ensures the op-amp can maintain the virtual ground without output voltage clipping or excessive loading, by providing extra muscle for the current drive.

The ADG736 is a dual SPDT analog switch IC that functions as a pair of electronically controlled relays in the feedback and sensing network. This allows the circuit to reconfigure or switch in different reference resistors and calibration loops. For example, when measuring a small impedance (which permits a large current), the ADG736 can switch to a small feedback resistor to avoid saturating U2. Conversely, for a large impedance or tiny currents, it can switch in a larger feedback resistor to produce a readable voltage.

In summary, U6, Q1, and the ADG736 work together to maintain an auto-balanced bridge: U2 nulls the DUT node voltage by adjusting its output current, Q1 extends the output current/voltage range, and the ADG736 selects the proper feedback settings for the DUT's range. This results in a system where the ratio of U6's output voltage to the source voltage is set by the ratio of the feedback impedance to the DUT's impedance (with a negative sign for the inversion). You can think of it like a frequency-dependent voltage divider between the DUT and the feedback resistor, actively driven to equilibrium. The following sections analyse the frequency response for each type of DUT (Resistor, Capacitor, Inductor) in terms of this ratio and the impedance characteristics Z_{DUT} (with $Z_R = R$, $Z_L = j\omega L$, $Z_C = \frac{1}{j\omega C}$).

4 List of Input and Output Signals of the Instrument

ADC Pins:

- **Voltage Signals:**
  - The ADC measures the voltage across the Device Under Test (DUT). Specifically, the voltage across the DUT is derived from the output voltage (V_{OUT}) and the input voltage (V_{IN}) of the auto-balancing bridge in [1].
  - The equation gives the relationship between these voltages:

$$V_{DUT} = \frac{V_{OUT}}{I_{DUT}} \times (V_{OUT} - V_{IN})$$

  - In the circuit, the DUT is connected to the auto-balancing bridge, and the voltage across the DUT is captured by the ADC for further processing. The ADC measures this voltage, which will then be used to calculate the impedance and other parasitic components.
- **Current Signals:**
  - The current flowing through the DUT is measured by the ADC. This is achieved by measuring the voltage drop across a shunt resistor connected in series with the DUT as can be seen in [2].
  - The voltage across the shunt resistor is proportional to the current flowing through it, and this measurement is amplified using an operational amplifier (op-amp) in combination with a transistor.
  - The current is then calculated using Ohm's law ($I = \frac{V_{shunt}}{R_{shunt}}$), where V_{shunt} is the voltage across the shunt resistor and R_{shunt} is its known value.
  - The ADC captures this current measurement, which will be used to calculate impedance, phase shift, and other parasitic elements of the DUT.

DAC:

- **3.3V Sine Wave Generation:**
  - The DAC generates a sine wave at a configurable frequency, a range of 100Hz to 100kHz, which is used as the stimulus signal for the DUT.
  - The DAC outputs a 3.3V peak-to-peak sine wave, which is applied to the input of the auto-balancing bridge.
  - The sine wave generated by the DAC is essential for stimulating the DUT in the bridge, allowing the system to measure how the DUT responds to the input signal regarding voltage and current.
  - Efficient sinewave generation is essential for accurate measurements. To achieve this, a look-up table (LUT) can be employed, storing 1/8 of a sinewave, which can then be computed and repeated to complete the full period of the sinewave. This method allows for efficient memory usage and faster computation, as only a fraction of the sinewave needs to be stored, and the full sinewave can be reconstructed using the appropriate computation over successive periods.

GPIO Pin:

- **Relay Select Pin:**
  - The GPIO pin controls the relay, which is used to switch between different feedback resistors in the auto-balancing bridge circuit.
  - The relay can either connect a high resistance or a low resistance in the feedback loop depending on the measured impedance of the DUT.
  - If the impedance is high, the relay connects the higher feedback resistor to maintain optimal measurement conditions. If the impedance is low, the relay switches to a lower feedback resistor to improve the system's measurement range.
  - This relay switching is done dynamically to ensure that the auto-balancing bridge maintains an optimal gain for the DUT being tested.

Operations:

- **ADC Sampling:**
  - The ADC continuously samples both the voltage and current signals from the DUT. These ADC samples represent the real-time behaviour of the DUT under test conditions.
  - The voltage signal is taken across the DUT, and the current signal is derived from the shunt resistor. These signals are essential for computing impedance and parasitic elements.

- The ADC samples these signals at a defined frequency and stores them for processing, particularly for frequency analysis using the Goertzel algorithm.

- **Goertzel Algorithm:**
  - The Goertzel algorithm is a recursive algorithm used to extract specific frequency components from the ADC samples. It is particularly useful for extracting the amplitude and phase of a single frequency component.
  - In the circuit, the Goertzel algorithm takes the voltage and current samples and computes the real (in-phase) and imaginary (quadrature) components of the signal.
  - These components allow the system to determine the impedance and phase shift of the DUT. The real and imaginary components are essential for calculating the resistance, reactance, and other parasitic components of the DUT.

- **Relay Control:**
  - The relay is controlled through a GPIO pin to select the appropriate feedback resistor. Depending on the impedance calculated from the measured signals, the relay switches to either a high or low resistance configuration.
  - If the impedance of the DUT is high, the relay will connect a high resistance to the bridge, and if the impedance is low, the relay will switch to a lower resistance, ensuring that the system adapts to varying DUT impedances.

- **Impedance Calculation:**
  - The impedance of the DUT is calculated by measuring the phase shift between the voltage and current components using the Goertzel algorithm. This phase shift is indicative of the nature of the DUT (resistive, inductive, or capacitive).
  - The impedance formula used in the system is derived from the voltage and current components as follows:

$$Z = \sqrt{R_s^2 + X_s^2}$$

    where R_s is the series resistance and X_s is the series reactance.
  - The system also computes the parasitic components, such as inductance (L_s) and capacitance (C_s), based on the calculated impedance and frequency of operation.

- **UART Output:**
  - The results of the impedance measurement, including the DUT's resistance (R_s), reactance (X_s), and any parasitic components (such as inductance and capacitance), are transmitted via UART to a terminal or display for further analysis.
  - The UART interface allows the user to monitor the real-time measurements of the DUT's impedance and other parameters directly on a computer or display terminal.

From the code, the following key signals are involved:

- **Relay Control Pin:** This pin controls the relay switching, allowing the adjustment of the feedback resistor based on the computed impedance of the DUT.
- **ADC Inputs (Voltage and Current):** These ADC inputs measure the voltage and current through the DUT, providing the necessary data for calculating the impedance and parasitic components of the DUT.
- **DAC Output:** The DAC generates the sine wave stimulus for testing, ensuring that the DUT is subjected to a known input signal.
- **UART Output:** The processed impedance and parasitic values are transmitted via UART to a terminal or display for real-time monitoring and analysis.

5 Specification achieved and Simulations

The only specification that was achieved was finding the phase of the signals through LT spice, which we confirmed by applying a sinewave from the wave generator in the oscilloscope.

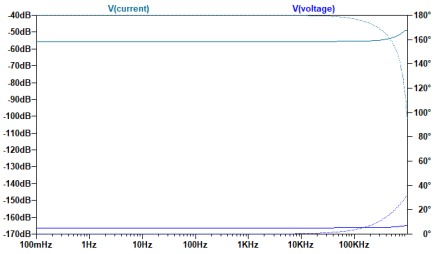


Figure 3: Frequency Sweep of Resistor as DUT

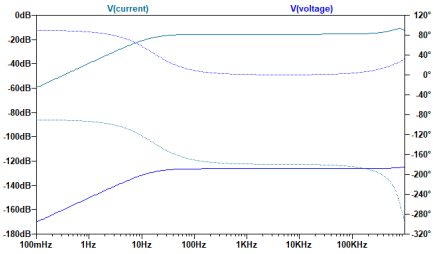


Figure 4: Frequency Sweep of Capacitor as DUT

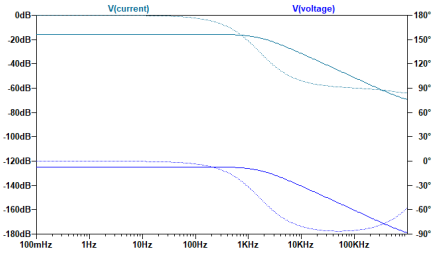


Figure 5: Frequency Sweep of Inductor as DUT

Resistor as DUT

Simulated Frequency Response: The LTspice AC sweep for a resistive DUT indeed shows a flat magnitude response (in dB) across the frequency range, matching the expectation of constant impedance. In the plotted result, the magnitude trace is horizontal (0 dB slope), indicating the gain from input to U2's output does not change with frequency. The exact level of this gain in dB is determined by the ratio of the feedback resistor to the DUT resistance (i.e. $20 \cdot \log_{10}\left(\frac{|V_{\text{out}}}{V_{\text{in}}}\right) = 20 \cdot \log_{10}\left(\frac{R_f}{R}\right)$). If R_f was equal to the DUT's R, the magnitude would be 0 dB; different values shift the magnitude up or down, but it remains frequency-independent (a purely resistive divider ratio). The phase plot for the resistor case is approximately -180° in the simulation. This -180° phase shift is not because the resistor itself is reactive (it's not), but because the trans-impedance amplifier inverts the signal. U2 outputs a voltage that is equal in magnitude to the voltage across the resistor (scaled by $\frac{R_f}{R}$), but opposite in phase, to balance the node.

Circuit Behaviour Explanation: With a resistor, the op amp U2 operates as a stable inverting amplifier with a gain of $-\frac{R_f}{R}$ (constant over frequency). The voltage division between the DUT and the feedback resistor is simple: since both are frequency independent, the ratio $\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{R}$. The "bridge" is balanced when U2's output exactly cancels the current through R, so this ratio holds at all frequencies. The flat magnitude in the Bode plot directly corresponds to this constant ratio. The phase of -180° is the hallmark of an inverting amplifier – U2 must output a voltage opposite in phase to the input to drive the summing node to 0 V. Op amp U2 thus ensures the resistor's current (which is proportional to $\frac{V_{\text{in}}}{R}$) is exactly mirrored by an opposite current through R_f, and it outputs the necessary opposite voltage. Transistor Q1 has little effect on ideal AC behaviour for a resistor; it primarily guarantees that if the resistor draws a large current (for example, if R is small and the source voltage is significant), the op-amp can supply it without saturating. Q1 extends the current driving capability but does not introduce frequency-dependent changes for the resistive case. ADG736 in this mode would select an appropriate reference resistor R_f to set the gain. For instance, if the DUT is a 100Ωresistor, the system might switch in an R_f of 100Ωas well, yielding a convenient -1 V/V gain (flat 0 dB). In summary, a pure resistor DUT produces a frequency response that is flat in magnitude and shows only the -180° phase from the inverting feedback action – exactly what we see in the plotted results, and exactly what basic impedance theory predicts for a constant real impedance.

Capacitor as DUT

Simulated Frequency Response: When the DUT is a capacitor, the AC sweep shows that the magnitude of the transfer from input to U2's output rises with frequency. This may seem opposite to the impedance behaviour, but remember that U2's output represents the current through the DUT (times the feedback resistor). At low frequencies, the capacitor greatly impedes current flow – very little current flows, so U2 hardly needs to output any voltage to balance the bridge. The result is a very low output magnitude at the low end of the frequency sweep (in the Bode plot, the gain starts far below 0 dB for low f). As frequency increases by a decade, the capacitor's reactance $\frac{1}{\omega C}$ drops by a decade, meaning ten times more current flows for the same input voltage. U2 outputs a correspondingly larger voltage ($I \cdot R_f$) to maintain the virtual ground, roughly ten times higher for each decade increase in frequency. This produces an approximate +20 dB/decade slope in the magnitude plot for the capacitive DUT. The simulation indeed shows the output gain climbing with a slope of about +20 dB/dec, as expected. At the highest frequencies of the sweep, the magnitude may flatten or roll off slightly – this would likely be due to real-world limitations like op amp bandwidth or the transition where the capacitor's impedance becomes so low that other parasitics dominate. But in the ideal mid-frequency range, the plot matches the theoretical high-pass characteristic: very low at low f, rising linearly on the log scale as frequency increases. The phase plot for the capacitor DUT is around -90° across the frequency range (the simulation might show -89°, -91°, etc., hovering near -90°). This indicates that U2's output voltage (proportional to the capacitor's current) is almost exactly a quarter cycle out of phase with the input voltage. In a capacitor, the current leads the voltage by +90°; however, U2 inverts the current when converting it to a voltage output. The inversion flips that +90° lead into a -90° lag. The outcome is that the output voltage (which we use to measure current) lags the source voltage by roughly 90°, which is why the phase trace is around -90°. This is fully consistent with the capacitor's fundamental behaviour: the voltage lags the current by 90°. The negative sign from the inversion doesn't

change the magnitude of the phase difference, it just ensures that the op amp's output is on the opposite side of the phasor diagram (lagging instead of leading). The AC sweep results for phase confirm this: the phase stays near -90° for frequencies where the capacitor's response dominates. (At extremely low or high frequencies, there might be minor phase deviations if the circuit has other small reactances, but the ideal theory holds in the mid-band.)

Circuit Behaviour Explanation: In this auto-balancing configuration, the op-amp will adjust such that $\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{Z_C}$. Substituting $Z_C = \frac{1}{j\omega C}$, we get $\frac{V_{\text{out}}}{V_{\text{in}}} = -R_f \cdot j\omega C$. This transfer function has a magnitude of $R_f \cdot \omega C$ and a phase of -90° (the factor of j contributes +90°, and the negative sign inverts it to -90°). We can interpret this as a kind of active high-pass filter behaviour: at low ω, the gain $|V_{\text{out}}/V_{\text{in}}| = R_f \cdot \omega C$ is very small (tending to 0 as $\omega \to 0$), and at high ω it grows linearly with ω (in proportion to frequency). The op-amp U2 automatically produces this frequency response by balancing the bridge: at low f, the capacitor blocks current so well that almost no feedback voltage is needed (the summing node stays at 0 V with minimal U2 output). At high f, the capacitor allows a lot of current, and U2 must drive a larger output (through R_f) to counter that current and hold the node at 0 V. Op amp U2 thus ends up outputting a voltage that increases with frequency, reflecting the $I = C \cdot \frac{dV}{dt}$ law (higher frequency → faster voltage change → more current).

Inductor as DUT

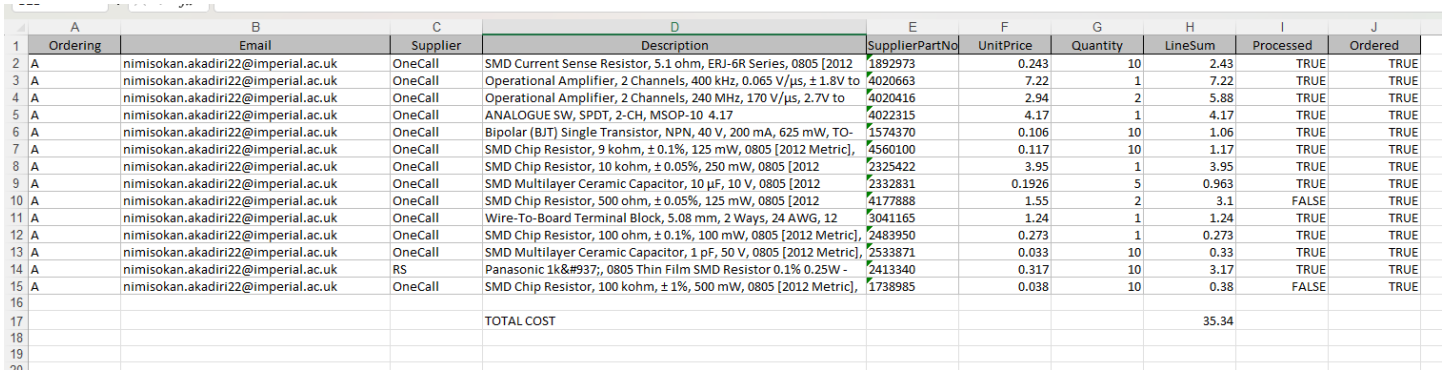
Simulated Frequency Response: For the inductive DUT, the AC sweep results show the opposite trend of the capacitor case. The magnitude of the transfer function (U2 output vs. input) falls as frequency increases. At the very low end of the frequency range, the plot may even start at an extremely high gain (in theory, as $f \to 0$, the required $V_{\text{out}}/V_{\text{in}} \to \infty$ because an ideal inductor at DC is just a short, drawing infinite current for any applied voltage). In practice, the simulation and the real circuit will be limited by resistances or the op amp's capabilities, so you'll see a very high gain at low frequency that levels off to whatever limit is imposed (for example, U2 saturating or a series resistance of the source limiting the current). As frequency increases from low values, the inductor's impedance ωL grows, so the current through the DUT for a given input voltage decreases. Consequently, U2 doesn't need to output as large a voltage to balance the node. The magnitude plot exhibits an approximate -20 dB/decade slope: each decade increase in frequency (making the inductor's impedance 10× bigger) reduces the current to 1/10, so U2's output voltage ($I \cdot R_f$) also drops to about 1/10, which is -20 dB. The AC sweep therefore shows a low-pass characteristic for the inductor: very high gain at low freq (limited by the circuit), and decreasing gain as freq grows. By the high end of the sweep, the magnitude may reach a very low level (approaching 0 dB or below, depending on R_f and L values), since the inductor eventually behaves almost like an open circuit for fast AC changes (very little current, hence very little output from U2). The phase plot for the inductor DUT is about +90° (in the simulation it might appear as +90 or sometimes -270° since +90° lead is equivalent to -270° depending on how the phase is unwrapped). A +90° phase difference here means U2's output voltage is leading the input voltage by 90°.

Circuit Behaviour Explanation: For the inductor, the feedback condition gives $\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{Z_L} = -\frac{R_f}{j\omega L}$. Simplifying, $\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{\omega L} \cdot \frac{1}{j} = \frac{R_f}{\omega L} \cdot j$. The magnitude of this is $\frac{R_f}{\omega L}$ (which decreases as frequency increases, since ωL is in the denominator), and the phase is +90° (the factor j). This is exactly what we described: a -20 dB/decade magnitude slope and a +90° phase shift. The op-amp U2 dutifully produces this transfer function by adjusting its output in response to the inductor's impedance.

Computation

The concept behind the simulation is to create distinct test cases for resistors, capacitors, and inductors by applying different ADC buffers in each case. Each test case is designed to simulate the characteristic behaviour of these components by using specific waveforms for current and voltage. In the `simulate_resistor_case()` function, the current and voltage are kept in phase with each other, as expected for a resistor. In the `simulate_capacitor_case()`, the voltage lags the current by 90 degrees, simulating the behavior of a capacitor. In the `simulate_inductor_case()`, the voltage leads the current by 90 degrees, reflecting the typical response of an inductor. These simulations are implemented by adjusting the ADC buffers (`adc1_buffer` for current and `adc2_buffer` for voltage) in each respective case, using the corresponding sine waveforms generated from the Look-Up Table (LUT). This allows for accurate testing of each component's impedance and parasitic characteristics. Additionally, we intended to compute the impedance and parasitic components based on the in-phase and quadrature components of the voltage and current signals. However, the implementation for this computation, although present in the code, is not fully functional at this stage. Despite this, the framework for processing the ADC data and calculating impedance components is already set up and could be utilised for future improvements and refinements in the system.

6 Bills of materials and total cost of orders submitted



	A	B	C	D	E	F	G	H	I	J
1	Ordering	Email	Supplier	Description	SupplierPartNo	UnitPrice	Quantity	LineSum	Processed	Ordered
2	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Current Sense Resistor, 5.1 ohm, ERJ-6R Series, 0805 [2012	1892973	0.243	10	2.43	TRUE	TRUE
3	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	Operational Amplifier, 2 Channels, 400 kHz, 0.065 V/µs, ± 1.8V to	4020663	7.22	1	7.22	TRUE	TRUE
4	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	Operational Amplifier, 2 Channels, 240 MHz, 170 V/µs, 2.7V to	4020416	2.94	2	5.88	TRUE	TRUE
5	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	ANALOGUE SW, SPDT, 2-CH, MSOP-10 4.17	4022315	4.17	1	4.17	TRUE	TRUE
6	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	Bipolar (BJT) Single Transistor, NPN, 40 V, 200 mA, 625 mW, TO-	1574370	0.106	10	1.06	TRUE	TRUE
7	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Chip Resistor, 9 kohm, ± 0.1%, 125 mW, 0805 [2012 Metric],	4560100	0.117	10	1.17	TRUE	TRUE
8	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Chip Resistor, 10 kohm, ± 0.05%, 250 mW, 0805 [2012	2325422	3.95	1	3.95	TRUE	TRUE
9	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Multilayer Ceramic Capacitor, 10 µF, 10 V, 0805 [2012	2332831	0.1926	5	0.963	TRUE	TRUE
10	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Chip Resistor, 500 ohm, ± 0.05%, 125 mW, 0805 [2012	4177888	1.55	2	3.1	FALSE	TRUE
11	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	Wire-To-Board Terminal Block, 5.08 mm, 2 Ways, 24 AWG, 12	3041165	1.24	1	1.24	TRUE	TRUE
12	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Chip Resistor, 100 ohm, ± 0.1%, 100 mW, 0805 [2012 Metric],	2483950	0.273	1	0.273	TRUE	TRUE
13	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Multilayer Ceramic Capacitor, 1 pF, 50 V, 0805 [2012 Metric],	2533871	0.033	10	0.33	TRUE	TRUE
14	A	nimisokan.akadiri22@imperial.ac.uk	RS	Panasonic 1kΩ, 0805 Thin Film SMD Resistor 0.1% 0.25W -	2413340	0.317	10	3.17	TRUE	TRUE
15	A	nimisokan.akadiri22@imperial.ac.uk	OneCall	SMD Chip Resistor, 100 kohm, ± 1%, 500 mW, 0805 [2012 Metric],	1738985	0.038	10	0.38	FALSE	TRUE
16										
17				TOTAL COST				35.34		
18										
19										

Figure 6: Budget showing cost of items ordered

7 Pseudocode for calibration

An attempt was made to implement this calibration process in software, but the results did not meet the professional standards expected for precise impedance measurement. Despite challenges during the implementation, the following pseudocode illustrates the intended calibration process, which aims to adjust for errors in magnitude and phase during DUT (Device Under Test) measurements.

The following pseudocode outlines the steps for performing the calibration and measurement of DUTs with automatic error correction:

```
// Initialize system (DAC, ADC, GPIO, Timer, Relay, UART)
Set default frequency range (100Hz, 1kHz, 10kHz, 100kHz)
Set reference components: Resistor (R_ref), Capacitor (C_ref), Inductor (L_ref)

// Calibration loop for each reference component
for each reference_component in [R_ref, C_ref, L_ref]:
    Set DUT to reference_component
    Wait for stabilization

    for each frequency in [100Hz, 1kHz, 10kHz, 100kHz]:
        Start DAC to generate sinewave at frequency
        Start ADC for voltage (V) and current (I)
        Wait for ADC samples

        Apply Goertzel to extract V_measured, I_measured, Phase_measured
        Z_measured = V_measured / I_measured
        Phase_error = Phase_measured - Expected_Phase(reference_component, frequency)
        Magnitude_error = |Z_measured| / Expected_Impedance(reference_component, frequency)

        Store Magnitude_error, Phase_error for frequency
        Log/Display calibration data

// Calculate final correction factors after all references
for each frequency in [100Hz, 1kHz, 10kHz, 100kHz]:
    Gain_correction = average(Magnitude_error)
    Phase_correction = average(Phase_error)

// DUT measurement and correction
while measuring DUT:
    Z_DUT_measured = Measure DUT
    Z_DUT_corrected = Apply corrections to Z_DUT_measured
    Display Z_DUT_corrected
```

8 Team member roles and contributions

Team Member	Role and Contributions
Dinushan	Initial Circuit Design, LTspice simulations, Error correction, Microcontroller Software development, Total Circuit and Microcontroller Implementation
Nimi	PCB design, Soldering, Hardware Testing

Table 1: Team Member Roles and Contributions

Appendix

1. Impedance Calculation

In this section, we calculate the impedance (Z) of the Device Under Test (DUT) based on the measurements of current and voltage.

1.1. Impedance (Z)

Impedance is computed using the series resistance (R_s) and series reactance (X_s):

$$Z = \sqrt{R_s^2 + X_s^2}$$

Where:

- R_s is the series resistance.
- X_s is the series reactance.

1.2. Series Resistance (R_s)

The series resistance R_s is calculated based on the voltage and current components. These components are obtained using the Goertzel algorithm:

$$R_s = \frac{(v_p \cdot i_q) - (v_q \cdot i_p)}{(i_p^2 + i_q^2)}$$

Where:

- v_p and v_q are the in-phase and quadrature components of the voltage signal.
- i_p and i_q are the in-phase and quadrature components of the current signal.

1.3. Series Reactance (X_s)

The series reactance X_s is calculated similarly to the series resistance:

$$X_s = \frac{(v_p \cdot i_q) + (v_q \cdot i_p)}{(i_p^2 + i_q^2)}$$

Where:

- v_p and v_q are the in-phase and quadrature components of the voltage signal.
- i_p and i_q are the in-phase and quadrature components of the current signal.

2. Phase Difference Calculation

The phase difference between the voltage and current is crucial for determining the nature of the DUT.

2.1. Phase Shift (ϕ)

The phase shift ϕ between the voltage and current is calculated as:

$$\phi = \text{atan2}(v_q, v_p) - \text{atan2}(i_q, i_p)$$

Where:

- $\text{atan2}(v_q, v_p)$ is the arctangent function to compute the phase angle of the voltage signal.
- $\text{atan2}(i_q, i_p)$ is the arctangent function to compute the phase angle of the current signal.

3. Quality Factor Calculation

The quality factor Q is an important parameter that gives insight into the energy dissipation of the system. It is calculated as:

$$Q = \frac{X_s}{R_s}$$

Where:

- X_s is the series reactance.
- R_s is the series resistance.

4. Parasitic Inductance and Capacitance Calculation

To analyze the parasitic components, such as inductance and capacitance, the following formulas are used:

4.1. Inductance (L_s)

The series inductance L_s is derived from the series reactance X_s and the angular frequency w:

$$L_s = \frac{X_s}{w}$$

Where:

- X_s is the series reactance.
- w is the angular frequency, where $w = 2\pi f$, and f is the frequency of the test signal.

4.2. Capacitance (C_s)

The series capacitance C_s is calculated as:

$$C_s = \frac{1}{w \cdot X_s}$$

Where:

- X_s is the series reactance.
- w is the angular frequency, where $w = 2\pi f$.

5. Goertzel Algorithm for Frequency Component Extraction

The Goertzel algorithm is a digital signal processing algorithm used to extract a specific frequency component from a signal.

5.1. Goertzel Algorithm Recurrence

The Goertzel algorithm is based on the following recursive relation:

$$s[n] = x[n] + 2 \cdot \cos(w) \cdot s[n-1] - s[n-2]$$

Where:

- $s[n]$ is the current sample in the algorithm.
- $x[n]$ is the input signal at the n-th sample.
- w is the angular frequency of the frequency of interest.
- $s[n-1]$ and $s[n-2]$ are previous states of the recurrence.

5.2. Real and Imaginary Components

After the recurrence relation, the real and imaginary components of the frequency component are computed as follows:

$$\text{real} = s[N-1] \cdot \cos(w) - s[N-2]$$
$$\text{imag} = s[N-1] \cdot \sin(w)$$

Where:

- N is the total number of samples.
- w is the angular frequency of the frequency of interest.

5.3. Frequency Bin Index

To extract the desired frequency component from the signal, the frequency bin index k is calculated as:

$$k = \frac{N \cdot f}{f_{\text{sample}}}$$

Where:

- N is the number of samples.
- f is the target frequency.
- f_{sample} is the sampling rate.

Summary of Formulas

- **Impedance:**

$$Z = \sqrt{R_s^2 + X_s^2}$$

- **Series Resistance (R_s):**

$$R_s = \frac{(v_p \cdot i_q) - (v_q \cdot i_p)}{(i_p^2 + i_q^2)}$$

- **Series Reactance (X_s):**

$$X_s = \frac{(v_p \cdot i_q) + (v_q \cdot i_p)}{(i_p^2 + i_q^2)}$$

- **Phase Difference (ϕ):**

$$\phi = \text{atan2}(v_q, v_p) - \text{atan2}(i_q, i_p)$$

- **Quality Factor (Q):**

$$Q = \frac{X_s}{R_s}$$

- **Inductance (L_s):**

$$L_s = \frac{X_s}{w}$$

- **Capacitance (C_s):**

$$C_s = \frac{1}{w \cdot X_s}$$

- **Goertzel Algorithm Recurrence:**

$$s[n] = x[n] + 2 \cdot \cos(w) \cdot s[n-1] - s[n-2]$$

- **Real and Imaginary Components:**

$$\text{real} = s[N-1] \cdot \cos(w) - s[N-2]$$

$$\text{imag} = s[N-1] \cdot \sin(w)$$

- **Frequency Bin Index:**

$$k = \frac{N \cdot f}{f_{\text{sample}}}$$

References

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