TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

MEAer (Integrated Master In Aerospace Engineering), Técnico, University of Lisbon

Laboratory 1: Circuit analysis methods

Group 3

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1 Introduction

The objective of this laboratory assignment is to study a circuit containing a sinusoidal voltage source V_I connected to a resistor R and a capacitor C in series. The circuit can be seen if Figure 1.

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In Section 2, a theoretical analysis of the circuit is presented. In Section 4, the circuit is analysed by simulation, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 5.

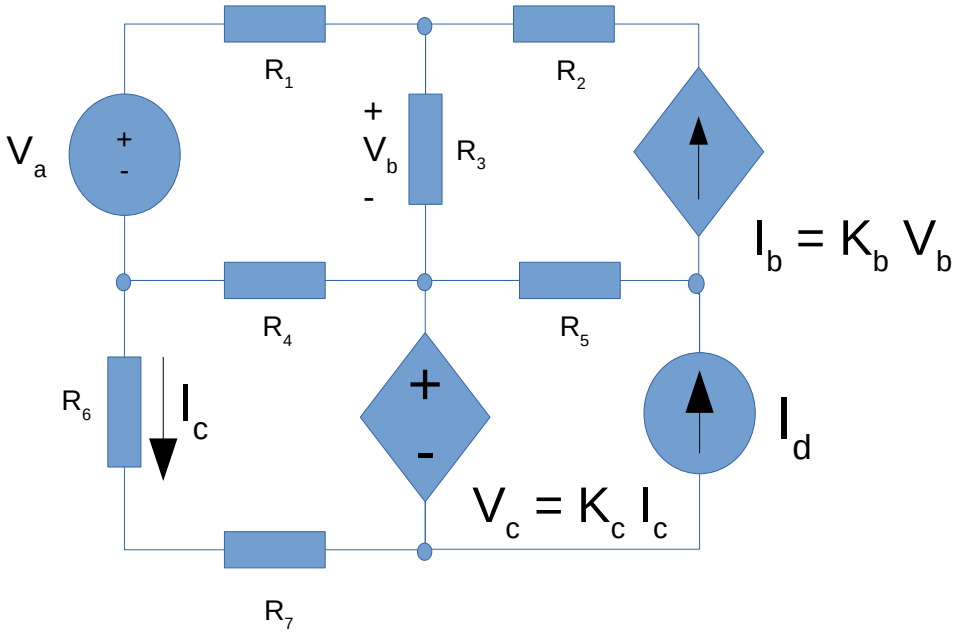

Figure 1: Voltage driven serial RC circuit.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically, in terms of its time and frequency responses.

3 Time response

The circuit consists of a single V-R-C loop where a current $i(t)$ circulates. The voltage source $v_I(t)$ drives its input, and the output voltage $v_O(t)$ is taken from the capacitor terminals. Applying the Kirchhoff Voltage Law (KVL), a single equation for the single loop in the circuit can be written as

$$Ri(t) + v_O(t) = v_I(t). \tag{1}$$

Because v_O is the voltage between capacitor C's plates, it is related to the current i by

$$i(t) = C\frac{dv_O}{dt}. \tag{2}$$

Hence, Equation (1) can be rewritten as

$$RC\frac{dv_O}{dt} + v_O(t) = v_I. \tag{3}$$

Equation (3) is a linear differencial equation whose solution is a superposition of a natural solution v_{On} and a forced solution v_{Of}:

$$v_O(t) = v_{On}(t) + v_{Of}(t). \tag{4}$$

As learned in the theory classes the natural solution is of the form

$$v_{On}(t) = Ae^{-\frac{t}{RC}}, \tag{5}$$

where A is an integration constant.

$$V_{Of}(t) = |\bar{V}_{Of}|cos(\omega t + \angle\bar{V}_{Of}), \tag{6}$$

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4 Simulation Analysis

Since this circuit is a steady one, the voltage or current values of the various components don't vary in time. Therefore, only the Operating Point Analysis is necessary in this circuit simulation

4.1 Operating Point Analysis

For this circuit's simulation on Ngspice, there was a need to introduce a nule voltage source between the ground node and the R7 resistor. The voltage related to node V2 will not appear in following table 1 because it has the same voltage as node V1 (its omission is necessary for the simulation to run correctly).

Table 1 shows the simulated operating point results for the circuit under analysis. Compared to the theoretical analysis results, one notices the following differences: describe and explain the differences.

Using the results of the theoretical analysis for mere guidance, we know the voltage values for the nodes, that should result from our simulation. We know then in which direction the voltage drops happen and we use this order for all branches except the current sources. In the current sources the order follows the current flow of such sources, as it is norm in Ngspice. Following the order we stated for the other branches means that the current that flows through every resistor must have a positive value in table 1, because in resistors the voltage drop and current flow have the same direction (resistors always consume energy!).

Analysing table 1, we notice that the current flowing through every resistor has a positive value, as it should be. I_a is the current flowing through R1, I_b is the current flowing through R2, I_c is the current flowing through R6 (and R7), and, finally, I_d is equivalent to Idd. Comparing the simulation results for the voltage and current values with the theoretical analysis values, we notice that the values for voltage in nodes V_1 to V_9 and the current for all four mesh currents are exactly equal, if we exclude all roundings carried out by NgSpice, since its precision (up to 7 significant algharisms) is far inferior to the precision we used in GNU Octave. (Shrinking the theoretical results to Ngspice precision, we get equal theoretical and simulation results).

Name	Value [A or V]
@gb[i]	-2.29771e-04
@idd[current]	1.005042e-03
@r1[i]	2.191669e-04
@r2[i]	2.297712e-04
@r3[i]	1.060424e-05
@r4[i]	1.185502e-03
@r5[i]	1.234813e-03
@r6[i]	9.663347e-04
@r7[i]	9.663347e-04
v(1)	-9.73914e-01
v(3)	1.063433e+01
v(4)	6.382611e+00
v(5)	6.843347e+00
v(6)	7.067298e+00
v(7)	1.953900e+00
v(8)	6.875344e+00
v(9)	0.000000e+00

Table 1: Operating point analysis. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

That being said, the theorectical results are equal to the simulation results (the complete accuracy is fruit of the staticness of the circuit), which confirms our theoretical analysis. The fact that the voltage and current results are equal obviously results in equal power values for each branch.

5 Conclusion

In this laboratory assignment the objective of analysing an RC circuit has been achieved. Static, time and frequency analyses have been performed both theoretically using the Octave maths tool and by circuit simulation using the Ngspice tool. The simulation results matched the theoretical results precisely. The reason for this perfect match is the fact that this is a straightforward circuit containing only linear components, so the theoretical and simulation models cannot differ. For more complex components, the theoretical and simulation models could differ but this is not the case in this work.

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