ISEL
INSTITUTO SUPERIOR DE ENGENHARIA DE LISBOA

Sistemas Embebidos

SPI Protocol

Microcontroller LPC1769

Licenciatura em Engenharia Eletrónica e Telecomunicações e de Computadores
Licenciatura em Engenharia Informática e de Computadores

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"O conteúdo deste ficheiro destina-se exclusivamente a apoiar os alunos que, tendo assistido às respetivas aulas, sabem enquadrar eventuais desafios, imprecisões, discordâncias, etc. que podem levar outros a equívoco."

Professor Hernâni Mergulhão

SPI - Serial Peripheral Interface

Overview

Provide an interface that supports serial, synchronous and full-duplex communications

Serial Data is transmitted over a single line one bit at a time in sequential order

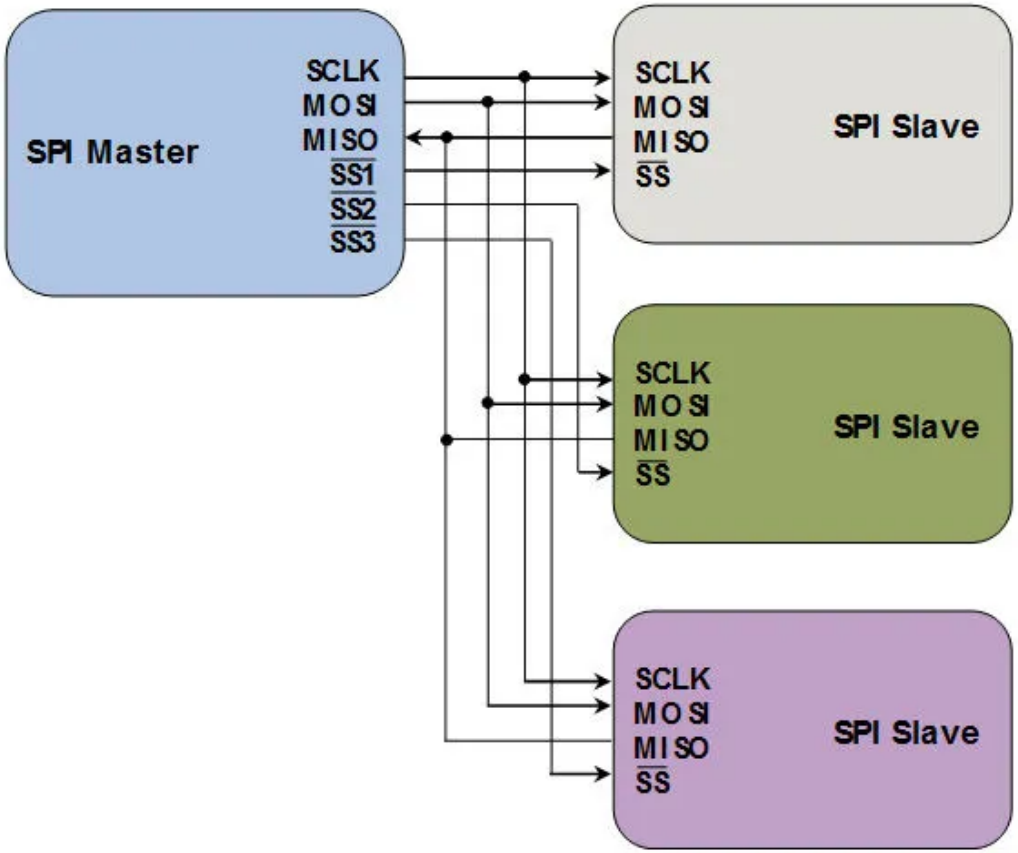
Synchronous Data is transmitted in a continuous data stream that works in conjunction with a timing signal used by both the transmitter and receiver

Full-duplex Data can be transmitted in both directions at the same time

SPI - Serial Peripheral Interface

Topologies

Star - Master connected to multiple slaves



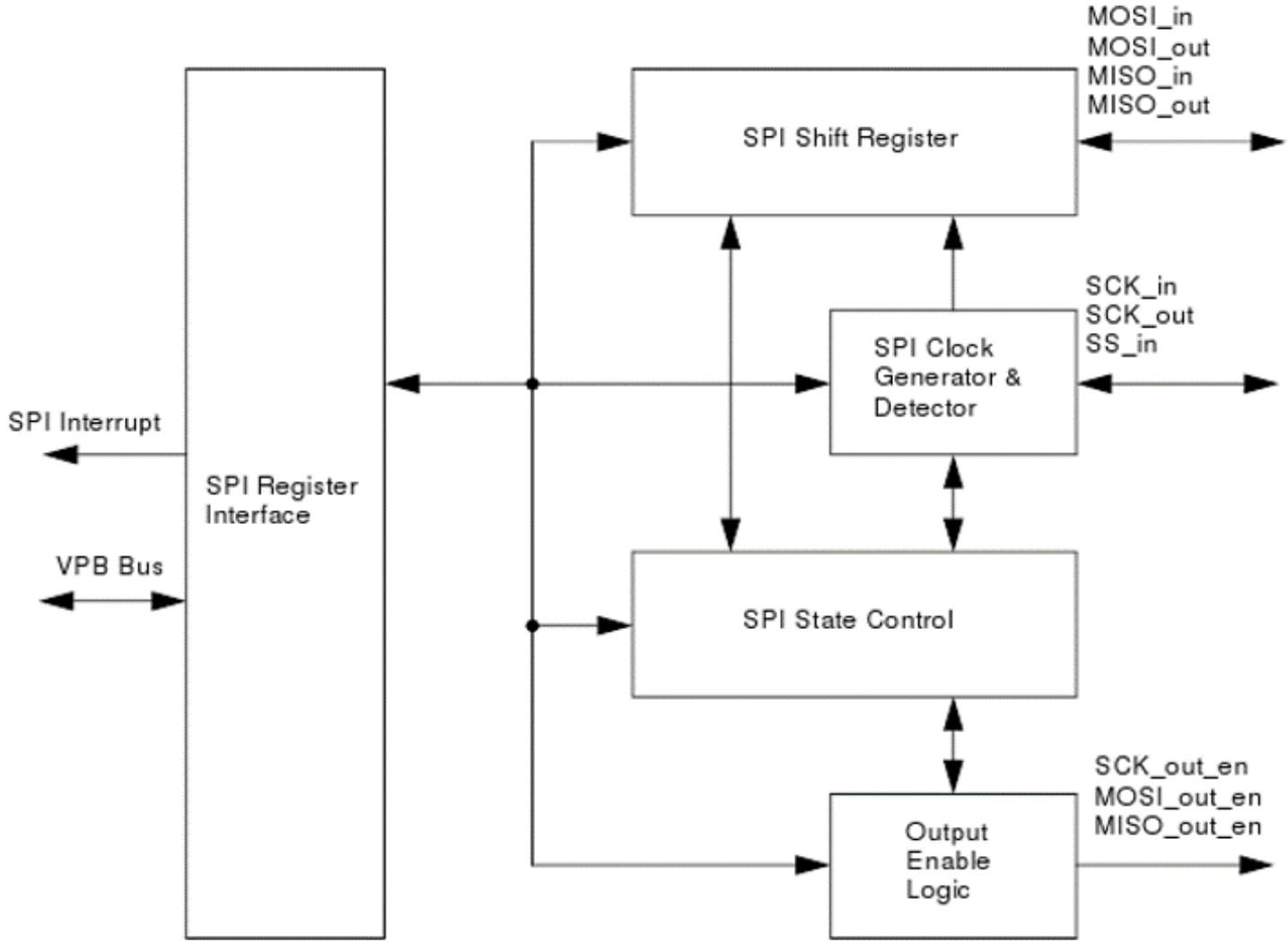
SPI - Serial Peripheral Interface

Features

- Compliant with Serial Peripheral Interface (SPI) specification
- Synchronous, Serial, Full Duplex Communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 or 16 bits transfer

SPI

Architecture



SPI

Pin description

SCK - Serial Clock

- Input/Output.
- Used to synchronize the transfer of data across the SPI interface
  - Always driven by the master and received by the slave
- Programmable to be active high or active low
  - Only active during a data transfer
    - Any other time, it is either in its inactive state, or tri-stated

SPI

Pin description

MISO - Master In Slave Out

- Input/Output
- Unidirectional signal used to transfer serial data from an SPI slave to an SPI master
  - When a device is a slave, serial data is output on this pin.
  - When a device is a master, serial data is input on this pin.
  - When a slave device is not selected, the slave drives the signal high-impedance.

SPI

Pin description

MOSI - Master Out Slave In

- Input/Output
- Unidirectional signal used to transfer serial data from an SPI master to an SPI slave
  - When a device is a master, serial data is output on this pin
  - When a device is a slave, serial data is input on this pin

SPI

Pin description

SSEL - Slave Select

- Input
- Active low signal indicates which slave is currently selected
- Each slave has its own unique slave select signal input
  - Must be low before data transactions begin
    - normally stays low for the duration of the transaction
  - If goes high any time during a data transfer
    - Transfer is considered to be aborted
    - Slave returns to idle
  - Not directly driven by the master
    - Could be driven by a simple general purpose I/O

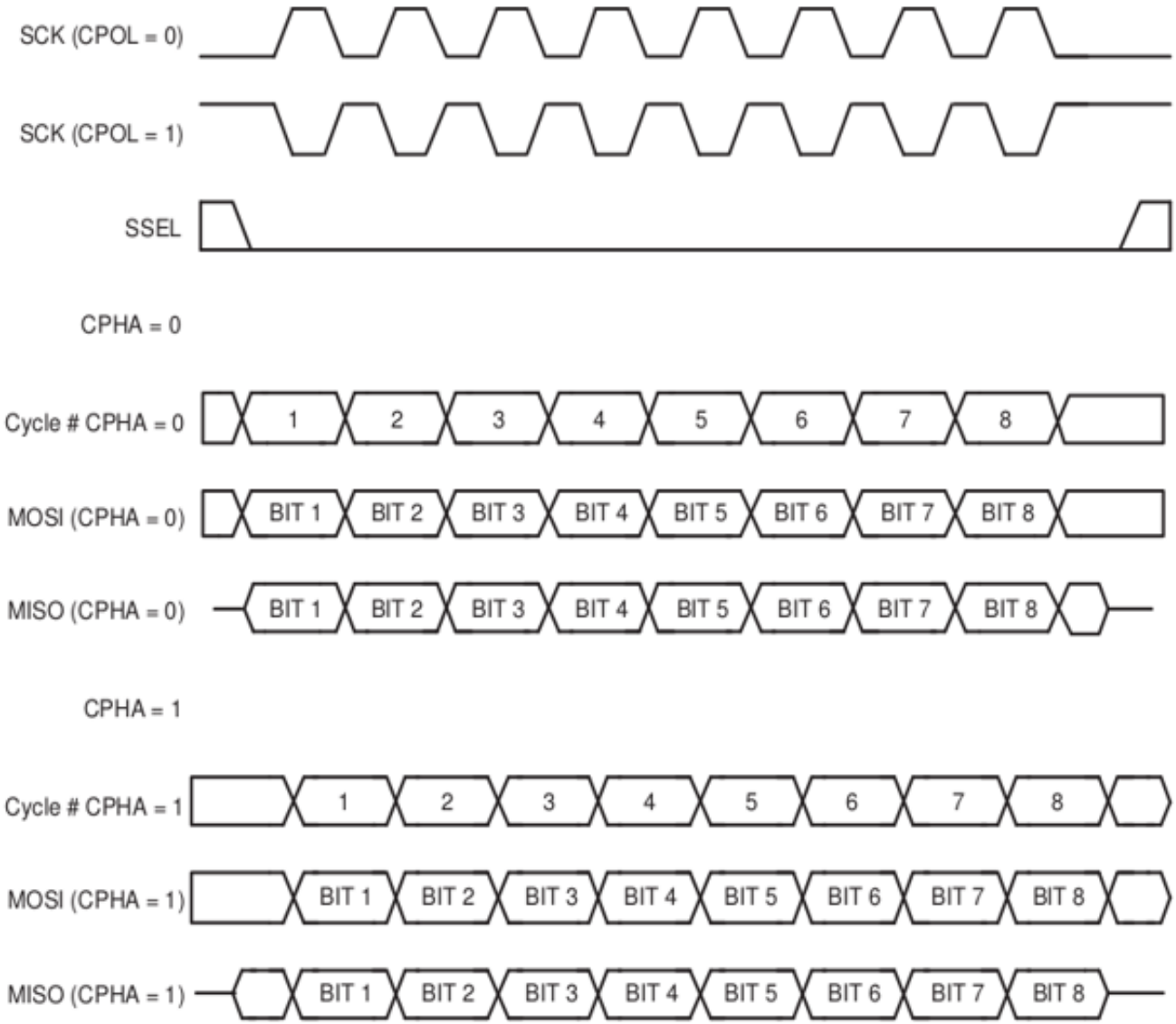
SPI

Description

CPOL and CPHA settings	When the first data bit is driven	When all other data bits are driven	When data is sampled
CPOL = 0, CPHA = 0	Prior to first SCK rising edge	SCK falling edge	SCK rising edge
CPOL = 0, CPHA = 1	First SCK rising edge	SCK rising edge	SCK falling edge
CPOL = 1, CPHA = 0	Prior to first SCK falling edge	SCK rising edge	SCK falling edge
CPOL = 1, CPHA = 1	First SCK falling edge	SCK falling edge	SCK rising edge

SPI

Data Transfer



SPI

Registers

Name	Description	Access	Reset Value[1]	Address
S0SPCR	SPI Control Register. This register controls the operation of the SPI.	R/W	0x00	0x4002 0000
S0SPSR	SPI Status Register. This register shows the status of the SPI.	RO	0x00	0x4002 0004
S0SPDR	SPI Data Register. This bi-directional register provides the transmit and receive data for the SPI. Transmit data is provided to the SPI0 by writing to this register. Data received by the SPI0 can be read from this register.	R/W	0x00	0x4002 0008
S0SPCCR	SPI Clock Counter Register. This register controls the frequency of a master's SCK0.	R/W	0x00	0x4002 000C
S0SPINT	SPI Interrupt Flag. This register contains the interrupt flag for the SPI interface.	R/W	0x00	0x4002 001C

SPI

Control Register

Bit	Symbol	Value	Description	Reset Value
1:0	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
2	BitEnable	0	The SPI controller sends and receives 8 bits of data per transfer.	0
		1	The SPI controller sends and receives the number of bits selected by bits 11:8.	
3	CPHA		Clock phase control determines the relationship between the data and the clock on SPI transfers, and controls when a slave transfer is defined as starting and ending.	0
		0	Data is sampled on the first clock edge of SCK. A transfer starts and ends with activation and deactivation of the SSEL signal.	
		1	Data is sampled on the second clock edge of the SCK. A transfer starts with the first clock edge, and ends with the last sampling edge when the SSEL signal is active.	

SPI

Control Register

Bit	Symbol	Value	Description	Reset Value
4	CPOL		Clock polarity control.	0
		0	SCK is active high.	
		1	SCK is active low.	
5	MSTR		Master mode select.	0
		0	The SPI operates in Slave mode.	
		1	The SPI operates in Master mode.	
6	LSBF		LSB First controls which direction each byte is shifted when transferred.	0
		0	SPI data is transferred MSB (bit 7) first.	
		1	SPI data is transferred LSB (bit 0) first.	
7	SPIE		Serial peripheral interrupt enable.	0
		0	SPI interrupts are inhibited.	
		1	A hardware interrupt is generated each time the SPIF or MODF bits are activated.	

SPI

Control Register

Bit	Symbol	Value	Description	Reset Value
11:8	BITS		When bit 2 of this register is 1, this field controls the number of bits per transfer:	0000
		1000	8 bits per transfer	
		1001	9 bits per transfer	
		1010	10 bits per transfer	
		1011	11 bits per transfer	
		1100	12 bits per transfer	
		1101	13 bits per transfer	
		1110	14 bits per transfer	
		1111	15 bits per transfer	
		0000	16 bits per transfer	
31:12	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

Status Register

Bit	Symbol	Description	Reset Value
2:0	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
3	ABRT	Slave abort. When 1, this bit indicates that a slave abort has occurred. This bit is cleared by reading this register.	0
4	MODF	Mode fault. when 1, this bit indicates that a Mode fault error has occurred. This bit is cleared by reading this register, then writing the SPI0 control register.	0
5	ROVR	Read overrun. When 1, this bit indicates that a read overrun has occurred. This bit is cleared by reading this register.	0
6	WCOL	Write collision. When 1, this bit indicates that a write collision has occurred. This bit is cleared by reading this register, then accessing the SPI Data Register.	0

SPI

Status Register

Bit	Symbol	Description	Reset Value
7	SPIF	SPI transfer complete flag. When 1, this bit indicates when a SPI data transfer is complete. When a master, this bit is set at the end of the last cycle of the transfer. When a slave, this bit is set on the last data sampling edge of the SCK. This bit is cleared by first reading this register, then accessing the SPI Data Register. **Note:** this is not the SPI interrupt flag. This flag is found in the SPINT register.	0
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

Data register

Bit	Symbol	Description	Reset Value
7:0	DataLow	SPI Bi-directional data port.	0x00
15:8	DataHigh	If bit 2 of the SPCR is 1 and bits 11:8 are other than 1000, some or all of these bits contain the additional transmit and receive bits. When less than 16 bits are selected, the more significant among these bits read as zeroes.	0x00
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

Clock Counter Register

- Master mode
  - Must be an even number greater than or equal to 8.
  - Rate may be calculated as: PCLK_SPI / SPI Clock counter value
    - SPI peripheral clock is determined by the PCLKSEL0 register contents for PCLK_SPI

Bit	Symbol	Description	Reset Value
7:0	Counter	SPI0 Clock counter setting.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

Clock Counter Register

- Slave mode
  - Must not exceed 1/8 of the PCLKSEL0 register contents for PCLK_SPI
  - The content of the Clock Counter Register is not relevant.

Bit	Symbol	Description	Reset Value
7:0	Counter	SPI0 Clock counter setting.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

Interrupt Register

Bit	Symbol	Description	Reset Value
0	SPIF	SPI interrupt flag. Set by the SPI interface to generate an interrupt. Cleared by writing a 1 to this bit. **Note:** this bit will be set once when SPIE = 1 and at least one of SPIF and WCOL bits is 1. However, only when the SPI Interrupt bit is set and SPI0 Interrupt is enabled in the NVIC, SPI based interrupt can be processed by interrupt handling software.	0
7:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SPI

CMSIS - Definitions

```
#define LPC_APB0_BASE          (0x40000000UL)

#define LPC_SPI_BASE           (LPC_APB0_BASE + 0x20000)

#define LPC_SPI                ((LPC_SPI_TypeDef       *) LPC_SPI_BASE )
```

```
typedef struct
{
  __IO uint32_t SPCR;
  __I  uint32_t SPSR;
  __IO uint32_t SPDR;
  __IO uint32_t SPCCR;
       uint32_t RESERVED0[3];
  __IO uint32_t SPINT;
} LPC_SPI_TypeDef;
```

SSP - Synchronous Serial Port

Features

Compatible with

- Motorola SPI
- 4-wire TI SSI
- National Semiconductor Microwire

Synchronous Serial Communication

Master or slave operation

8 frame FIFOs for both transmit and receive

4 to 16 bit data frame

DMA transfers supported by GPDMA

SSP

Pin description

SCK - Serial Clock (CLK / SK)

- Clock signal used to synchronize the transfer of data.
  - It is driven by the master and received by the slave.
- When the SPI interface is used is programmable
  - otherwise it is always active-high
- When not used
  - its inactive state
  - does not drive it (leaves it in high-impedance state)

SSP

Pin description

MISO - Master In Slave Out (DR-M,DX-S / SI-M,SO-S)

- Transfers serial data from the slave to the master
- When is a slave
  - Serial data is output on this signal
- When is a slave and is not selected
  - Leaves it in high-impedance state
- When is a master
  - It clocks in serial data from this signal.

SSP

Pin description

MOSI - Master Out Slave In (DX-M,DR-S / SO-M,SI-S)

- Transfers serial data from the master to the slave
- When is a master:
  - It outputs serial data on this signal
- When is a slave:
  - It clocks in serial data from this signal

SSP

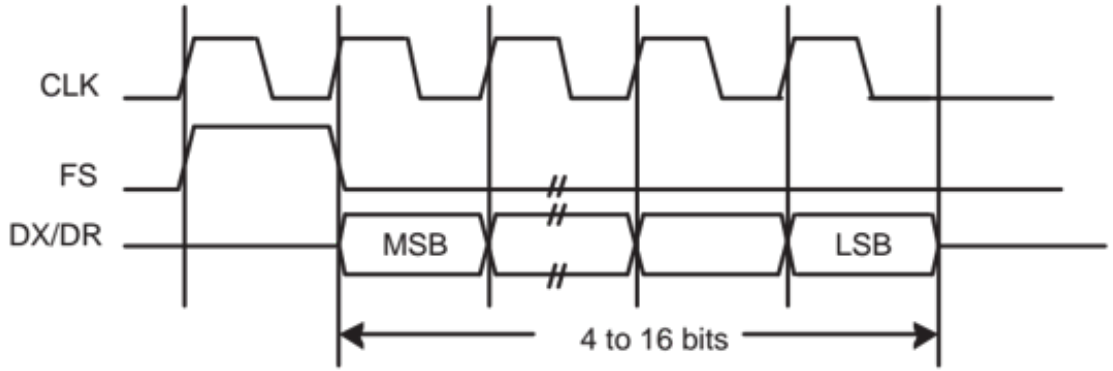
Pin description

SSEL - Slave Select (FS CS)

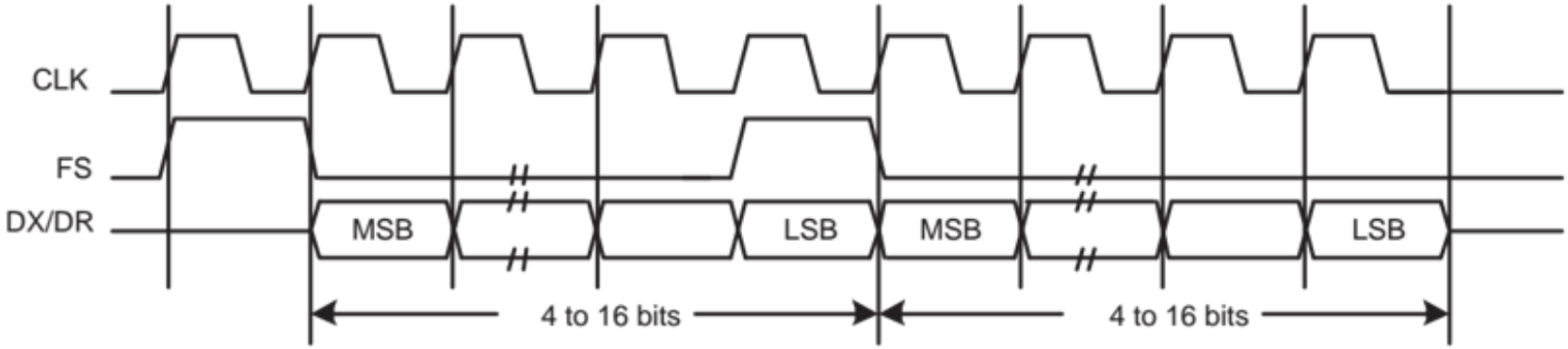
- When is a bus master
  - Drives to an active state before the start of serial data
  - Releases it to an inactive state after the serial data sent.
- The active state of this signal can be high or low depending upon the selected bus and mode.
- When is a bus slave:
  - Qualifies the presence of data from the Master

SSP

TI Synchronous Serial Frame Format



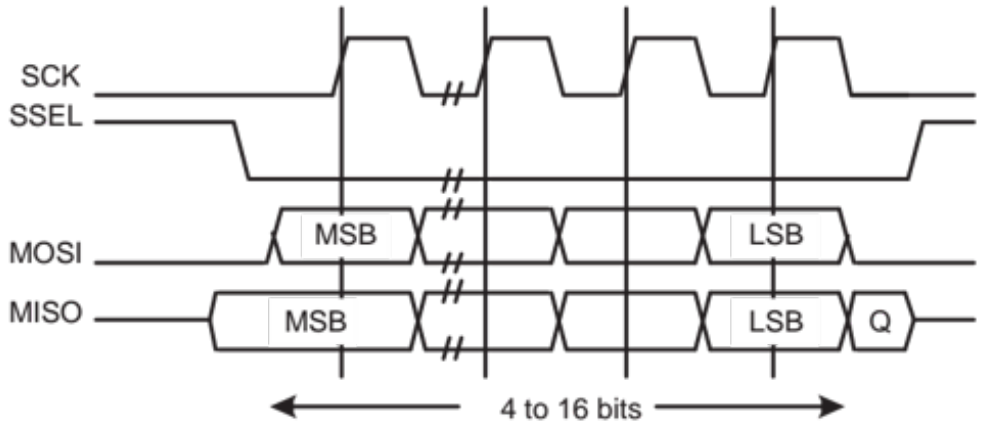
a. Single frame transfer



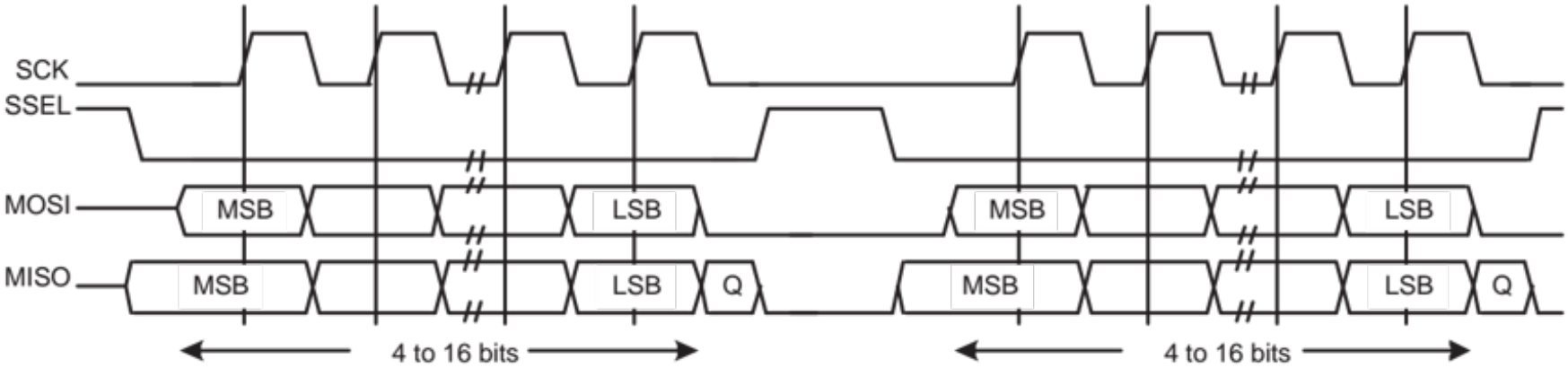
b. Continuous/back-to-back frames transfer

SSP

SPI Frame Format



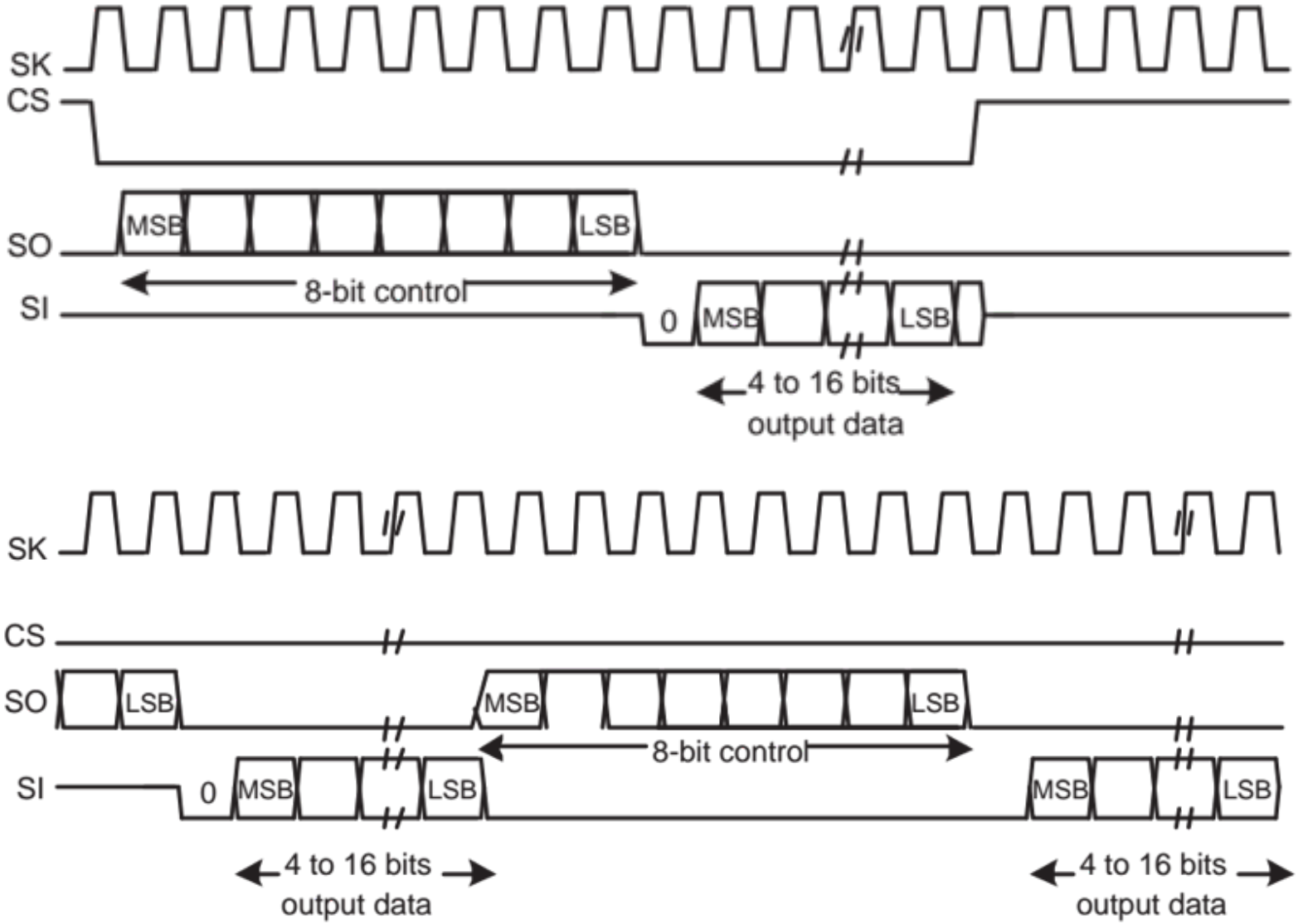
a. Single transfer with CPOL=0 and CPHA=0



b. Continuous transfer with CPOL=0 and CPHA=0

SSP

Microwire Frame Format



SSP

Registers

Generic Name	Description	Access	Reset Value[1]	SSPn Register Name & Address
CR0	Control Register 0. Selects the serial clock rate, bus type, and data size.	R/W	0	SSP0CR0 - 0x4008 8000 SSP1CR0 - 0x4003 0000
CR1	Control Register 1. Selects master/slave and other modes.	R/W	0	SSP0CR1 - 0x4008 8004 SSP1CR1 - 0x4003 0004
DR	Data Register. Writes fill the transmit FIFO, and reads empty the receive FIFO.	R/W	0	SSP0DR - 0x4008 8008 SSP1DR - 0x4003 0008
SR	Status Register	RO		SSP0SR - 0x4008 800C SSP1SR - 0x4003 000C
CPSR	Clock Prescale Register	R/W	0	SSP0CPSR - 0x4008 8010 SSP1CPSR - 0x4003 0010

SSP

Registers

Generic Name	Description	Access	Reset Value[1]	SSPn Register Name & Address
IMSC	Interrupt Mask Set and Clear Register	R/W	0	SSP0IMSC - 0x4008 8014 SSP1IMSC - 0x4003 0014
RIS	Raw Interrupt Status Register	R/W		SSP0RIS - 0x4008 8018 SSP1RIS - 0x4003 0018
MIS	Masked Interrupt Status Register	R/W	0	SSP0MIS - 0x4008 801C SSP1MIS - 0x4003 001C
ICR	SSPICR Interrupt Clear Register	R/W	NA	SSP0ICR - 0x4008 8020 SSP1ICR - 0x4003 0020
DMACR	DMA Control Register	R/W	0	SSP0DMACR - 0x4008 8024 SSP1DMACR - 0x4003 0024

SSP

Control Register 0

Bit	Symbol	Value	Description	Reset Value
3:0	DSS		Data Size Select. This field controls the number of bits transferred in each frame. Values 0000-0010 are not supported and should not be used.	0000
		0011	4-bit transfer	
		0100	5-bit transfer	
		0101	6-bit transfer	
		0110	7-bit transfer	
		0111	8-bit transfer	
		1000	9-bit transfer	
		1001	10-bit transfer	
		1010	11-bit transfer	
		1011	12-bit transfer	
		1100	13-bit transfer	
		1101	14-bit transfer	
		1110	15-bit transfer	
		1111	16-bit transfer	

SSP

Control Register 0

Bit	Symbol	Value	Description	Reset Value
5:4	FRF		Frame Format.	00
		00	SPI	
		01	TI	
		10	Microwire	
		11	This combination is not supported and should not be used.	
6	CPOL		Clock Out Polarity. This bit is only used in SPI mode.	0
		0	SSP controller maintains the bus clock low between frames.	
		1	SSP controller maintains the bus clock high between frames.	
7	CPHA		Clock Out Phase. This bit is only used in SPI mode.	0
		0	SSP controller captures serial data on the first clock transition of the frame, that is, the transition **away from** the inter-frame state of the clock line.	
		1	SSP controller captures serial data on the second clock transition of the frame, that is, the transition **back to** the inter-frame state of the clock line.	
15:8	SCR		Serial Clock Rate. The number of prescaler-output clocks per bit on the bus, minus one. Given that CPSDVSR is the prescale divider, and the APB clock PCLK clocks the prescaler, the bit frequency is PCLK / (CPSDVSR × [SCR+1]).	0x00
31:8	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Control Register 1

Bit	Symbol	Value	Description	Reset Value
0	LBM		Loop Back Mode.	0
		0	During normal operation.	
		1	Serial input is taken from the serial output (MOSI or MISO) rather than the serial input pin (MISO or MOSI respectively).	
1	SSE		SSP Enable.	0
		0	The SSP controller is disabled.	
		1	The SSP controller will interact with other devices on the serial bus. Software should write the appropriate control information to the other SSP registers and interrupt controller registers, before setting this bit.	
2	MS		Master/Slave Mode.This bit can only be written when the SSE bit is 0.	0
		0	The SSP controller acts as a master on the bus, driving the SCLK, MOSI, and SSEL lines and receiving the MISO line.	
		1	The SSP controller acts as a slave on the bus, driving MISO line and receiving SCLK, MOSI, and SSEL lines.	
3	SOD		Slave Output Disable. This bit is relevant only in slave mode (MS = 1). If it is 1, this blocks this SSP controller from driving the transmit data line (MISO).	0
31:4	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Status Register

Bit	Symbol	Description	Reset Value
0	TFE	Transmit FIFO Empty. This bit is 1 is the Transmit FIFO is empty, 0 if not.	1
1	TNF	Transmit FIFO Not Full. This bit is 0 if the Tx FIFO is full, 1 if not.	1
2	RNE	Receive FIFO Not Empty. This bit is 0 if the Receive FIFO is empty, 1 if not.	0
3	RFF	Receive FIFO Full. This bit is 1 if the Receive FIFO is full, 0 if not.	0
4	BSY	Busy. This bit is 0 if the SSPn controller is idle, or 1 if it is currently sending/receiving a frame and/or the Tx FIFO is not empty.	0
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Data register

Bit	Symbol	Description	Reset Value
15:0	DATA	**Write:** software can write data to be sent in a future frame to this register whenever the TNF bit in the Status register is 1, indicating that the Tx FIFO is not full. If the Tx FIFO was previously empty and the SSP controller is not busy on the bus, transmission of the data will begin immediately. Otherwise the data written to this register will be sent as soon as all previous data has been sent (and received). If the data length is less than 16 bits, software must right-justify the data written to this register. **Read:** software can read data from this register whenever the RNE bit in the Status register is 1, indicating that the Rx FIFO is not empty. When software reads this register, the SSP controller returns data from the least recent frame in the Rx FIFO. If the data length is less than 16 bits, the data is right-justified in this field with higher order bits filled with 0s.	0x0000
31:16	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Clock Prescale Register

Slave mode

- Must not exceed 1/12 of the SSP peripherial clock
- The content is not relevant.

Master mode

- Must be an even number greater then or equal to 2

Bit	Symbol	Description	Reset Value
7:0	CPSDVSR	This even value between 2 and 254, by which SSP_PCLK is divided to yield the prescaler output clock. Bit 0 always reads as 0.	0
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Interrupt Mask Set/Clear Register

Bit	Symbol	Description	Reset Value
0	RORIM	Software should set this bit to enable interrupt when a Receive Overrun occurs, that is, when the Rx FIFO is full and another frame is completely received. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTIM	Software should set this bit to enable interrupt when a Receive Time-out condition occurs. A Receive Time-out occurs when the Rx FIFO is not empty, and no has not been read for a "time-out period". The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	0
2	RXIM	Software should set this bit to enable interrupt when the Rx FIFO is at least half full.	0
3	TXIM	Software should set this bit to enable interrupt when the Tx FIFO is at least half empty.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Raw Interrupt Status Register

Bit	Symbol	Description	Reset Value
0	RORRIS	This bit is 1 if another frame was completely received while the RxFIFO was full. The ARM spec implies that the preceding frame data is overwritten by the new frame data when this occurs.	0
1	RTRIS	This bit is 1 if the Rx FIFO is not empty, and has not been read for a "time-out period". The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	0
2	RXRIS	This bit is 1 if the Rx FIFO is at least half full.	0
3	TXRIS	This bit is 1 if the Tx FIFO is at least half empty.	1
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Masked Interrupt Status Register

Bit	Symbol	Description	Reset Value
0	RORMIS	This bit is 1 if another frame was completely received while the RxFIFO was full, and this interrupt is enabled.	0
1	RTMIS	This bit is 1 if the Rx FIFO is not empty, has not been read for a "time-out period", and this interrupt is enabled. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	0
2	RXMIS	This bit is 1 if the Rx FIFO is at least half full, and this interrupt is enabled.	0
3	TXMIS	This bit is 1 if the Tx FIFO is at least half empty, and this interrupt is enabled.	0
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

Interrupt Clear Register

Bit	Symbol	Description	Reset Value
0	RORIC	Writing a 1 to this bit clears the “frame was received when RxFIFO was full” interrupt.	NA
1	RTIC	Writing a 1 to this bit clears the "Rx FIFO was not empty and has not been read for a time-out period" interrupt. The time-out period is the same for master and slave modes and is determined by the SSP bit rate: 32 bits at PCLK / (CPSDVSR × [SCR+1]).	NA
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

DMA Control Register

Bit	Symbol	Description	Reset Value
0	Receive DMA Enable (RXDMAE)	When this bit is set to one 1, DMA for the receive FIFO is enabled, otherwise receive DMA is disabled.	0
1	Transmit DMA Enable (TXDMAE)	When this bit is set to one 1, DMA for the transmit FIFO is enabled, otherwise transmit DMA is disabled	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

SSP

CMSIS - Definitions

```
#define LPC_APB0_BASE             (0x40000000UL)
#define LPC_APB1_BASE             (0x40080000UL)

#define LPC_SSP0_BASE             (LPC_APB1_BASE + 0x08000)
#define LPC_SSP1_BASE             (LPC_APB0_BASE + 0x30000)

#define LPC_SSP0                  ((LPC_SSP_TypeDef       *) LPC_SSP0_BASE )
#define LPC_SSP1                  ((LPC_SSP_TypeDef       *) LPC_SSP1_BASE )


typedef struct
{
  __IO uint32_t CR0;
  __IO uint32_t CR1;
  __IO uint32_t DR;
  __I  uint32_t SR;
  __IO uint32_t CPSR;
  __IO uint32_t IMSC;
  __IO uint32_t RIS;
  __IO uint32_t MIS;
  __IO uint32_t ICR;
  __IO uint32_t DMACR;
} LPC_SSP_TypeDef;
```